Microelectronics Presentation Days, 4th/5th Feb. 2004

Time	Title	Author/Company	Abstract Wednesday, 4th February 2004
Morning: Technologies and Design Methodology			
9:00	**Welcome**	ESTEC	Welcome and presentation of the Microelectronics Section
9:15	DARE – Desgin Against Radiation Effects	Emmanuel Liegeon, Alcatel Space Toulouse (F), Steven Redant, IMEC Leuven (B)	Because Rad-hard foundries are leaving the marketplace and to take advantage of the more advanced possibilities of deep sub-micron technologies, a Standard cell library has been developed for a commercial .18 technology. The cells of the library were radiation-hardened using layout techniques. A test chip and a complex telecom ASIC have been developed using this hardened library. -- In this presentation the work carried out, the current status of the library validation and characterization, and some preliminary results of the ongoing radiation tests will be reported. The test vehicles and the overall project flow will be briefly covered.
9:45	Preparation of an ECSS Standard for Space Product Assurance of ASIC/FPGA Development	Hartwig Storm, Volker Lück, Tesat-Spacecom GmbH, Backnang, (D)	A new draft ECSS Standard for ASIC/FPGA development has been established that consolidates and updates ASIC design and assurance requirements presently defined in various ESA and industry documents (such as QC/172/RDM, WDN/PS/700 and other pertinent documents). As a unified requirements document this Standard shall be applicable to the development of state-of-the-art custom designed circuits implementing digital, analogue or mixed signal functions to be applied for the fabrication of ASIC devices or the programming of FPGAs. The development work has been structured into management planning and engineering activities that are harmonised by quality assurance measures. The development flow consists of several development steps described by a corresponding list of engineering tasks, a list of quality checks and a list of required outputs. Each development step is concluded by a review meeting that decides on successful completion of this phase and an authorisation to proceed with the subsequent development phase.
10:15	MPW Programme for Space in CMOS 0.18 rad hard ATC18RHA technology	Jean Bouillon, ATMEL Nantes (F)	In our continuing commitment to give customers access to advanced technologies for Space applications, ATMEL with the support of the European Space Agency is in the process of developing an ASIC Space Multi Project Wafer offering (SMPW). -- This SMPW will reduce manufacturing costs of ASIC developments in CMOS 0.18µm technology (ATC18RHA) by sharing reticules and silicon costs between several designs. -- The Space Multi Project Wafer offering will produce a silicon service compliant with Space standards. -- This presentation will review some of the constraints we have to solve to set-up a service compliant with Space standards. Some specific milestones will also be introduced to allow a successful management of this approach.
10:45	**Coffee Break**		
11:00	FPGAs in Critical Applications and Model Support	Sandi Habinc, Gaisler Research, Gothenburg (S)	The dominating reprogrammable Field Programmable Gate Array (FPGA) devices currently on the space market are from Xilinx Inc. The devices have a good total dose resistance, but the on-chip configuration memory is soft with respect to Single Event Upsets (SEUs). -- Xilinx has in several publications stated that they have developed mitigation techniques that would cancel out the effects of SEUs in their FPGAs. During the last couple of years these techniques have been updated and improved. The first objective of this activity has been to compile and review all publications available concerning the use ofXilinx FPGAs in a harsh environment. -- The second objective has been to study the use of Triple Modular Redundancy (TMR) for the protection of combinatorial and sequential logic in reprogrammable logic devices. A VHDL approach has been developed for automatic TMR insertion and a demonstration design has been evaluated. The approach is called Functional Triple Modular Redundancy (FTMR).

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11:30	The SEUs Perl Tool	Daniel Gonzalez Gutierrez, ESTEC Microelectronics Section	Single Event Effects and in particular Single Event Upsets (SEUs) are of major concern when dealing with electronic designs that will suffer the consequences of a radiation environment. The sooner we know the effects of SEUs on a particular design, the better. This is the main reason for the development a tool able to emulate SEUs while still in the simulation (HDL) stages. -- The SEUs Perl Tool (SPT) consists of a set of perl and tcl scripts used to prepare the environment to be able to upset (bit flip) any register or internal signal of the design under test (DUT), while a simulation is running. A test bench for the DUT is needed in order to detect if the upsets modify in any way the behaviour of the design.
12:00	FT-UNSHADES, a Xilinx based SEU emulator	Miguel Angel Aguirre Echánove, Jonathan N.Tombs, AICIA-GTE (E)	HW SEU emulator test tool (Xilinx based) to facilitate automatic search, analysis and diagnosis and precharacterisation of SEU effects in IC designs.
12:30	**Lunch**		
Afternoon: Processors, System-On-Chip and On Board Data Handling			
13:30	ATMEL AT697 processor prototype development status	Nicolas Renaud, Atmel Nantes (F)	AT697 is the new ATMEL 32-bit Sparc processor based on the ESA LEON2 fault tolerant model, dedicated to space applications. After an overview of the project, the presentation brings information on the following aspects: on-going work in ATMEL on this development, description of the product as of today, expected performance and characteristics, development timeframe, test plan, and the road towards flight models.
14:00	LEONUMC – The LEON-2 Fault-Tolerant Processor in 0.18 um UMC Commercial Technology	Roland Weigand, ESTEC Microelectronics Section, Steven Redant, IMEC (B)	The LEON2 fault-tolerant (FT) VHDL model was mapped by ESA into 0.18 um UMC technology with commercial (Virtual Silicon) libraries. Layout was done by IMEC and the chip was manufactured on a MPW via Europractice. -- The objectives of this project were three-fold: Proving the efficiency of the FT circuitry (TMR with clock spreading, EDAC), measuring the radiation performance of a purely commercial technology compared to hardened technologies, and providing early prototypes of the radiation-hard LEON processor AT697 implemented by Atmel. -- Numerous challenges and pitfalls have led to lessons learned and workarounds. As a side effect, this work allowed us to gain valuable experience with the LEON-FT model itself and its implementation in 0.18 um technology, which proves to be extremely useful in supporting other LEON related developments.
14:30	Design of a test board, validation and radiation test of the LEON-UMC processor	Jiri Gaisler (S), Gaisler Research (S), Richard Pender, Pender Electronic Design (CH)	To test the functionality of the UMC 0.18 LEON-FT device, a prototype board was designed, and used for SEU testing using heavy-ion injection. The board was equipped with flash prom, 1 Mbyte of SRAM and 64 Mbyte of SDRAM. All tested LEON-FT devices operated satisfactory at 100 MHz, correctly executing a number of validation tests. One device was subjected to SEU Testing using the ESTEC Californium SEU Test equipment. Numerous SEU events were logged during the testing, including multiple events. All SEU events were correctly detected and corrected by the FT logic inherent in the design, and no crashes or anomalous behavior of the device occurred. However, the device was found to be susceptible to latch-up, which occured approximately once per 1/2 hour.

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15:00	ChipSat – a System-on-a-chip for Small Satellite Data Processing and Control: Architectural Study and FPGA Implementation	Tanya Vladimirova, Surrey Space Centre, and Alex da Silva Curiel SSTL, Guildford (GB)	This presentation will describe research work aimed at miniaturisation of the on-board data handling system of a small satellite. A mixed-mode application-specific integrated circuit that represents a single chip implementation of an on-board command and data handling subsystem for a low-cost small satellite is outlined. A system-on-a-chip design of an on-board computer is proposed, which is based on integration of soft intellectual property cores and is structured around the Leon microprocessor core. A downsized on-board computer implementation on a single programmable logic chip and a low-cost CCSDS-based communication system are described. Details are given about the design and integration of a mathematical floating-point co-processor core, based on the CORDIC algorithm, and a DMA controller core. The use of the system-on-a-chip in a "credit-card" size on-board computer design and aspects of reconfigurability are discussed.
15:30	**Coffee Break**		
16:00	Building Blocks for System-on-a-Chip: Spacecraft Controller on a Chip (SCoC)	Marc Lefèbvre, Marc Souyri, EADS-Astrium (Vélizy, F)	In the past years, the ASICs developed under ESA contracts were offered to European industrials as ASSP. Most of these chips were designed by using the VHDL language creating software macros that can be reused under certain conditions. The idea by now is to merge all these available blocks in a single ASIC called “System-on-a-Chip” that would be able to perform a large number of the Data Management System functions of a platform. The selected SoC is a “Spacecraft Controller on a Chip” that embeds LEON1 SPARC processor, PCI, Spacewire and 1553 interfaces and TMTC management function. The SCoC has been designed and implemented into a commercial XILINX FPGA mounted on a specifically developed board -BLADE.
16:30	SpaceWire Router	Stephan Fischer, Paul Rastetter, Tim Pike, EADS Astrium Munich (D), Gerald Kempf, Austrian Aerospace Vienna (A), Steve Parkes, University of Dundee (GB)	SpaceWire is a standard for high-speed data handling which is intended to meet the needs of future, high-capability, remote sensing instruments. The standard is based on two existing commercial standards, IEEE-1355 and LVDS, which have been combined and adapted for use in space applications. Basically, the SpaceWire network consists of nodes (i.e. sources or destinations of data packets) and packet switching routers which are interconnected through bi-directional point-to-point high-speed (>100Mbps) digital serial links. Due to the large number of modules to be interconnected, it is essential to have a SpaceWire packet switching router. In this project a new radiation tolerant SpaceWire router is developed which is fully compliant to the latest SpaceWire standard and which comprises eight SpaceWire ports and two external parallel ports. In the project a FPGA version of the Router is designed and validated. For the validation exercise the necessary tools and SpaceWire compliant nodes are developed. Following the validation exercise, the ASIC design is finished and finally the Router ASIC is manufactured and validated.
16:50	Next Generation TMTC System (NTTS)	Brian Tatman, Gregg Sims, Judie Elington, Satellite Services, Katwijk (NL)	The NTTS system has been developed to provide a flexible Telemetry and Telecommand system for spacecraft and ground system testing. Traditional systems constructed TM and TC processing chains from discrete components, boards, modules and units which limited their flexibility, upgradability and re-use. The NTTS system uses System-On-A-Programmable-Chip (SOPC) technologies to integrate the entire TM (acquisition and simulation) and TC (transmission and reception) processing chains into single chips. -- The technology also uses software controlled in-circuit reprogramming to allow user selectable firmware versions and "emailable upgrades". -- The presentation will focus on: the backgrounds to the project, the integration process, the proven success through the deployment of the completed systems as well as future and on-going development and use.

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17:20	Single Chip Telemetry and Telecommand (SCTMTC) ASIC	Tom Seeman, Saab Ericsson Space AB, Sandi Habinc, Gaisler Research (Gothenburg, S)	The objective of the Single Chip Telemetry and Telecommand (SCTMTC) ASIC development has been to provide the European space market with a much awaited standardised single chip solution for on-board telemetry and telecommand data handling. All functions that are normally operated in hot redundancy are now included in a single device, permitting the on-board computer to be used in cold redundancy. -- The SCTMTC fully implements the CCSDS recommendations and the recently established ECSS standards, adopting all new frame lengths and packet formats. The SCTMTC does not only incorporate all the functions previously implemented in devices such as the VCA, VCM and the MA1916, it also provides several novel functions and increased performance. -- The telemetry encoder implements eight Virtual Channels (VC) using a built-in router making it possible to send telemetry packet data to either VC via a SpaceWire interface. Telemetry packet data can also be sent using an individual PacketWire interface for either VC. The SCTMTC implements new encoding schemes such as turbo coding and punctured convolutional coding, allowing to either reduce the downlink power output or to increase the downlink bit rate. -- The telecommand decoder implements Multiple Access Point (MAP) de-multiplexing and re-routing, providing redundant paths for distributing telecommand packets. The vital Command Pulse Distribution Unit (CPDU) can be shared between the telecommand decoder, an external reconfiguration unit and the on-board computer. A novel approach is used to multiplex and prioritise the CPDU packets originating from these three sources. -- The performance of the SCTMTC is scalable, being proportional to the number of external memory devices that are attached. The minimum configuration requires one SRAM and one PROM device. The maximum configuration allows two of each, providing improved throughput performance. Optional EDAC support is provided for the external memory. -- By providing both ECSS SpaceWire and PacketWire serial synchronous interfaces for telemetry packet input, telecommand packet output, and control, the SCTMTC is versatile enough to fit any type of on-board system.
17:50	The New SpaceWire Compliant SMCS332 / SMCSlite ASIC	Stephan Fischer, Paul Rastetter, Uwe Liebstückel, Tim Pike, EADS Astrium Munich (D), Steve Parkes, University of Dundee (GB)	The SMCS (Scalable Multi-channel Communication Sub-system) device is a radiation hardened communication controller designed for space applications. The SMCS provides hardware supported execution of the major parts of the inter-processor communication protocol. Generally two devices are available using a common coder/decoder. The SMCS332 implements three IEEE-1355 links and the SMCSlite (or SMCS116) implements one link. The current devices base on the IEEE-1355 protocol and are not based on the SpaceWire standard. Since the SpaceWire standard is becoming increasingly important and both devices are frequently used communication controllers, new versions of the SMCS332 and of the SMCSlite will be developed by EADS Astrium GmbH and Atmel with ESA support. These versions will be fully compliant to the SpaceWire standard and known anomalies of both devices will be corrected. In order to ensure that existing SMCS components can continue to be used, it is foreseen that the new versions will be PIN compatible with the present products. Both devices will be manufactured in a radiation-tolerant gate array technology from Atmel (MG2RT and MG2RTP respectively). The new SMCS332 and SMCSlite devices are planned to be available as catalogue products in 2004 Q3.

Time	Title	Author/Company	Abstract Thursday 5. February 2004
Morning: Navigation and Signal Processing			
9:00	High-performance low power front-end for multi-band satellite navigation systems	Frederik Naessens, IMEC, Leuven (B)	Portable satellite positioning systems are commonly used. Focus is being put at low power, multi-band receivers. In this project a low power satellite receiver for GPS and GLONASS bands is targeted. The front-end, using subsampling at 232 MHz, offers the possibility to process all the satellite bands (both GPS as GLONASS). This technique requires a good pre-filtering of the signal. The filters are implemented in IMEC's MCM technology where the amplifiers and ADCs are flip chipped onto. This enables a high integration of the complete front-end. The ADC has an accuracy of 1 bit, but through decimation filtering (reduction of sampling frequency), the accuracy can be increased to 2 bits. The digital processing will be done on an FPGA. Implementing this into an ASIC can further reduce the power dissipation. The complete system will be tested using the existing AGGA-2 GNSS receiver. As a part of the project, multipath mitigation and semi-codeless tracking techniques were implemented and tested by Septentrio.
9:30	AGGA-3: Next Generation GNSS ASIC	Stefan Berberich, EADS-Astrium, Ottobrunn (D)	The AGGA-3 is a compact, low consumption next generation GNSS ASIC optimised for earth applications which includes the LEON-FT microprocessor. The GNSS baseband processor enhances the proven AGGA-2 concept with additional functionalities such as digital down conversion, beamforming, enhanced power level detection, loop aiding support, fast acquisition support through FFT and optimised raw sampling. Implementation losses are reduced due to 3-bit pre-correlation processing . The number of highly configurable GNSS channels is increased to 36. The AGGA-3 provides enhanced high speed digital signal processing functionality, a powerful on-board microprocessor and flexible interfaces for a wide range of GNSS applications.
10:00	T@MPO: Turbo coding at minimum power ASIC	Lieven Hollevoet, IMEC, Leuven (B)	Turbo coding allows getting the best performance out of a channel, thereby approaching Shannon's limit. However, the attractive features of the iterative decoding scheme come at the cost of a high computational complexity, a considerable decoding latency, and last but not least a high decoding power requirement. IMEC has implemented the T@MPO (Turbo coding At Minimum POwer) ASIC. The T@MPO incorporates the complete functionality of a full-duplex convolutional turbo encoder and decoder. It tackles the two major bottlenecks (latency and decoding power) while achieving bit rates of up to 80 Mbps. The T@MPO is designed in 0.18 um CMOS technology and consumes less then 10 nJ per decoded bit. Application of IMEC's Data Transfer and Storage Exploration (DTSE) methodology and innovative research efforts have lead to what is to our knowledge the world record in turbo decoding energy per bit.
10:30	**Coffee Break**		
11:00	BroadCast: A Combined Satellite/ Terrestrial UMTS Terminal Platform	Lieven Philips, Agilent Technologies (B)	In the BroadCast project, Sirius Communications (and then Agilent Technologies Belgium) have developed flexible digital IP blocks for the inner and outer modem for a reconfigurable W-CDMA transceiver. Reconfigurability includes addressing satellite the W-CDMA air interface extension on top of terrestrial UMTS, flexible channel allocation, extension possibility to other chip rates, algorithmic choices for the receiver algorithms, etc. The digital part has been mapped on an FPGA-based platform, under control of an ARM7 subsystem. An analog frontend interface board allows connectivity with various radio architectures. The platform has been tested in the field with various radio implementations, in collaboration with several organizations and companies. In one of the use cases, the platform is currently being upgraded and demonstrated for S-DMB in the MoDiS and Maestro EU projects.

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11:30	ASTRIX ASIC	Franck Koebel, EADS-ASTRIUM (Vélizy, F) and IXSEA (F)	ASTRIX is a full european solid-state gyroscope product family for every space application (LEO, GEO, science, deep space, ...) developed under ESA and CNES funding. The ASTRIX ASIC is the main digital component of this Fiber Optical Gyroscope family developed commonly by Astrium and IXSEA companies. This ASIC ensures all the digital signal processing related to the fiber optic loop. This ASIC is also in charge of the following management functions : communication with the OBC through 1553 or UART links, acquisition of TM at board level, on-chip datation and mode control including test modes. The ATMEL MG2RT technology is the target for the ASTRIX ASIC.
12:00	Autocorrelation Spectrometers	Dr. Anders Emrich, J. Dahlberg, L. Landen, S. Andersson, C. Tegnander, Omnisys, Gothenburg (S)	The use of autocorrelation spectrometers is planned for several future space missions for both aeronomy and astronomy. The autocorrelation technique promise to improve performance as well as reliability, compared to alternatives such as the chirp or AOS based solutions. It will have substantially lower mass and cost compared to the alternatives, and now also much less power consumption. -- At 1995, state of the art was correlator chips with 50 MHz clock rate, with 16 correlator channels, and the ADC/digitizer was implemented with descrite designs. At 1997, the chip set for the ODIN satellite was presented by Omnisys, the first integrated full custom chip set, a CMOS correlator chip and a bipolar digitizer. The development, now partly financed by ESA, has continued with two generations of chip sets, and we have now chips that process 1024 correlator channels, over 2 GHz bandwidth. We have been about a factor of 200 better than Moores law, and we should now focus on getting spectrometers out to the user community. -- The design and design approach will be presented, as well as test results. The results are from the performance test in the lab, total dose radiation tests, as well as demonstrator test by scientist, observing the ozone line at 110 GHz.
12:30	**Lunch**		

Time	Title	Author/Company	Abstract Thursday 5. February 2004
Thursday 5. February 2004, Afternoon: Imaging and Mixed Signal Developments			
13:30	FlexWave Image Compression	Jan Bormans, IMEC (B)	The FlexWave has been developed as a dedicated image compression component for spaceborne applications, enabling a multitude of application scenarios, including lossless and lossy compression. The key functionality of the FlexWave is the LWT processor: a superscalar architecture with dedicated processing modules, interchanging their data along localized data transfer busses for high-speed processing. The architecture has been tailored to achieve a minimal memory size and access cost. For 1k x 1k images, the memory cost has been reduced with one order of magnitude compared to more conventional implementations. -- The project outcome includes a design kit and an FPGA prototype. Additionally, the FlexWave technology has impacted ongoing standardization efforts in the context of the Consultative Committee for Space Data Systems (CCSDS).
14:00	Recent and future rad-tolerant CMOS image sensors	Werner Ogiers, FillFactory nv, Mechelen (B)	We discuss the existing IRIS3 sensor, a 700kpixel monitoring camera-on-a-chip, and the forthcoming HAS, a high-end star sensor, and LCMS, a low-end star sensor with on-chip pre-processing and SpaceWire link.
4:30	Development of a flight-worthy microcamera based on the CMOS Integrated Radiation tolerant Imager System (IRIS3)	Tom Torfs, Thys Cronje, Chris Van Hoof, IMEC, Leuven (B), Werner Ogiers, FillFactory, Mechelen (B)	Based on the IRIS-3 CMOS camera-on-a-chip, a compact visual inspection camera for use on spacecraft has been built. Both a black-and-white and color version of the camera has been developed. A new, flat type of space-qualified housing has been designed and produced, as well as custom optics, at OIP Sensor Systems. -- The camera features 2 Gbit of SDRAM memory for storage of up to 82 full-frame (1024 x 768 pixels) images, including error-detection-and-correction redundancy. This image buffer can be automatically filled with images taken at regular intervals, from one image per 32 seconds up to the maximum frame rate of 10 images per second. -- The camera interfaces to the spacecraft using RS-422-like asynchronous serial (at up to 25Mbaud) or TTC-B-01 synchronous serial protocols, and can employ the CCSDS-ESA packetizing protocol for telecommand and telemetry. It operates directly from the 28V spacecraft power bus. -- Environmental tests on the camera are planned for the first quarter of 2004.
15:00	**Coffee Break**		

Time	Title	Author/Company	Abstract Thursday 5. February 2004
15:30	The FEIC development for the NPAL Project – A Core Image Processing Chip for Smart Landers Navigation Applications	Marc Souyri, EADS Astrium, Vélizy (F), Benoit Frapard, Christian Boléat, Gregory Flandin, EADS Astrium Toulouse (F)	The “Feature Extraction Integrated Circuit” -or FEIC- development is part of the “Navigation for Planetary Approach and Landing” study conducted by a consortium led by Astrium for ESA (Contract AO/1-3839/NL/FM). -- The NPAL study aims at developing a complete navigation camera demonstrator for enabling soft landing capability for future exploration missions, the BepiColombo serving as a reference mission. -- The FEIC is a key element in this compact camera, in charge of the most demanding image processing algorithm for extraction and tracking, to be continuously operated on the image flow at a high rate for providing the OBC with smart data in support to the piloting and navigation of an active lander in a rough unknown area. The FEIC first capability is to extract specific feature points in the image by using a Harris algorithm, and managing subsequenlty a list of candidate points, that is sent to the OBC for selection via a SpaceWire interface. The FEIC then displays a generic correlation capability that is used to track surface feature points across a sequence of images, measuring the motion of these points to support surface relative navigation. -- The FEIC features a parallel access through a flip-flop buffer for fast image transfer. The FEIC implements a SpaceWire router for command / control of the camera and direct interface to the navigation processor. The NPAL camera is specified for a 20 Hz image rate at high resolution (1024 x 1024). -- The FEIC in the NPAL project is implemented inside a X2CV6000 Xilinx FPGA in order to test it on a dedicated System and Validation Test bench. The FPGA is then further integrated onto the camera electronics in an elegant breadboard of the camera, functionally and mechanically representative of the flight hardware. The camera is expected to be available by the second semester of 2004.
16:00	MSREM Breadboard development	Jack Schneider, Hans-Ulrich Mathys, Contraves (CH)	Improvement developments of SREM (Standard Radiation Environmental Monitor) using the SIP (Small Instrument Point) for total dose measurements and an A/D converters for particle counting.
16:30	STJ-SARA	Gunnar Maehlum, S. Mikkelsen, N. Pavlov, Ideas (N)	Superconducting Tunnel Jun+D82ctions have been extensively investigated as photon detectors covering the range from near-infrared to X-ray energies. STJ detector developments now focus on the integration of many devices into large imaging arrays. However, current state-of-the-art preamplifier electronics for these detectors still rely on circuits build from discrete components. An attempt to integrate 64 preamplifier channels into an ASIC set was made. Two ASICs have thus been developed. One consists of 64 low-noise, low-offset pre-amplifier channels, while the other contains the same number of shaping filters and threshold detection circuits. The inputs are designed to handle large capacitive load and at the same time have exceptionally low noise The accompanying trigger ASIC incorporates 64 CR-RC shaping amplifiers, comparators and a hit address encoder. Both ASICS were realized in 0.8µm CMOS technology. In parallel an ADC board was developed for simultaneous readout and analogue to digital conversion of signals from a 128 pixel STJ array using the chip-set.
17:00	High Performance Monolithic AD Converter Design	Väinö Hakkarainen, Markku Åberg, VTT, HUT and Nokia (SF)	VTT, Helsinki University of Technology and Nokia are designing a 8-bit 2 GSPS analogue-to-digital converter, using a 0.35 mm SiGe process. The design is based on the time interleaved architecture with 24 parallel pipe line converters, ”fingers”, having a sampling frequency of 80 MHz. The pipe line converters consist of 1.5 bit stages and a 2 bit flash stage, and have a resolution of 10 bits. The timing of the fingers is done with a delay-locked loop (DLL) that is taking the reference from an external crystal oscillator. The main issues of the design are low jitter and low power consumption. To find an optimum trade-off between these a combined DLL and clock divider strategy is used. In pipe line converter fingers power is reduced by double sampling, i.e. using one operational amplifier for a pair of channels in opposite phase, and by scaling the stages towards the back end of the converter. SiGe transistors are used only in the most critical blocks: operational amplifiers of the sample-and-hold and converter stages. All other blocks are pure CMOS.
17:30	**Conclusion**		