FlexWave: Development of a Wavelet Compression Unit

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SEEDS FOR TOMORROW'S WORLD

Outline

- Scope and motivation
- FlexWave image encoder
- Local Wavelet Transform (LWT) processor
- CCSDS context
- Results

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Scope and Motivation

- To develop an image compression device, together with a bit-true SW model and synthesizable HW model
- For different missions and usage contexts
  - Lossless/lossy
  - Image-based/push-broom
  - Visual/IR/… data
  - Different storage and/or transmission characteristics
- 10 Msample/s
- Enabling low-power solutions

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Wavelet-based Compression

- Wavelets: intrinsic scalability characteristics
  - Quality scalability: graceful increase of the image quality (up to lossless)
  - Spatial scalability: graceful increase of the image size (“thumbnailing” possible)
- In lossy mode: type of artefacts can be influenced by wavelet filter choice
- No explicit tiling of image needed (as in e.g., DCT-based schemes)
- Excellent compression performance in entropy coder chains
- But: potentially complex hardware implementation
  - Large memory sizes
  - Large latency between input availability and production of minimal data entities for entropy coding
  - Arithmetic coding

FlexWave-II: Flexible Wavelet-based Solution

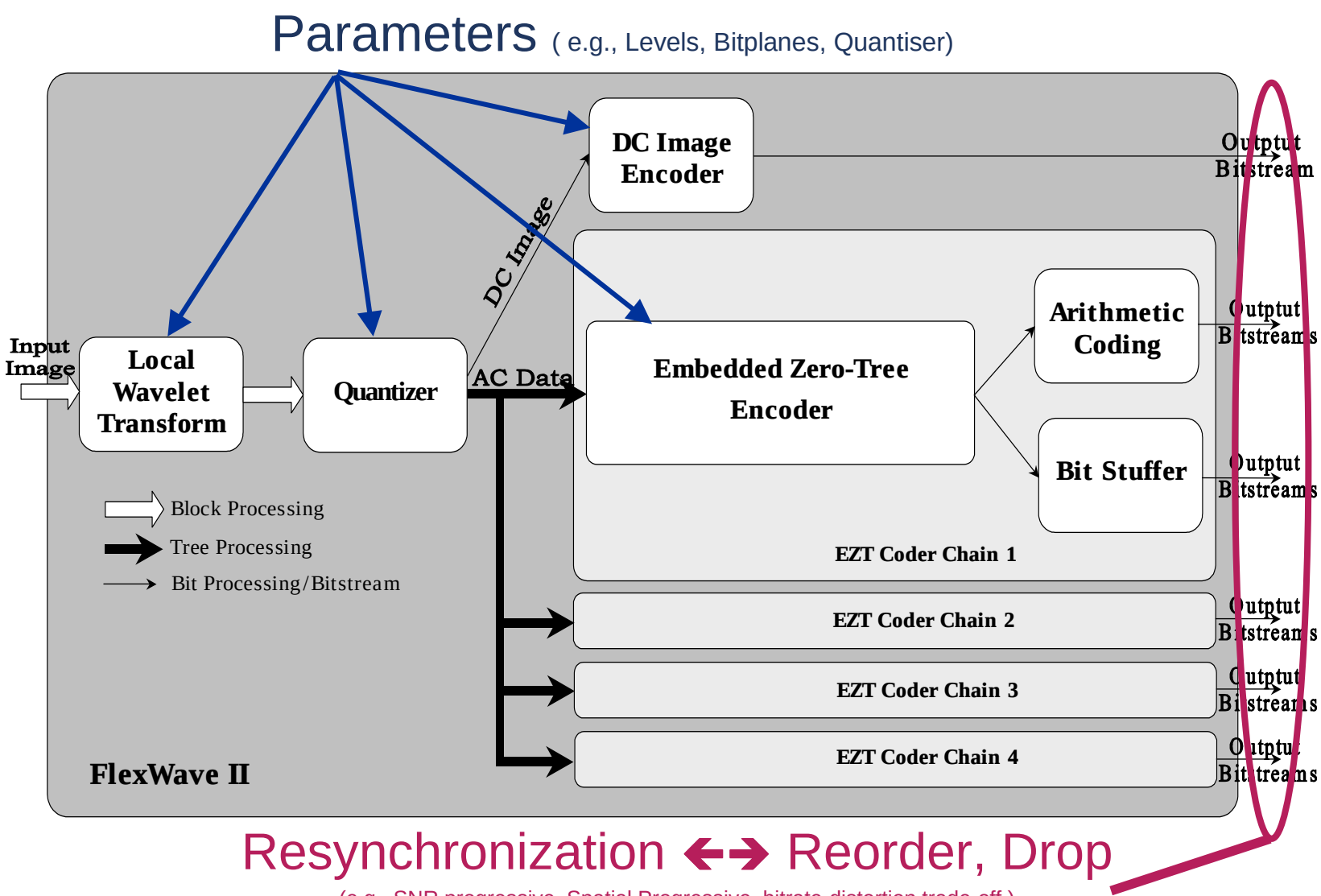
- Problem: traditional solutions often sacrifice wavelet functionality to reduce implementation complexity
  - E.g., introduce tiling to reduce memory requirements

➔ FlexWave-II solution

- Wavelet processor engine for maximal flexibility
- IMEC's Local Wavelet Transform (LWT)
  - algorithmically equivalent (i.e. no tiling)
  - block-based computation

1k x 1k	Classical	RPA	LWT
Memory Size	1 M	327 k	281 k
Memory Accesses/pixel	2.67	11.3	3.07

FlexWave-II Architecture



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LWT Architecture

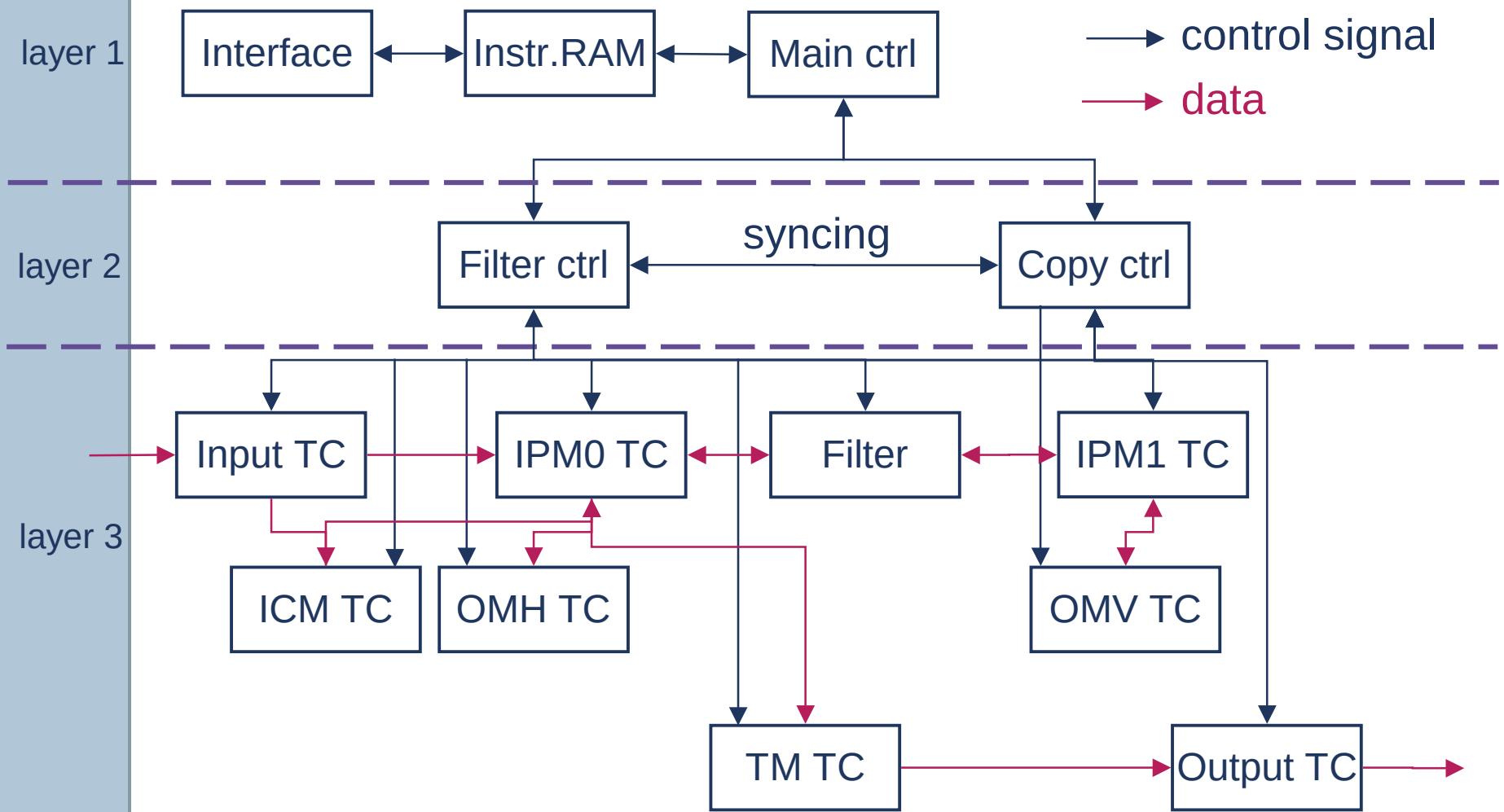
- Two groups of operations
  - Filtering operations
  - Copy operations between small memories
- Parallelism for high efficiency and throughput
  - Between the filter and copy operations
  - Between the different copy operations

hierarchical structure of several controllers

LWT:

a superscalar, instruction-based custom processor

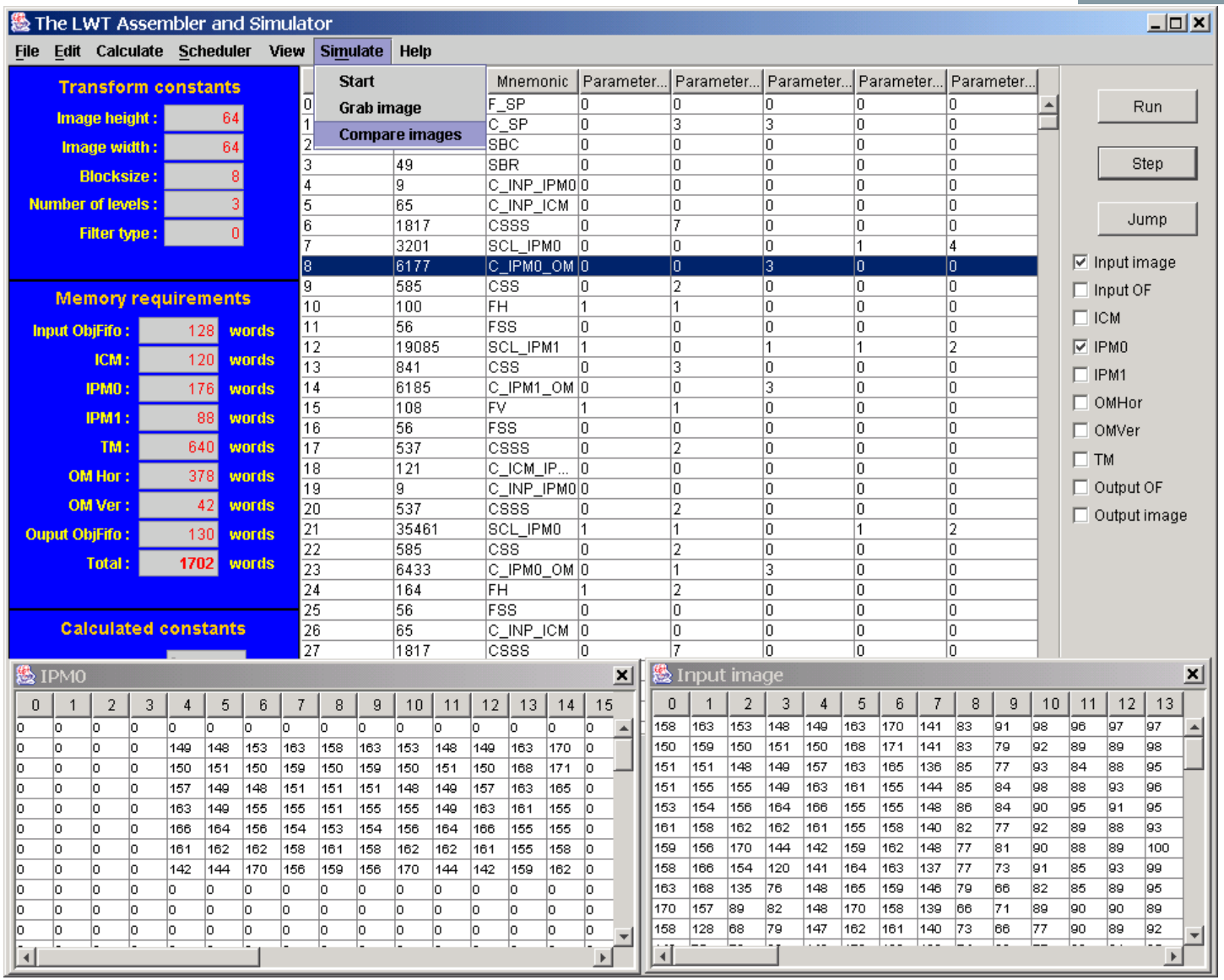
LWT: Superscalar Hierarchical Controller Structure



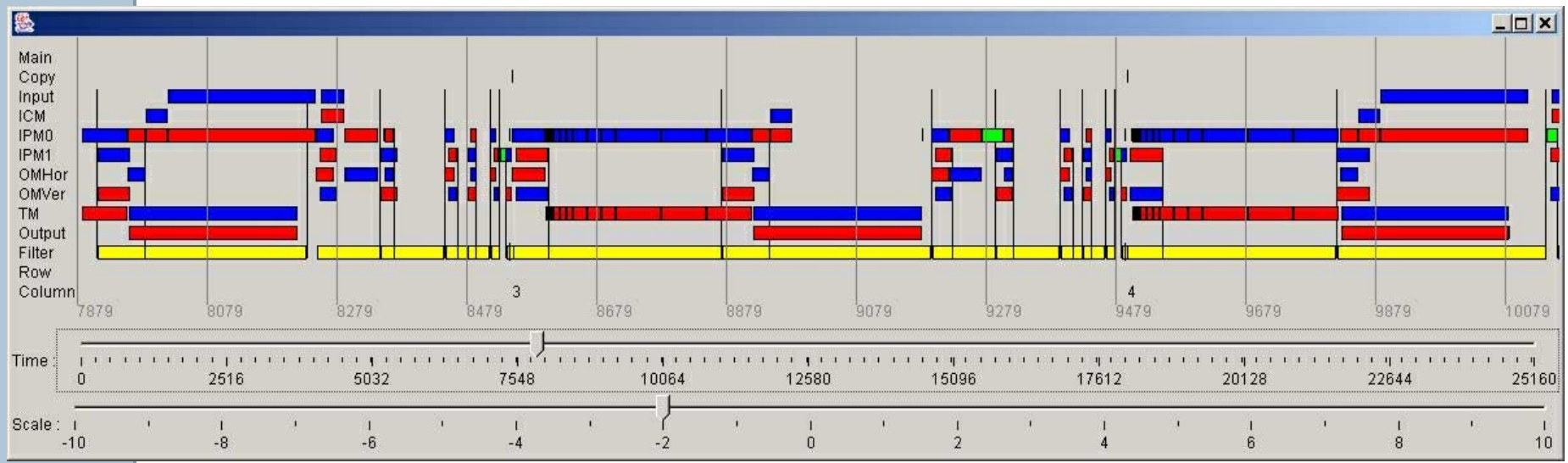
LWT Processing Based on Sequence of Instructions

- Specific instruction set
- Possibility to program specific tasks
  - Region of Interest
  - View-dependent texture coding
  - Standard-depending coding
  - Push-broom processing

Software Support Eases Schedule Creation, Debugging & Synchronisation Check



High-Level Simulator



- Avoids (slow) VHDL simulations to test sequence
- Visually intuitive
  - Source/destination/filter/symmetrical copy operations
  - Syncing from/to filter/copy controller
  - Only relevant information
- Facilitates debugging/optimizing of sequence

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Consultative Committee for Space Data Systems (CCSDS)

- SLS Data Compression panel
- FlexWave-II demonstrated the feasibility of low-complexity wavelet encoding
- LWT compatible with NASA's Bit Plane Encoder (BPE)

➔ FlexWave-II played an important role in the acceptance by CCSDS of wavelet-based schemes, in line with ESA requirements

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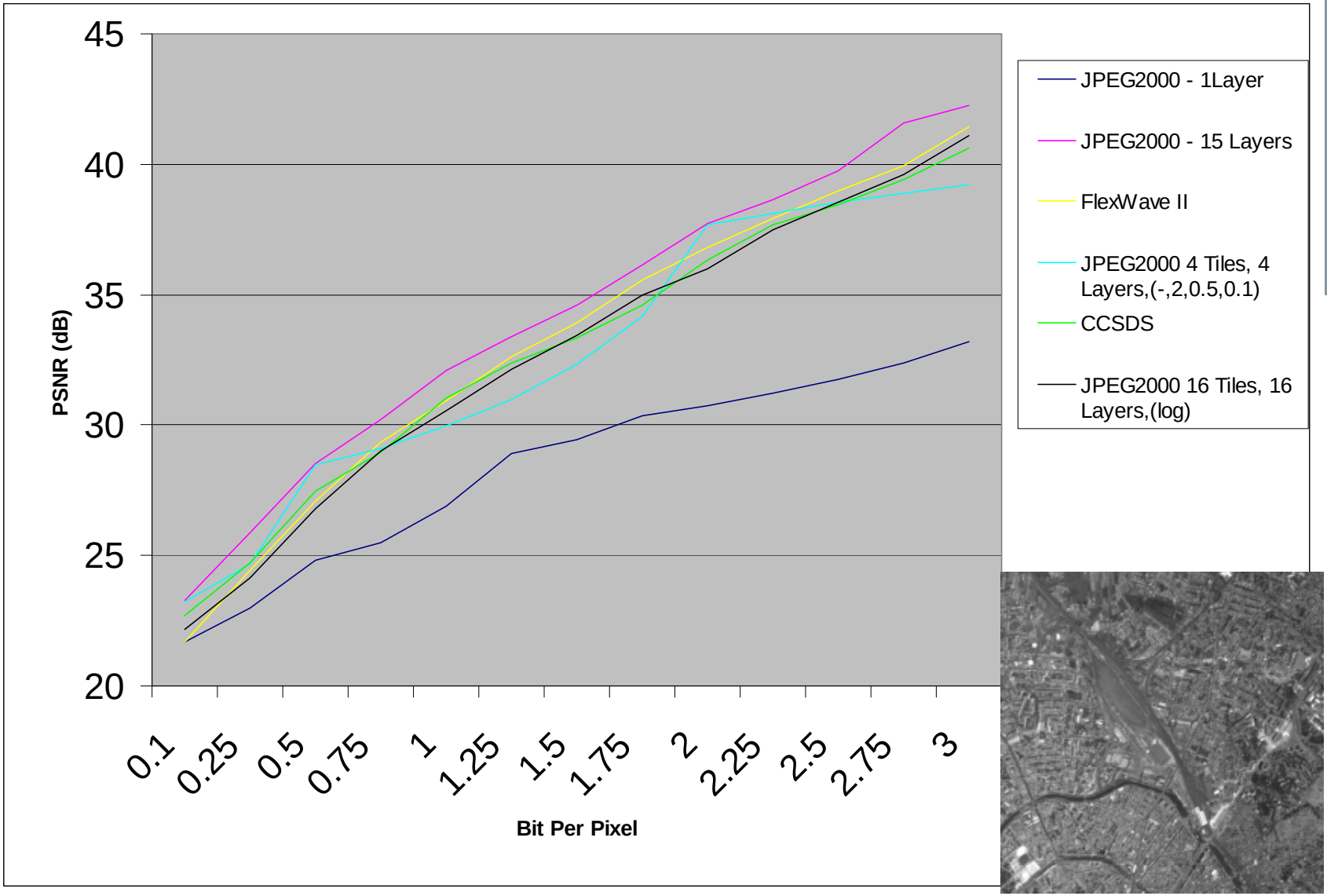
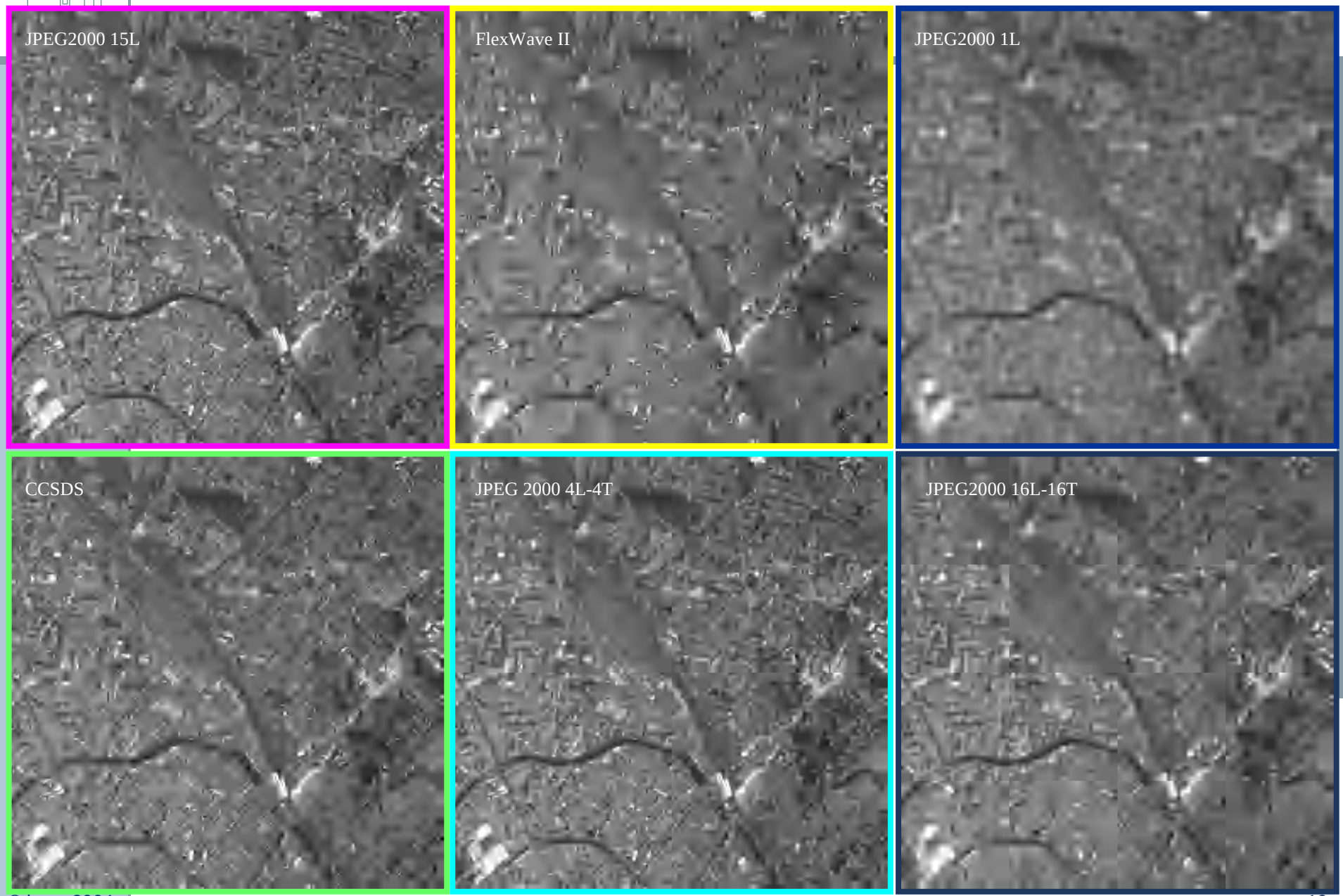
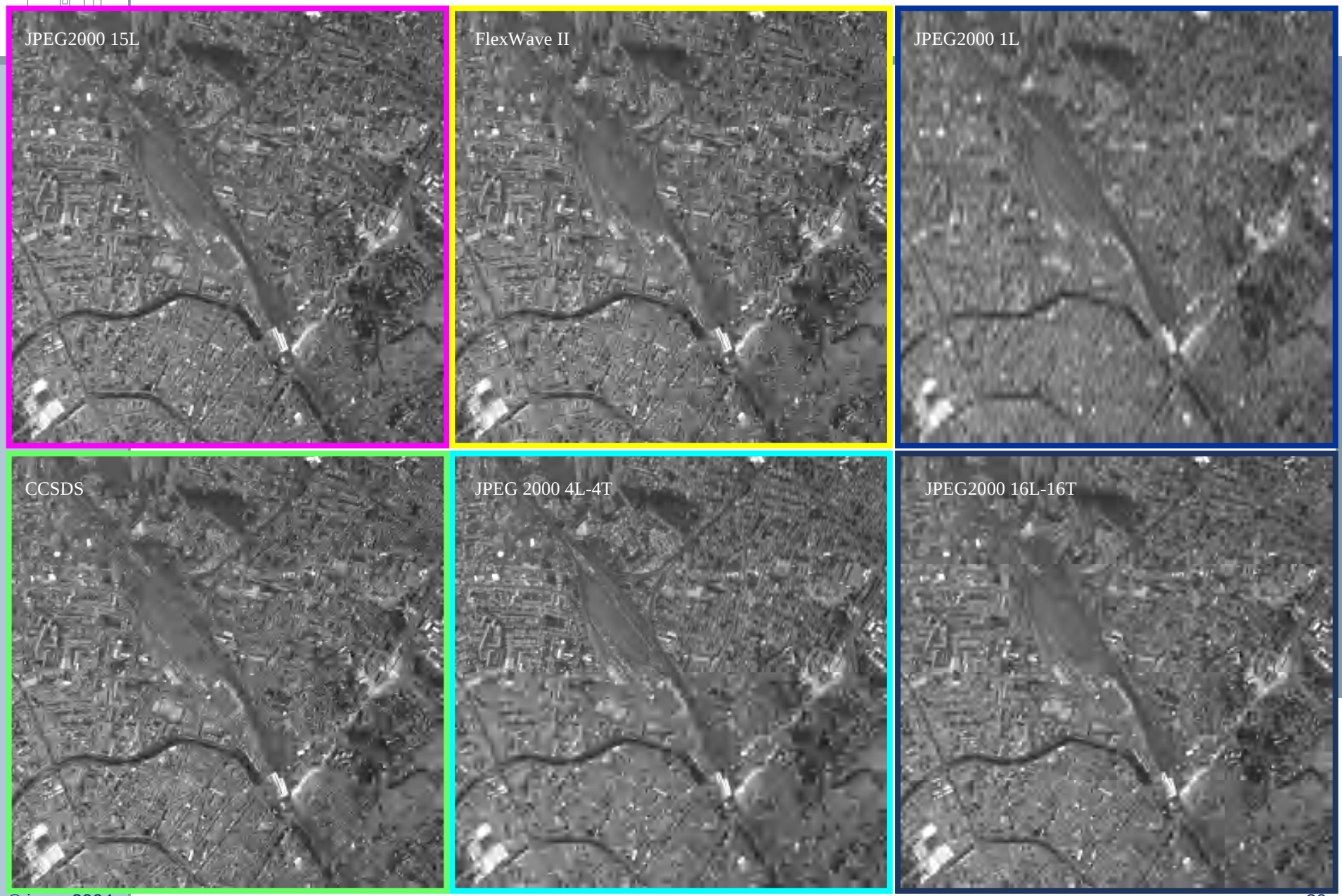
FlexWave-II Compression Performance



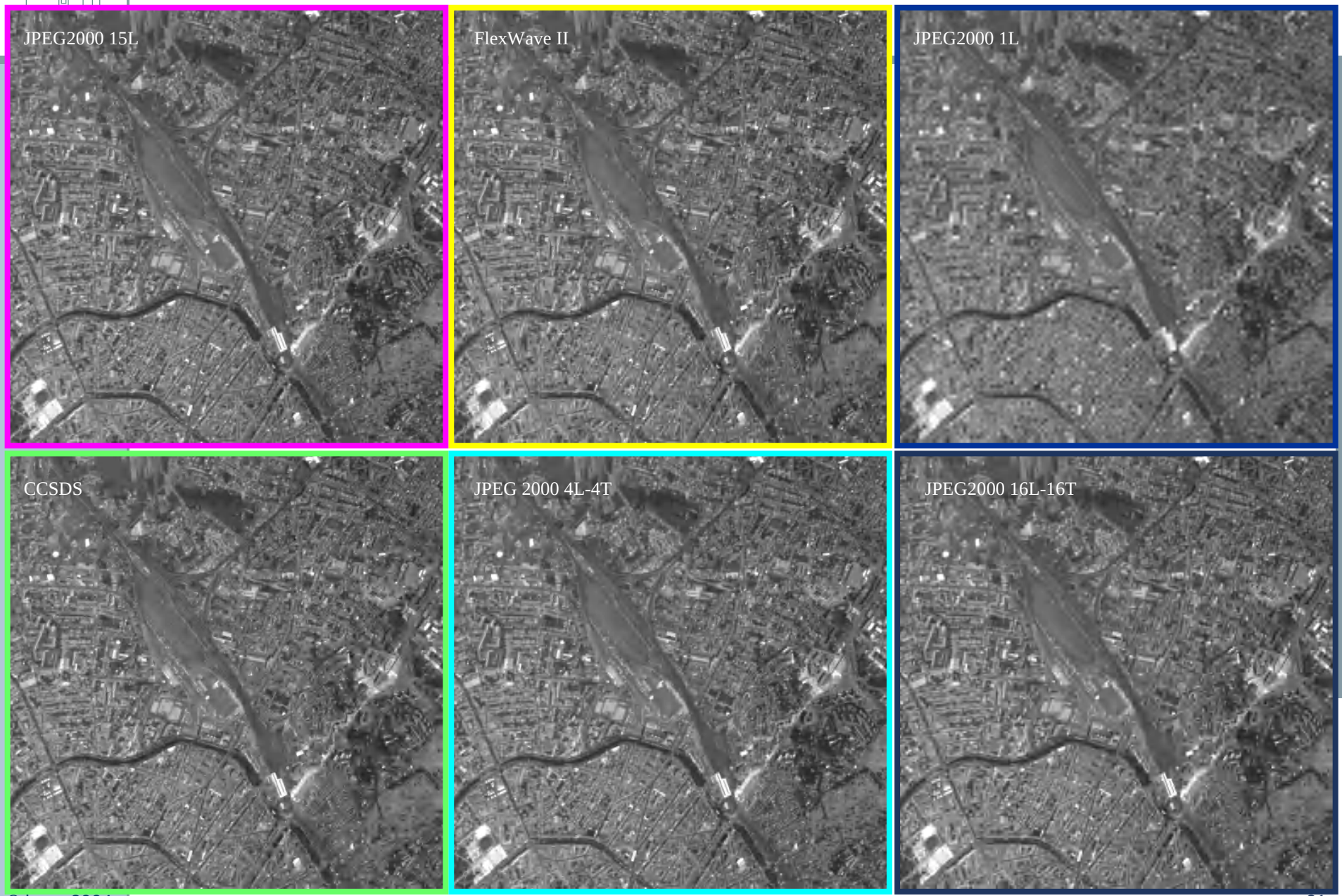
Visual Performance Results @ 0.1 bpp



Visual Performance Results @ 0.25 bpp



Visual Performance Results @ 0.5 bpp



LWT FPGA implementation report on Xilinx Virtex2 XC2V6000

```
Target Device  : x2v6000
Target Package : bf957
Target Speed   : -6
Design Summary
--------------
   Number of Slices:                3,626 out of  33,792   10%
   Number of Slices containing
      unrelated logic:                  0 out of   3,626    0%
   Number of Slice Flip Flops:      2,293 out of  67,584    3%
   Total Number 4 input LUTs:       6,176 out of  67,584    9%
      Number used as LUTs:                        5,730
      Number used as a route-thru:                  446
   Number of bonded IOBs:             138 out of     684   20%
      IOB Flip Flops:                             124
   Number of Block RAMs:              128 out of     144   88%
   Number of MULT18X18s:               21 out of     144   14%
   Number of GCLKs:                     2 out of      16   12%
   Number of DCMs:                      2 out of      12   16%
Total equivalent gate count for design:  8,551,309
Additional JTAG gate count for IOBs:  6,624
--------------
Max. Clock Frequency                                      50 MHz
```

LWT Processing Performance Results (FPGA)

Image	5-3 Filter					9-7 Filter				
	Block Size	Levels	Memory (words)	Clk/Pix	Frm/Sec	Block Size	Levels	Memory (words)	Clk/Pix	Frm/Sec
256×256	32×32	5	19,877	4.21	181	32×32	5	42,673	5.81	131
		4		4.19	182		4		5.82	131
		3		4.08	187		3		5.71	134
		2		3.82	200		2		5.35	143
	16×16	4	8,453	4.30	177	16×16	4	20,497	6.27	122
		3		4.26	179		3		6.13	124
		2		3.84	199		2		5.66	135
	8×8	3	4,397	5.31	144	8×8	3	11,353	5.81	131
		2		4.88	156		2		5.82	131
512×512	32×32	5	29,813	3.66	52	32×32	5	71,489	4.80	40
		4		3.65	52		4		4.79	40
		3		3.54	54		3		4.68	41
		2		3.32	57		2		4.37	44
	16×16	4	14,245	3.99	48	16×16	4	36,913	5.65	34
		3		3.95	48		3		5.49	35
		2		3.56	54		2		5.06	38
	8×8	3	8,045	5.13	37	8×8	3	21,401	8.17	23
		2		4.71	40		2		7.21	26
1024×1024	32×32	5	49,685	3.41	14	32×32	5	129,121	4.33	11
		4		3.40	14		4		4.30	11
		3		3.30	14		3		4.20	11
		2		3.09	15		2		3.92	12
	16×16	4	25,829	3.85	12	16×16	4	69,745	5.36	9
		3		3.81	13		3		5.20	9
		2		3.43	14		2		4.78	10
	8×8	3	15,341	5.05	9	8×8	3	41,497	7.95	6
		2		4.62	10		2		6.98	7

FlexWave-II FPGA implementation report on Xilinx Virtex2 XC2V6000

```
Target Device  : x2v6000
Target Package : bf957
Target Speed   : -6

Design Summary
--------------
   Number of Slices:                14,571 out of  33,792   43%
   Number of Slices containing
      unrelated logic:                   0 out of  14,571    0%
   Number of Slice Flip Flops:      11,957 out of  67,584   17%
   Total Number 4 input LUTs:       19,987 out of  67,584   29%
      Number used as LUTs:                      17,396
      Number used as a route-thru:                 725
      Number used for 32x1 RAMs:                 1,840
      (Two LUTs used per 32x1 RAM)
      Number used as 16x1 ROMs:                     26
   Number of bonded IOBs:             105 out of     684   15%
      IOB Flip Flops:                                10
   Number of Tbufs:                    40 out of  16,896    1%
   Number of Block RAMs:              144 out of     144  100%
   Number of MULT18X18s:               30 out of     144   20%
   Number of GCLKs:                     2 out of      16   12%
   Number of RPM macros:           28
Additional JTAG gate count for IOBs:  5,040
--------------
Max. Clock Frequency                                      41 MHz
```

Resources	LWT	LWT part of FlexWave II	FlexWave II
Slices	3,626	24.8 %	14,571
Memory Blocks	128	88.8 %	144
Multipliers	21	70.0 %	30
Clk/Pix (1k×1k, 32×32, 5)	3.41	64.7 %	5.27

FlexWave-II processing performance for the 5/3 wavelet filter (FPGA)

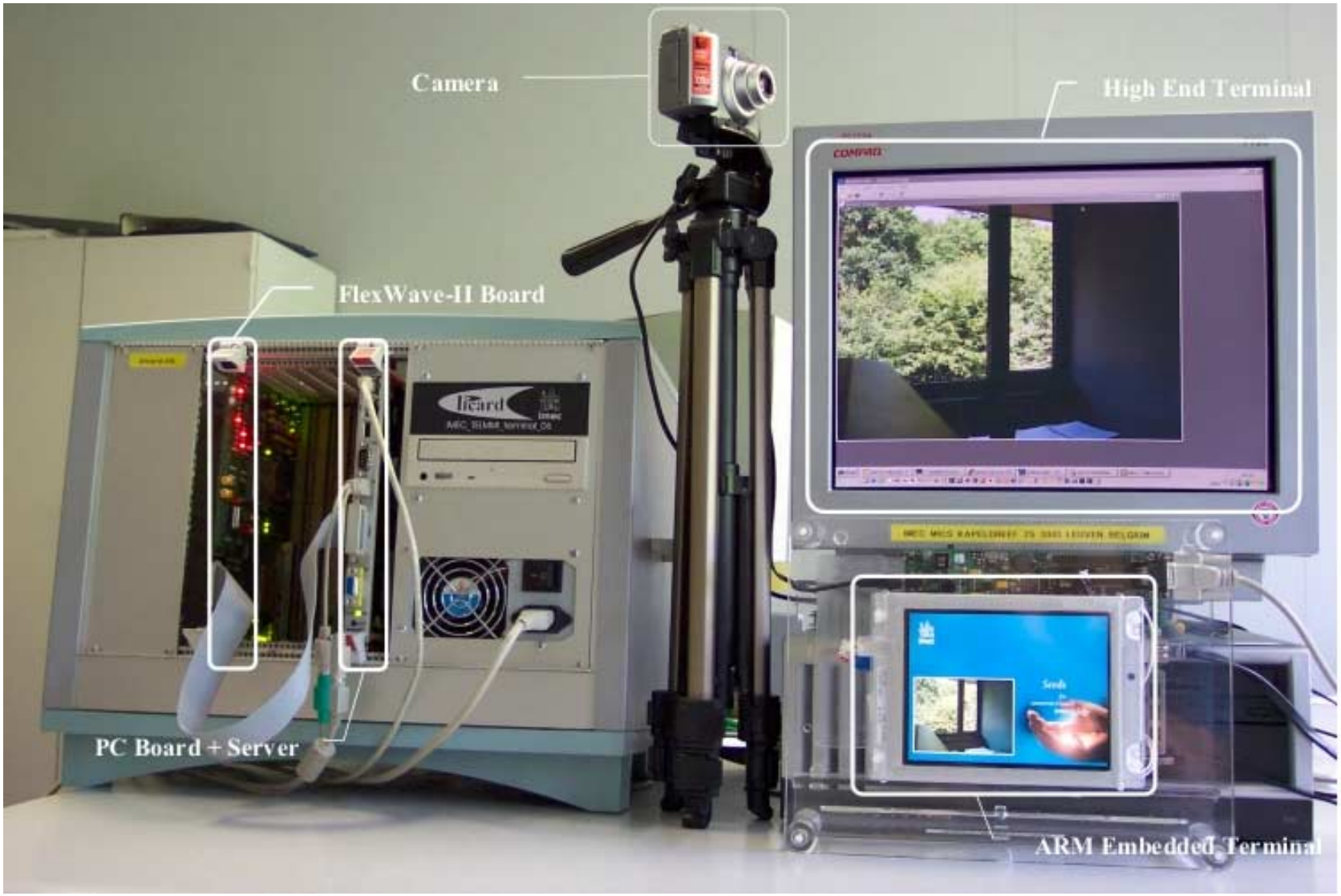
Image Size	BlockSize	Nr of levels	Clock Cycles/Pix
1024×1024	32	5	5.27
		4	5.27
		3	5.27
	16	4	5.66
		3	5.66
	8	3	7.40
512×512	32	5	5.42
		4	5.42
		3	5.42
	16	4	5.74
		3	5.74
	8	3	7.45
256×256	32	5	5.81
		4	5.82
		3	5.80
	16	4	5.92
		3	5.93
	8	3	7.56

FlexWave-II Estimated Synthesis and Timing Results for 0.18μm UMC Technology

Block	Gate Count	Percentage
LWT	51070	29.2%
Quantisation unit	6733	3.9%
CoderBlock 0	26890	15.4%
CoderBlock 1	26769	15.3%
CoderBlock 2	26769	15.3%
CoderBlock 3	26769	15.3%
DC coder	7508	4.3%
Glue	2266	1.3%
Total	174776	100%

Operating conditions	RAM Delay	Critical path	Clock frequency
Best Case	3 ns	8.84 ns	113 MHz
Typical Case	4 ns	11.91 ns	84 MHz
Worst Case	5 ns	19.89 ns	50 MHz

FlexWave-II Scalability Demonstrator Photo



Conclusions

- FlexWave-II: combining compression performance, flexibility and low implementation complexity
- Programmable/tunable for different usage contexts
- Key component: LWT enabling block-based processing without image tiling
- Impacted CCDSS standardization
- Design kit and FPGA prototype

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