Radiation Hardening By Design

Low Power, Radiation Tolerant Microelectronics Design Techniques

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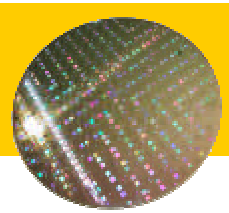
ALCATEL SPACE

The foundry problem...



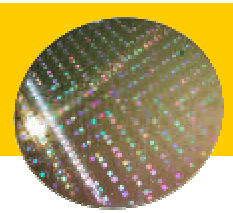
Rad-Hard foundries are leaving the marketplace

- Reduced demand from military customers
- Too small volumes
- Only 1 supplier in Europe left (ATMEL)

Solution: Hardening commercial CMOS technologies

- US independent
- more advanced, deep sub-micron technologies possible
- Higher speed
- Low power
- Low volume/mass
- Low cost
- => A lot of interest from the (European) space community

Design Against Radiation Effects



Using layout techniques to minimize the radiation impact

- Free library for European Space Industry

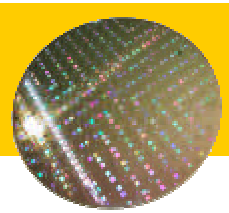
Technology: UMC .18 μm CMOS, 6 metal

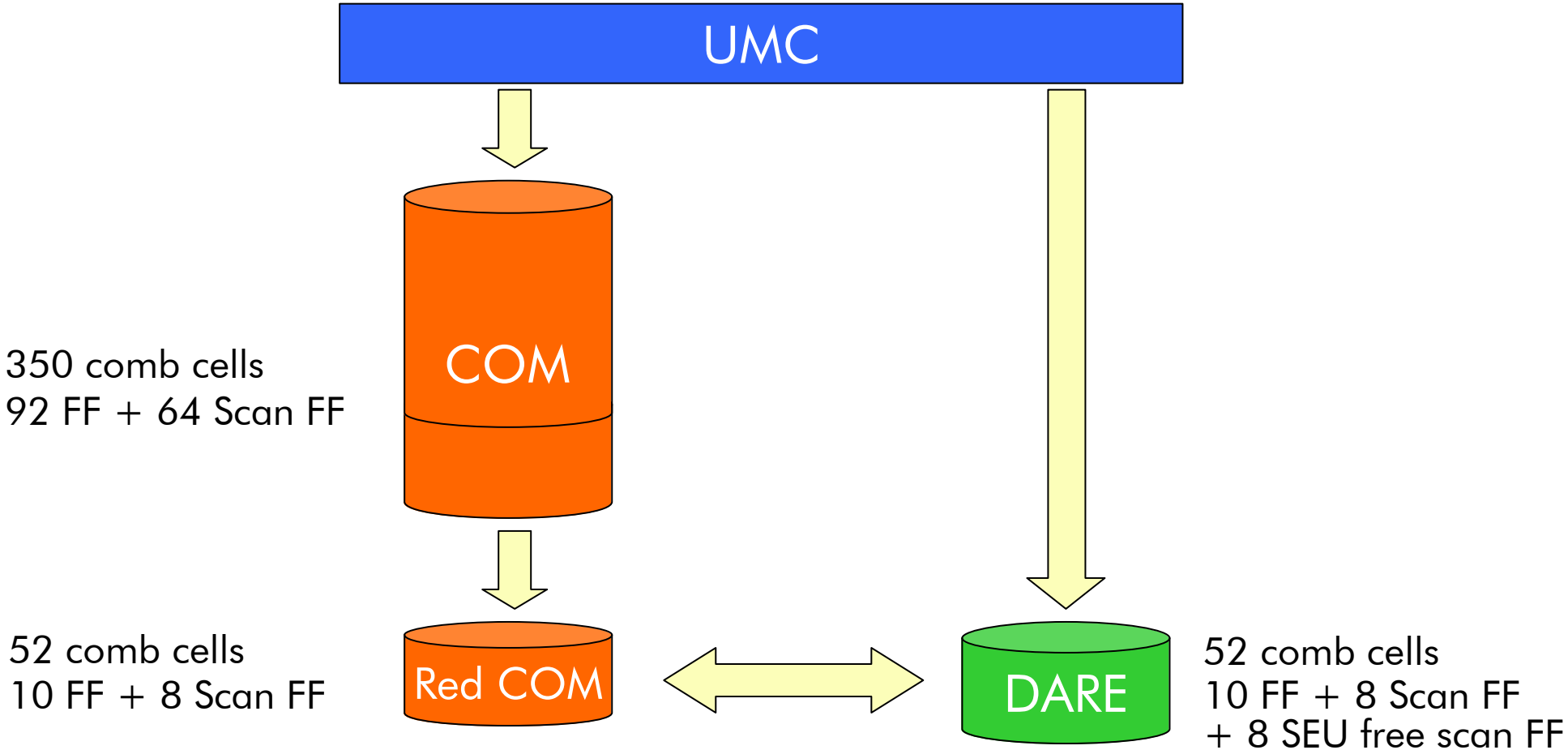
- Available through EUROPRACTICE (MPW shuttle every month)
- Very smooth co-operation between IMEC and UMC
- Stable commercial technology

DARE library includes

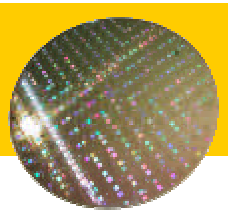
- 78 Core Cells
  - → Scan equivalents for all flip-flops
  - → SEU hardened flip-flops included (HIT cell)
- 23 In-line IO Pad Cells (+ P/G + Corners + Fillers)
  - → 3.3V & 2.5V I/O's
  - → Includes LVDS
  - → Cold spare & 5V tolerance additions are being investigated
- Single Port SRAM Compiler
- PLL

Libraries used





Available EDA tool views



Liberty (.lib) file – for 6 process corners using accurate table lookup timing model

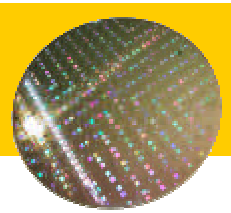
- Synopsys Design Compiler / PrimeTime
- Synplicity Synplify ASIC
- …

Verilog & VITAL simulation Models

Avant! Apollo layout and timing views

Any LVS tool using CDL input

Project Flow



DARE design - Imec

Telecom Chip Design – Alcatel Space

Parasitic information for CWL model generation and ECO's

Test Chip design - Imec

Place & Route + checks - Imec

MPW Manufacturing - UMC

MPW Manufacturing - UMC

EUROPRACTICE

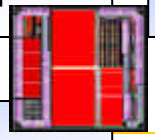
Packaging - EdgeTek

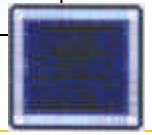
Packaging - HCM

Testing – Microtest

Radiation test - Alcatel Space

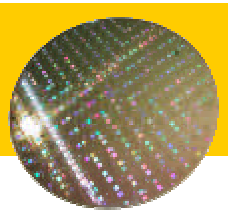
Functional & Radiation test - Alcatel Space





funtional test – Imec

Actual chip sizes



Commercial Library

- Pad Limited
- Chip size : 6.540 x 6.540 mm^2
- Core size: 4.039 x 5.519 mm^2

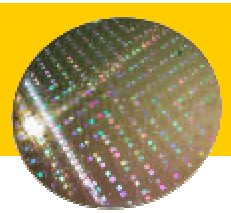
Commercial Library reduced sub-set

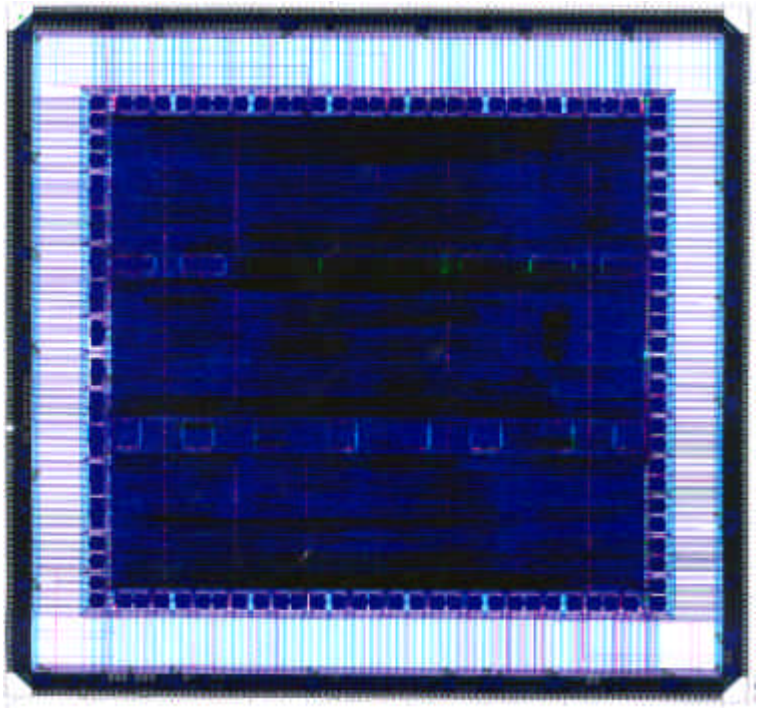
- Same

DARE

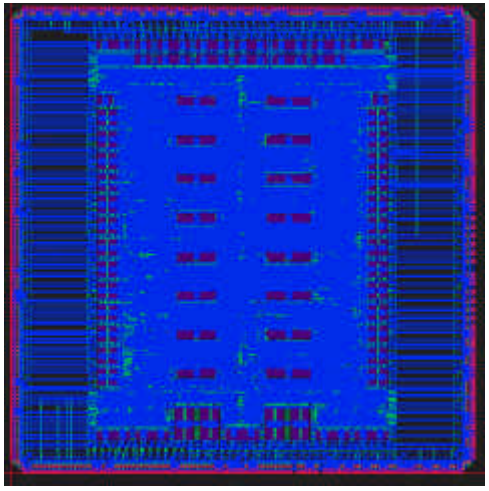
- Pad Limited, in-line pads
- Chip size : 9.418 x 9.418 mm^2
- Core size : 7.046 x 7.344 mm^2
- => 2 times bigger

Layouts

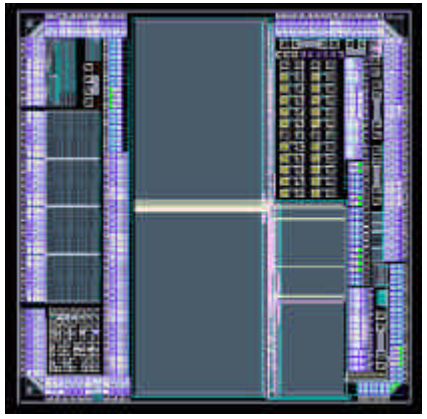




DARE DROM

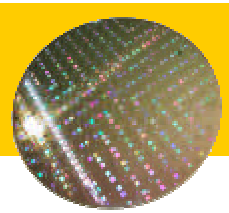


COM DROM
(= Reduced COM)



DIE HARD

What if Staggered IO?



Commercial In-line IO

- 6540 x 6540 = 42.77mm^2

Commercial Staggered IO

- 6360 x 4860 = 30.91mm^2

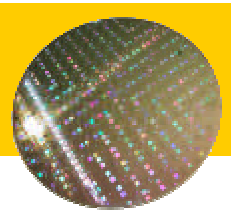
DARE In-Line IO

- 9418 X 9418 = 88.7mm^2

DARE Staggered IO (estimated)

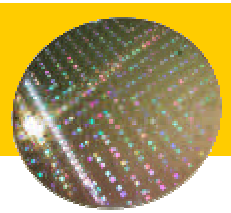
- 8200 x 8474 = 69.48 mm^2
- => 2.25 times bigger

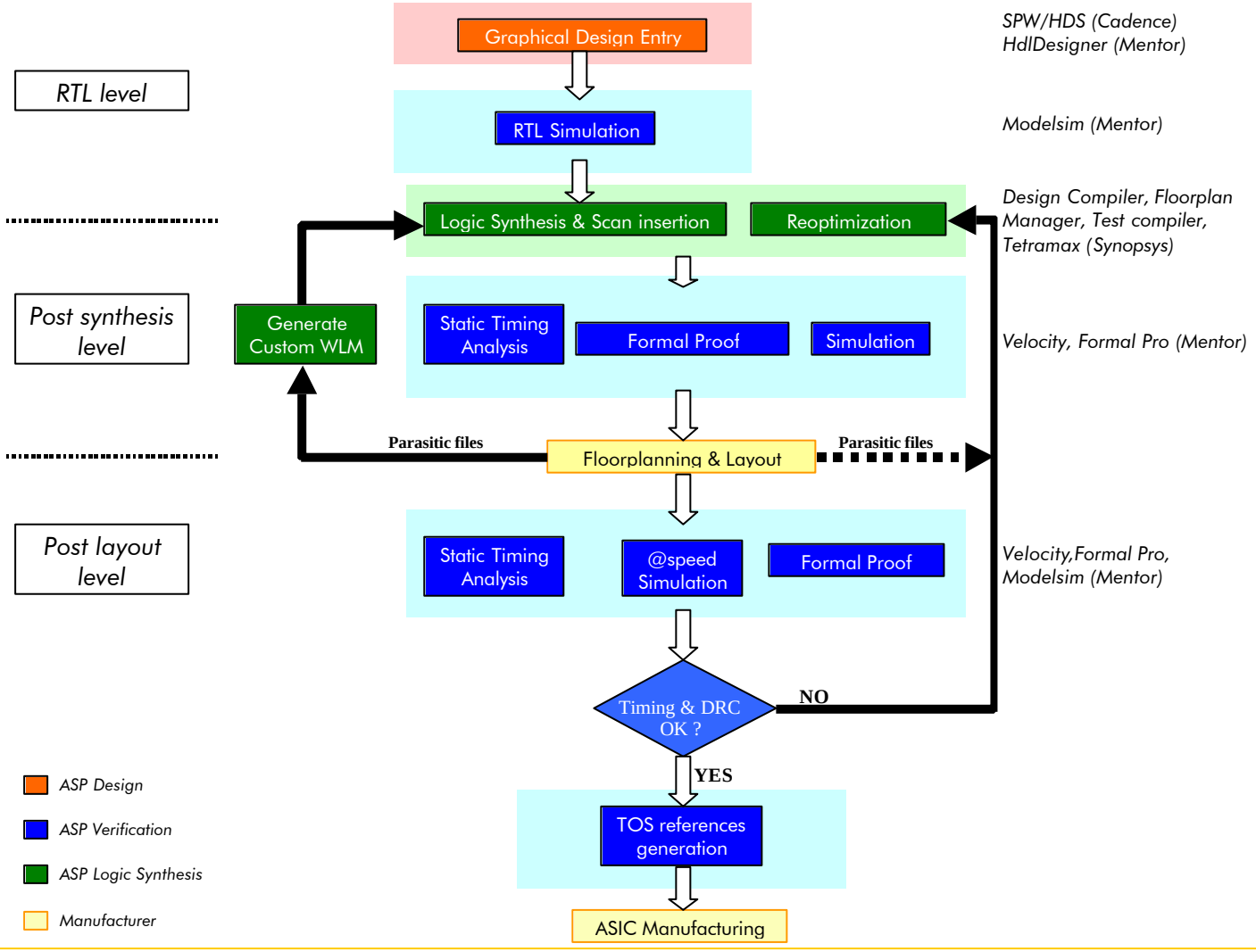
DROM ASIC



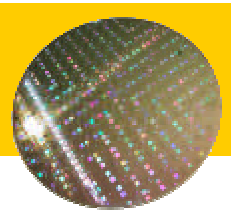
- DROM : Digital Signal Processing ASIC for Bent Pipe Processor running at 105 MHz
- 114 SRAMs = 84 kbits
  - 104 SRAMS used at 26.25 MHz max
  - 10 SRAMS used at 52.5 MHz max (~ TPRAM functionality)
- LVDS I/O
- Total number of equivalent gates 1.3 MGates
- Total number of bond pads : 403 pads
- Package : CPGA 476

DROM design flow



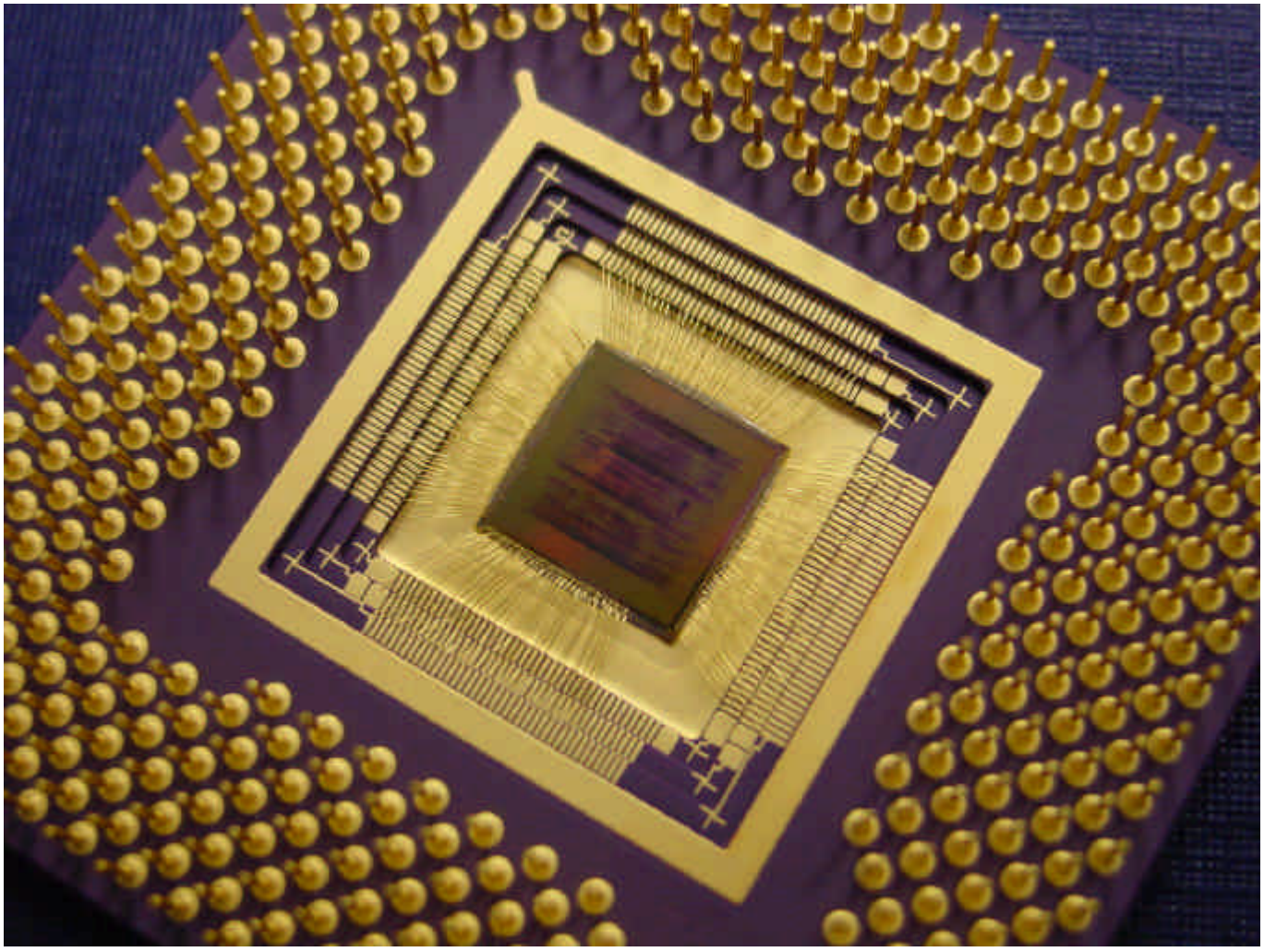


Timing closure after layout

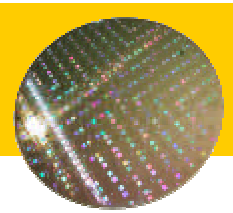


- Example on a critical path in 105MHz domain
  - with CWLM : td = 5.24 ns
  - After 3 layout iterations : td = 6.14 ns (+17%)
  - important to take some frequency margin during the architecture phase (~15%)
- Hold violations have to be fixed
  - at least after first layout
  - convergence problem after layout of the logic inserted to correct violations

DROM



Library comparison



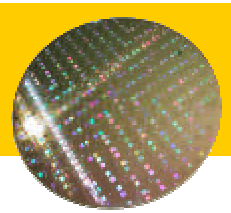
Comparison on operators/ DROM

- area
  - → Reduced COM = COM
  - → DARE = 3 x Reduced COM
  - → DARE/MH1RT : units problem (SOG / Standard cell)
- speed (delay)
  - → Reduced COM = COM
  - → DARE # Red COM
  - → DARE 2 times faster than MH1RT

Power consumption

- COM 0.18 μm: 50 nW/gate/MHz
- DARE 0.18 μm: 180 nW/gate/MHz
- MH1RT 0.35 μm: 400 nW/gate/MHz

Single Event Effect (SEE) Tests



Two types of test have been performed :

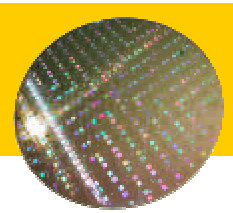
- **Heavy Ions Test** : The European Heavy Ions Facility of Louvain La Neuve has been used for this evaluation. Ions used in the course of the present evaluation :

Ion Specy	**Energy** (MeV)	**LET** (MeV/(mg/cm²))	**Range** μm
15-N	62	2.97	64
20-Ne	78	5. 85	45
40-Ar	150	14. 1	42
84-Kr	316	34	43
132-Xe	459	55. 9	43

- **Proton Test** : The CPO (Centre Protonthérapie d'Orsay) Facility of the University of Orsay (France) has been used for this evaluation.

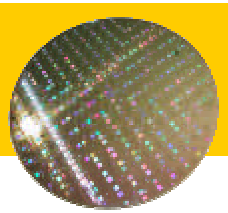
  Energy : 150 MeV, 100 MeV, 70 MeV, 50 MeV and 30 MeV.

Single Event Effect (SEE) Tests



- Selftest Configuration (Autotest) : specific test to easily control the nominal functionality of the ASIC
  - Autotest 1 with a 45.8 MHz carrier waveform
  - Autotest 2 with a temporal ramp
- Bist Configuration : to evaluate SRAM cells
- Scan Configuration : to evaluate D flip-flops (implemented physically) placed in several regions on the die
  - SCAN 0 is for « all 0 » initial pattern
  - SCAN 1 for « all 1 » initial pattern.

Main SEE Results

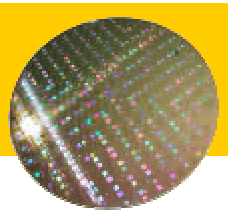


- No Single Event Latchup (SEL)
- No Single Event Hard Errors (SHE): Stuck bits
- No Single Event Functional Interrupt (SEFI)
- Only Single Event Upset (SEU) observed on basic cells : SRAM, DFF

=> Impact on DROM functionality is a transient perturbation but the ASIC recovers after few clock cycles

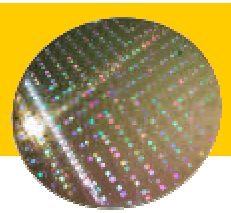
NB : More detailed evaluation of 0.18 μm CMOS basic structures will be performed on the Test Chip March 2004

Main SEE Results



SCAN 1	$t_{(HI\ and\ p+)} = 12.0\ 10^{-8}$ SEU/cell.day (GEO)
SCAN 2	$t_{(HI\ and\ p+)} = 7.7\ 10^{-8}$ SEU/cell.day (GEO)
BIST	$t_{(HI\ and\ p+)} = 11.0\ 10^{-8}$ SEU/cell.day (GEO)
Autotest 1	$t_{(HI\ and\ p+)} = 5.6\ 10^{-2}$ SEU/ASIC.day (GEO)
Autotest 2	$t_{(HI\ and\ p+)} = 7.81\ 10^{-2}$ SEU/ASIC.day (GEO)

Total Ionizing Dose (TID) Tests



- **6 Functional Tests** (Same as the ones used for SEE Tests)
  - Selftest Configuration (Autotest) :
    - → Autotest 1 with a 45.8 MHz carrier waveform
    - → Autotest 2 with a temporal ramp
  - Bist Configuration
  - Scan Configuration : SCAN 0 and SCAN 1
- **Parametric measurements** : Icc (1.8V and 3.3V)
- **Bias during Irradiation**
  - in Autotest Mode
- 10 samples + 1 control
- Irradiation Steps : 0, 50, 70, 100 krad(Si) Low Dose Rate
  200, 500, 700 and 1 Mrad(Si) High Dose Rate
- **Tests initiated - In progress**