ChipSat – a System-on-a-chip for Small Satellite Data Processing and Control Architectural Study and FPGA Implementation

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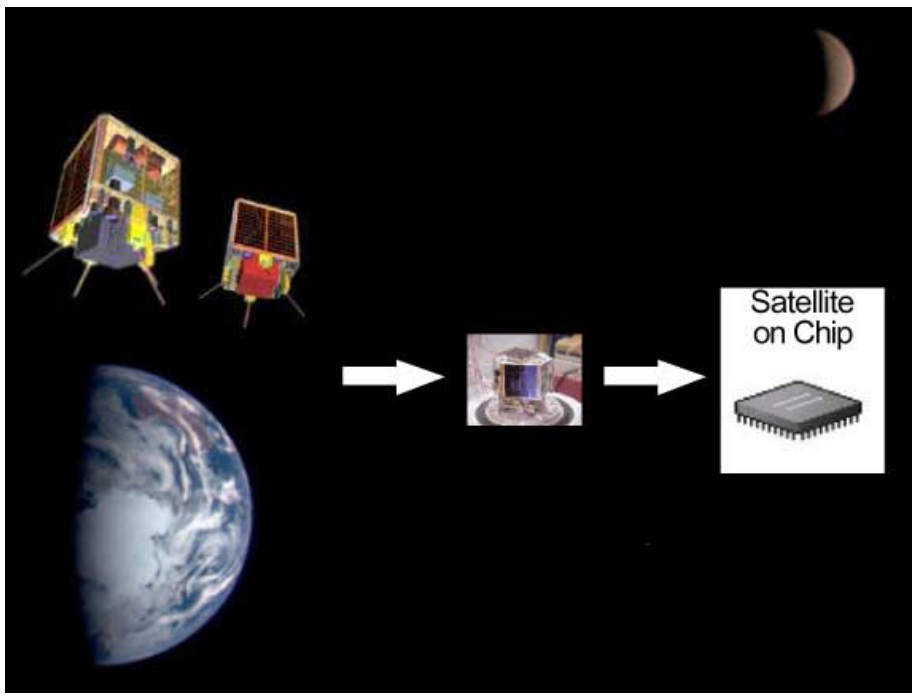
Outline

- Single chip implementation of an on-board command and data handling subsystem for a low-cost small satellite - mixed-mode ASIC.
- SoC design of an on-board computer for a small satellite - based on integration of soft IP cores, compatible with the LEON microprocessor core.
- Downsized on-board computer implementation on a single programmable logic chip and a low-cost CCSDS-based communication system.
- Design and integration of a mathematical floating-point co-processor core, based on the CORDIC algorithm.
- Credit-card size on-board computer system using the SoC.
- DMA controller and DDR SDRAM Controller core for the LEON CPU.
- Aspects of reconfigurability.

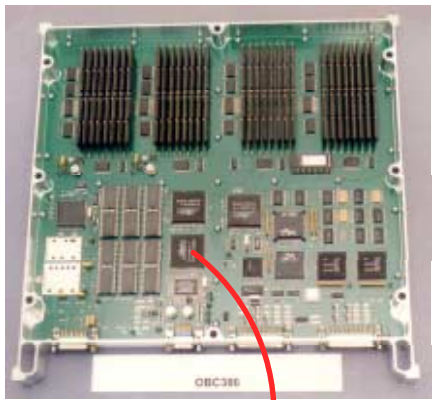
SoC Research at SSC

Long-term

Miniaturisation of the Small Satellite Platform



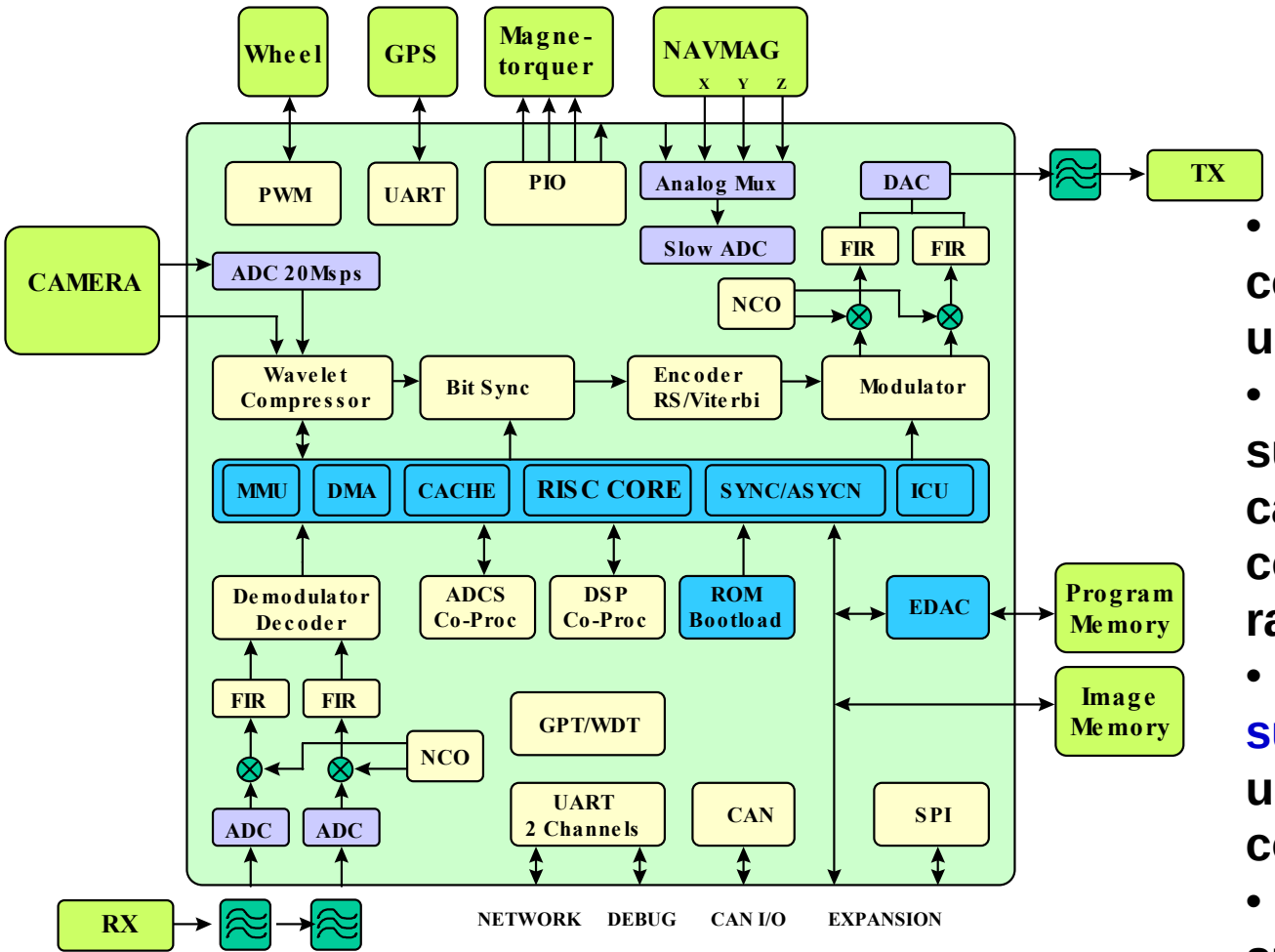
Surrey Satellite Technology's (SSTL) On-Board Computer (OBC)



1) 

2) **Credit-Card Size OBC System**

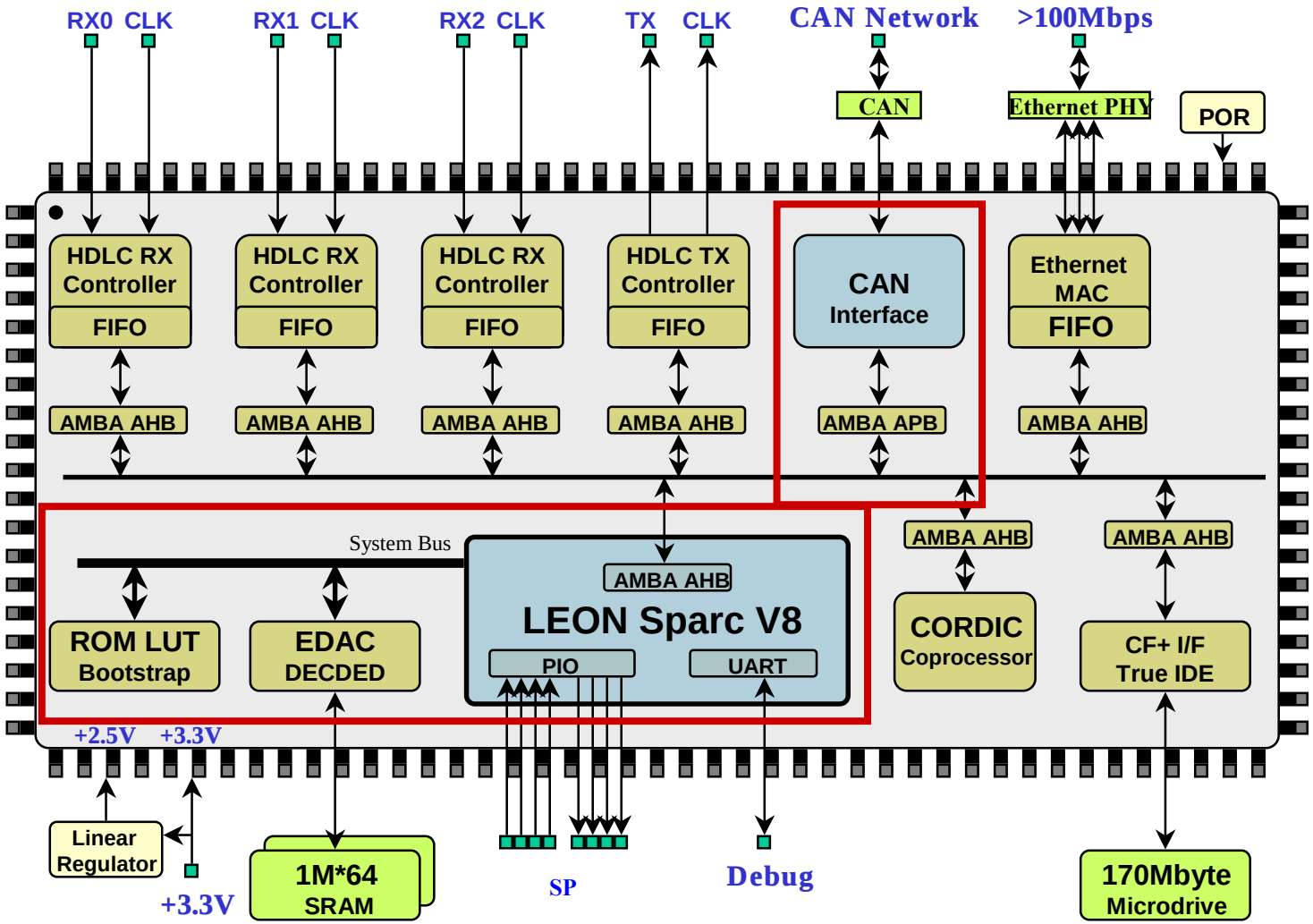
OBCDH Mixed-Mode SoC for EO Small Satellite Missions



Four subsystems:

- a **32-bit RISC processor** core modified for space use;
- an **image handling** subsystem capable of capturing and compressing still or video-rate images;
- a **communication subsystem** for the satellite uplink and downlink connection; and
- a **supporting** peripheral subsystem.

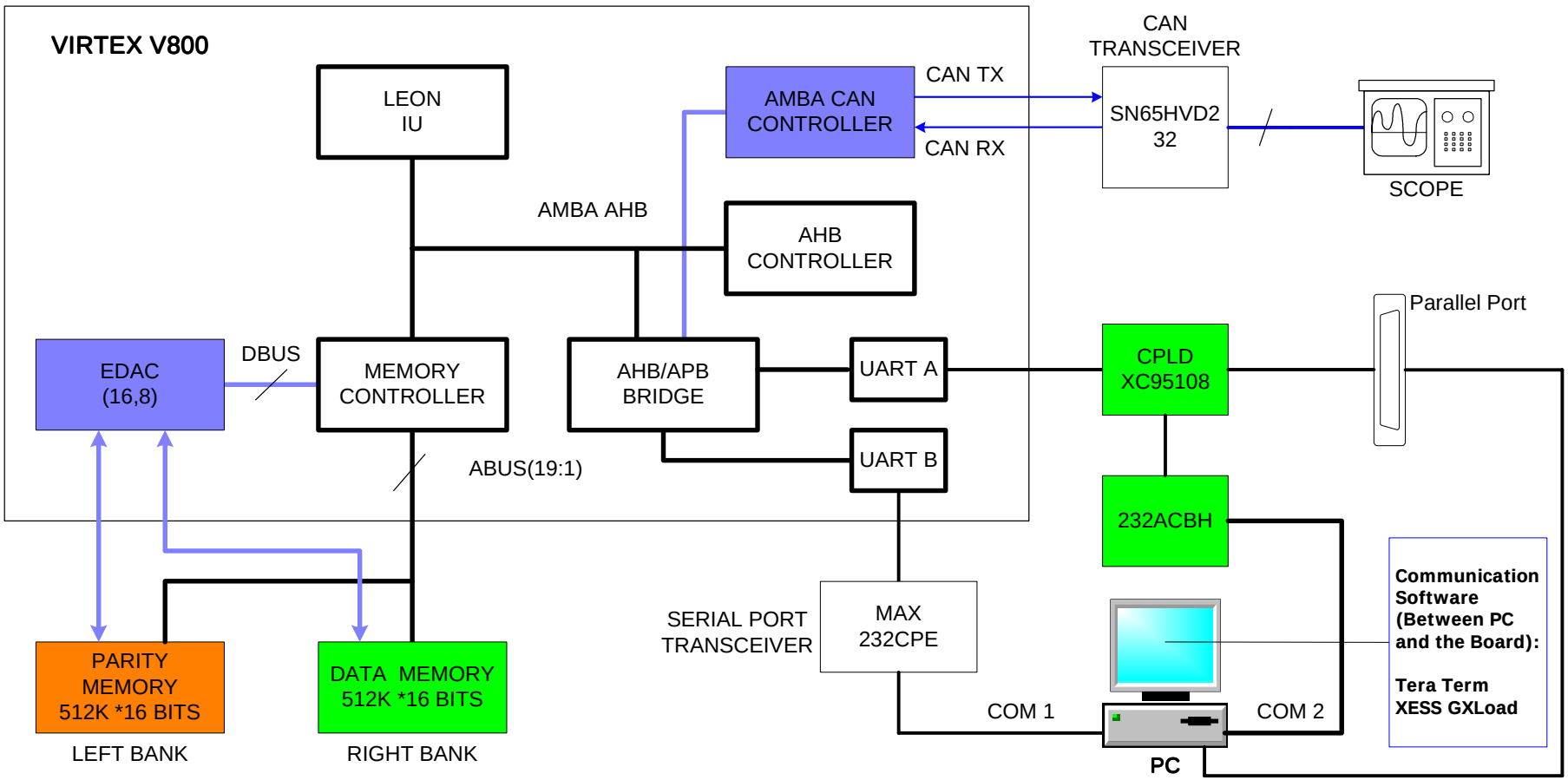
System-on-a-Chip OBC



XILINX Virtex XCV800 FPGA

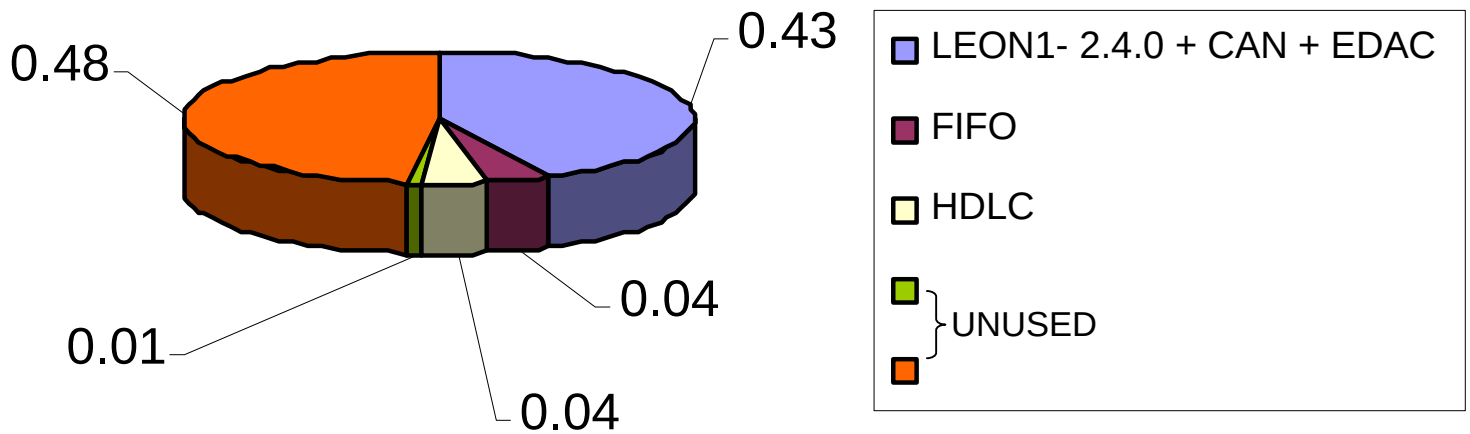
Downsized SoC - FPGA Implementation

Integration of CAN, EDAC and LEON



FPGA Chip Usage

Virtex XCV-800 FPGA

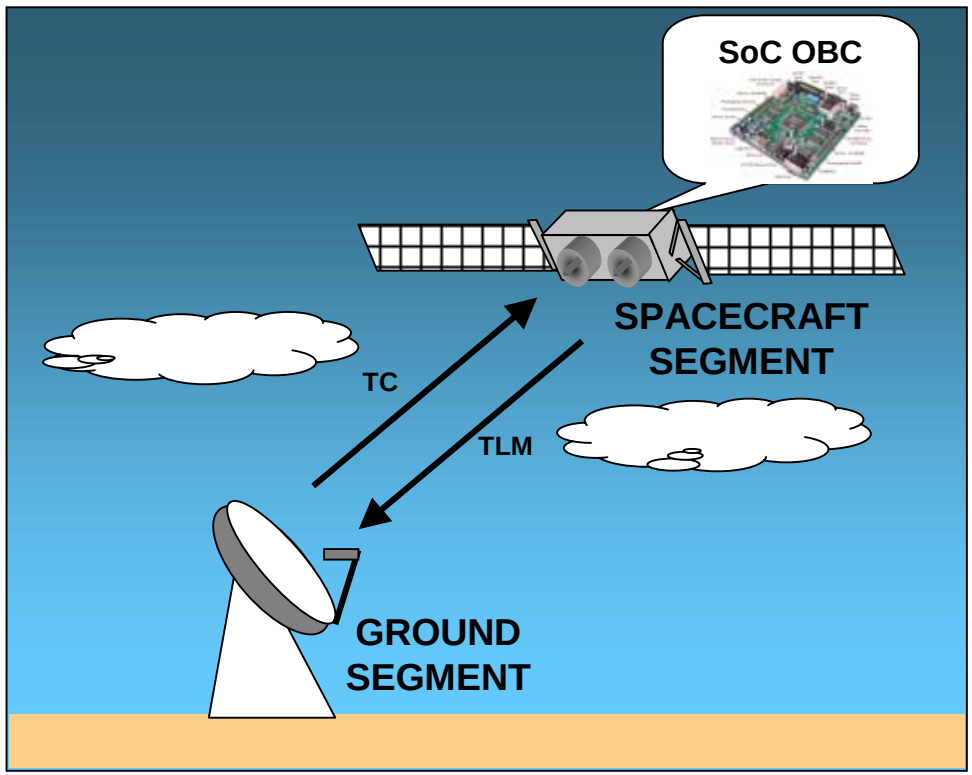


Based on Synthesis Results

- **Synthesis Tool: Synplify 6.0 +**
- **LEON IP core + CAN IP core + EDAC IP core => 43% of XCV800**
- **QPRO XILINX Virtex family of radiation hardened FPGAs:**
  - **qualified for space use**
  - **guaranteed total ionising dose to 100K Rad (si)**
  - **latch-up immune to LET > 125 Mev cm^2/mg @ +125 ^{o}C**

A CCSDS-Based Communication System for a Single-Chip OBC

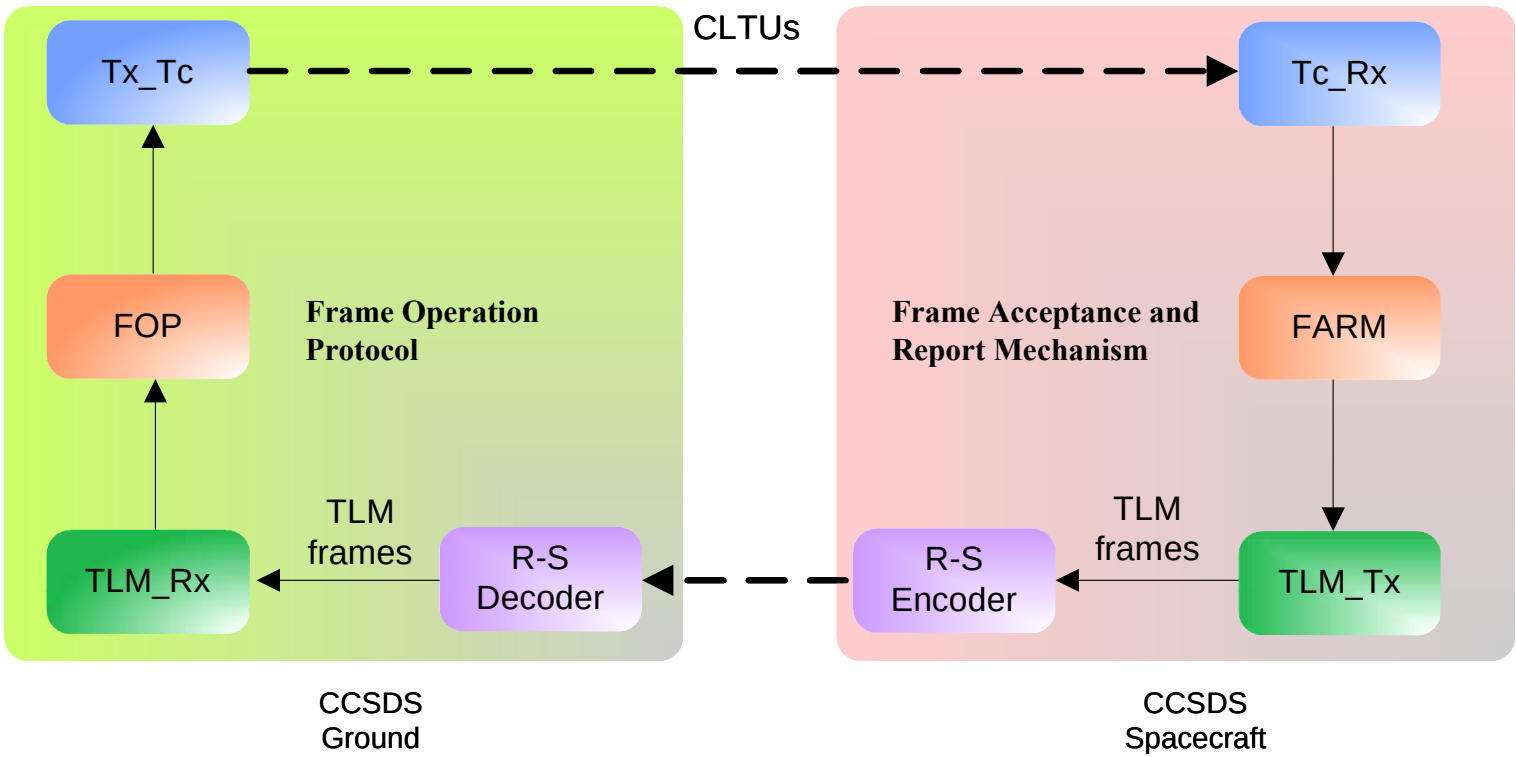
- **Implementation of a *simplified yet* RELIABLE Consultative Committee of Space Data Systems (CCSDS) *TLM & TC* space communication system satisfying the needs of a single chip on-board computer (OBC) of a small satellite.**
- **Simulation of the operation of the software on a single-chip OBC prototype.**



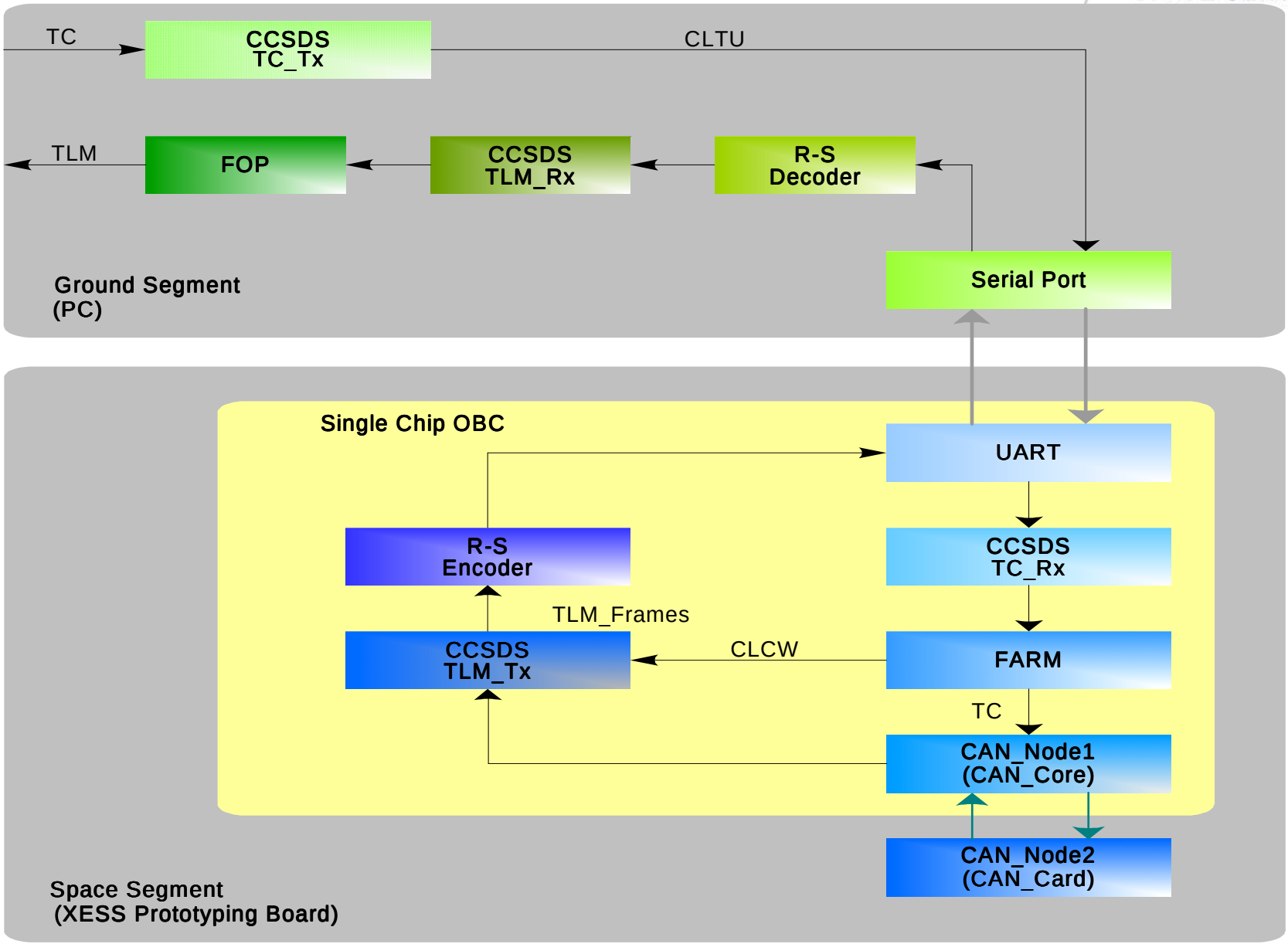
CCSDS

- Standard space industry communication protocol.
- Employed on numerous missions ranging from relatively simple low earth missions to deep space probes.
- Could lead to spacecraft interoperability, re-usable systems and mission cross support – not just for in-house missions but across the CCSDS space agencies members.

Structure and Interfaces of the CCSDS Software Package



Simulation Scheme



Downsized FPGA Implementation Summary

- Processor - LEON 2-1.0.2a VHDL IP core (SPARC V8) (ESA)
  - **Working Frequency – 25 MHz**
  - **UART Baud Rate – 38,400 bps**
  - **Internal S-Record Boot Loader**
- On-Board Network (Node 1) - HurriCANe VHDL IP core (ESA)
  - **Baud Rate: 312,500 bps**
- EDAC – EDAC VHDL IP core (SSTL)
  - **Double-bit correcting Quasi-Cyclic (16,8) shortened EDAC code**
- Prototyping Board - XESS XSV800 (Xilinx Virtex XCV800 FPGA)
  - **Up to 100 MHz programmable oscillator**
  - **16M Bits SRAM (two banks - 512K x 16)**
  - **16M Bits flash RAM**
- On-Board Application Program – S-Record File
  - **160K Bytes (CCSDS_SC Software Package)**

The CORDIC Algorithm

CORDIC equations:

$$[x_0, y_0]^T \qquad \theta = \sum_{i=0}^{n-1} \delta_i \alpha_i \qquad \delta_i \in \{ -1, 1 \}$$

$$\begin{cases} x_{i+1} = x_i - m\, y_i \delta_i 2^{-i} \\ y_{i+1} = y_i + x_i \delta_i 2^{-i} \\ z_{i+1} = z_i - \delta_i \alpha_i \end{cases}$$

$$\delta_i = sign(z_i) \qquad i = 0,1,2,...,n-1$$

Composite functions:

$\tan z = \sin z / \cos z$

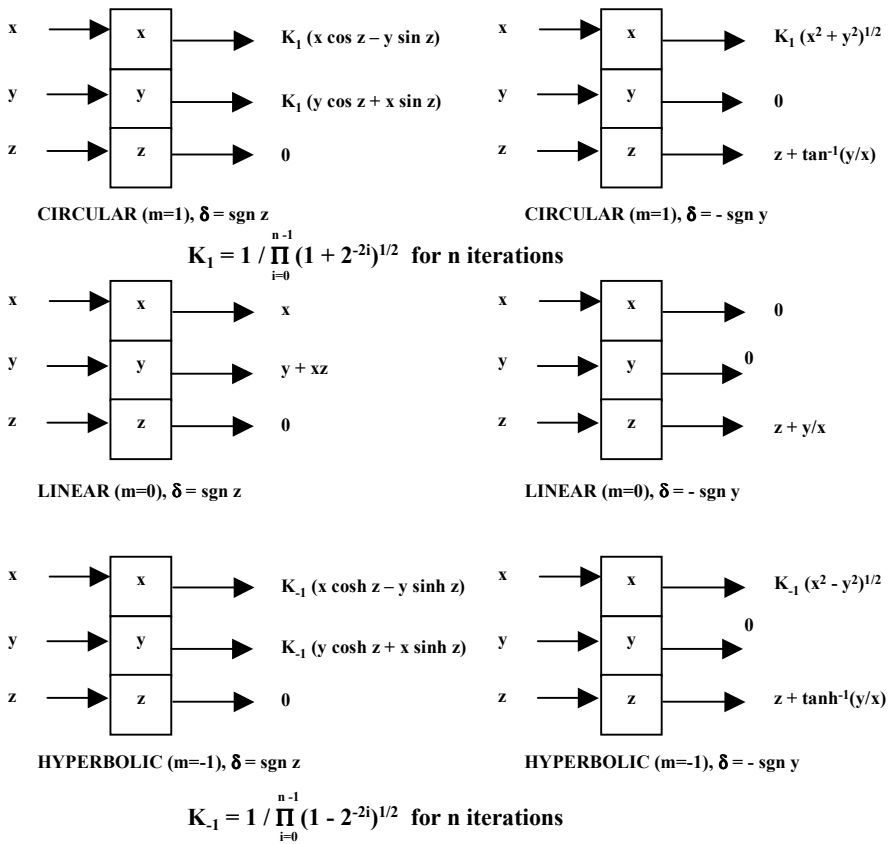
$\tanh = \sinh z / \cosh z$

$\exp z = \sinh z + \cosh z$

$\ln w = 2 \tanh^{-1}(y/x)$ *where* $x = w+1$ *and* $y = w-1$

$\sqrt{w} = \sqrt{(x^2 - y^2)}$ *where* $x = w+1/4$ *and* $y = w-1/4$

CORDIC modes

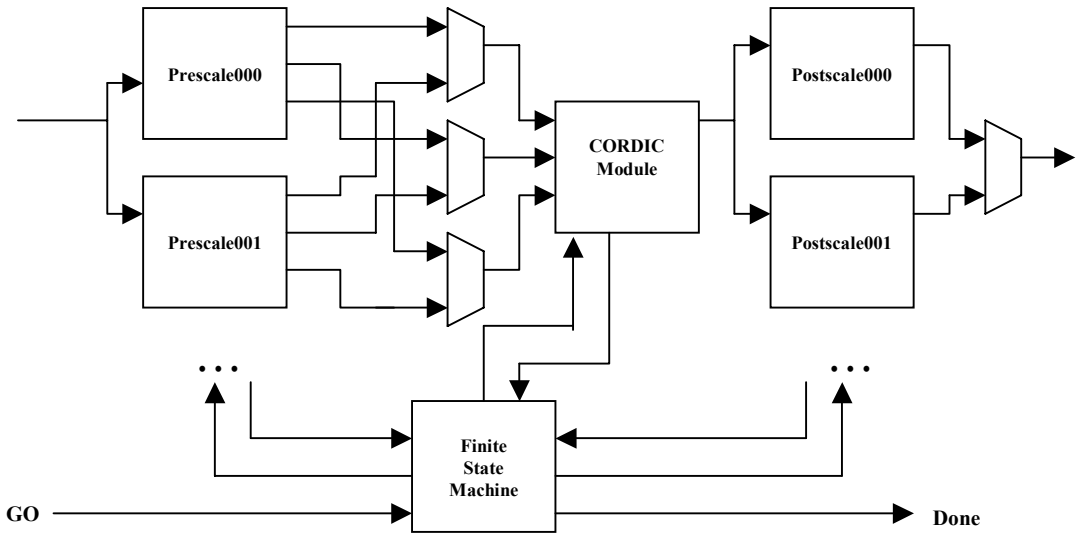


CORDIC Algorithm – Domain Extension

Idenitity	Domain
$\sin(Q\,90 + D) = \begin{cases} \sin D & \text{if } Q \bmod 4 = 0 \\ \cos D & \text{if } Q \bmod 4 = 1 \\ -\sin D & \text{if } Q \bmod 4 = 2 \\ -\cos D & \text{if } Q \bmod 4 = 3 \end{cases}$	$\lvert D\rvert < 90$
$\cos(Q\,90 + D) = \begin{cases} \cos D & \text{if } Q \bmod 4 = 0 \\ -\sin D & \text{if } Q \bmod 4 = 1 \\ -\cos D & \text{if } Q \bmod 4 = 2 \\ \sin D & \text{if } Q \bmod 4 = 3 \end{cases}$	$\lvert D\rvert < 90$
$\tan(Q\,90 + D) = \sin(Q\,90 + D) / \cos(Q\,90 + D)$	$\lvert D\rvert < 90$
$\tan^{-1}(1/y) = 90 - \tan^{-1}(y)$	$\lvert y\rvert < 1$
$\sinh(Q \log_e 2 + D) = (2^Q/2)[\cosh D + \sinh D - 2^{-2Q}(\cosh D - \sinh D)]$	$\lvert D\rvert < \log_e 2$
$\cosh(Q \log_e 2 + D) = (2^Q/2)[\cosh D + \sinh D + 2^{-2Q}(\cosh D - \sinh D)]$	$\lvert D\rvert < \log_e 2$
$\tanh(Q \log_e 2 + D) = \sinh(Q \log_e 2 + D) / \cosh(Q \log_e 2 + D)$	$\lvert D\rvert < \log_e 2$
$\tanh^{-1}(1 - M2^{-E}) = \tanh^{-1}(T) + (E/2) \log_e 2$ where $T = (2 - M - M2^{-E}) / (2 + M - M2^{-E})$	$0.17 < T < 0.75$ for $0.5 \le M < 1$, $E \ge 1$
$\exp(Q \log_e 2 + D) = 2^Q(\cosh D + \sinh D)$	$\lvert D\rvert < \log_e 2$
$\log_e (M2^E) = \log_e M + E \log_e 2$	$0.5 \le M < 1.0$
$\text{sqrt}(M2^E) = \begin{cases} 2^{E/2}\,\text{sqrt}(M) & \text{if } E \bmod 2 = 0 \\ 2^{(E+1)/2}\,\text{sqrt}(M/2) & \text{if } E \bmod 2 = 1 \end{cases}$	$\{0.5 \le M < 1.0$ $\{0.25 \le M/2 < 0.5$
$(M_x 2^{Ex})(M_z 2^{Ez}) = (M_x M_z) 2^{Ex + Ez}$	$0.5 \le M_z < 1.0$
$(M_y 2^{Ey}) / (M_x 2^{Ex}) = (M_y / 2M_x) 2^{Ey - Ex + 1}$	$0.25 \le M_y / 2M_x < 1.0$

32-Bit Floating Point Co-Processor Design

Top-Level Block-Diagram



IEEE 754 standard compliance

Sign bit	Exponent	Mantissa	Number represented
0	0	0	Zero
0	255	0	$+\infty$
1	255	0	$-\infty$
0 or 1	255	Not 0	Not-a-number (NaN)

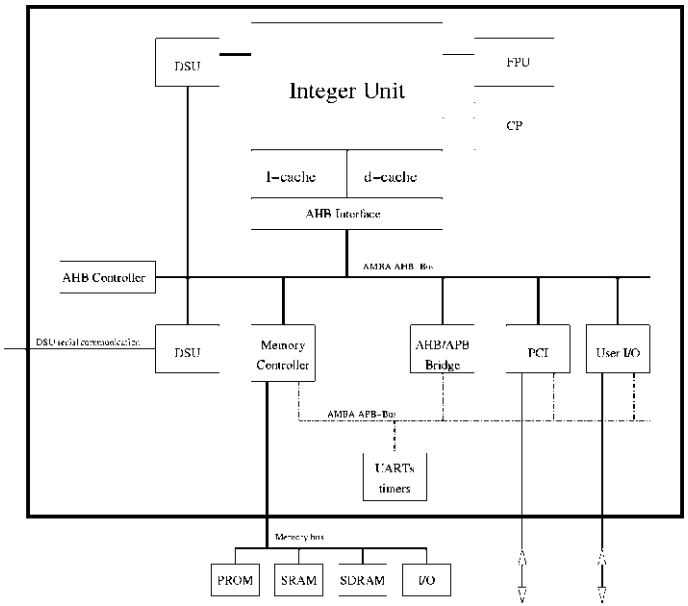
Grouping of Functions

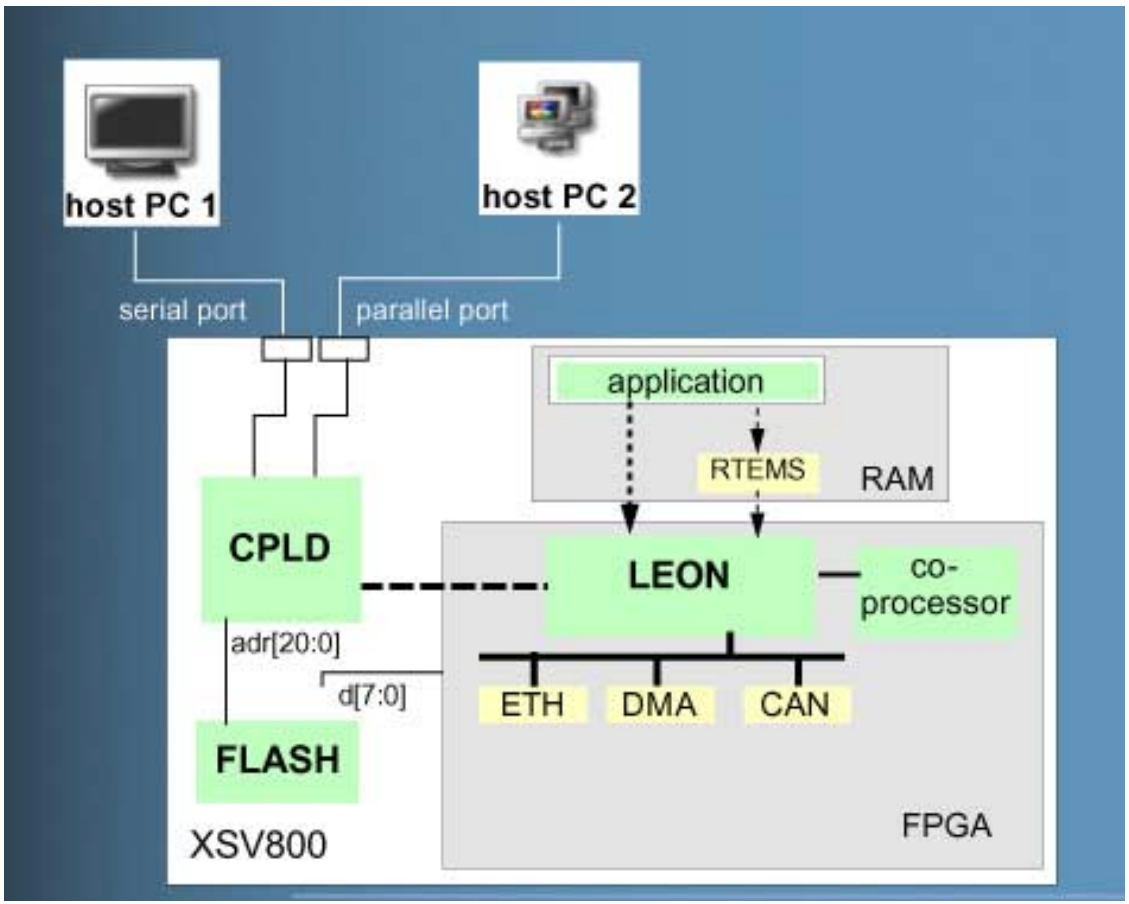
Function	Group	Number
sin	000	000
cos	000	001
tan	000	010
sinh	000	100
cosh	000	101
tanh	000	110
exp	000	111
$\sin^{-1}$	001	000
$\cos^{-1}$	001	010
$\tan^{-1}$	010	000
$\tanh^{-1}$	011	000
sqrt	100	000
multiplication	101	000
division	110	000
$\log_e$	111	000

4 arithmetic + 13 elementary functions

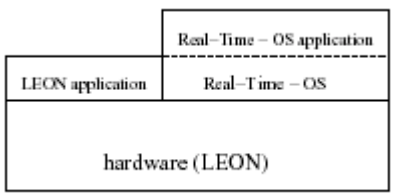
CP Integration with LEON SPARC V8

The LEON IP core





LEON with RTOS RTEMS



The Real Time Executive for Multiprocessor Systems (RTEMS) is an open source real-time operating system (RTOS), which provides a high performance environment for embedded systems

Interface with the LEON IP Core

Enabling co-processor support in a user program

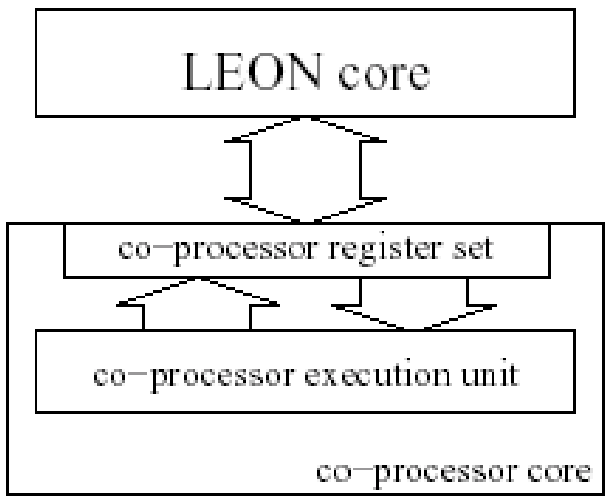
```
#ifdef CP_ENABLE
  a = cpmul(t,
      cpatan(cpmul( t2,
          cpmul(cpsin(x),
              cpdiv(cpcos(x),
                  (cpadd(cpcos(cpadd(x,y)),
                      (cpsub(cpcos(cpsub(x,y)),
                          1.0)))))))));

  b = cpmul(t,
      cpatan(cpmul( t2,
          cpmul(cpsin(y),
              cpdiv(cpcos(y),
                  (cpadd(cpcos(cpadd(x,y)),
                      (cpsub(cpcos(cpsub(x,y)),
                          1.0)))))))));
#else
c = t * atan(t2*sin(x)*cos(x) / (cos(x+y)+cos(x-y)-1.0));
d = t * atan(t2*sin(y)*cos(y) / (cos(x+y)+cos(x-y)-1.0));
#endif
```

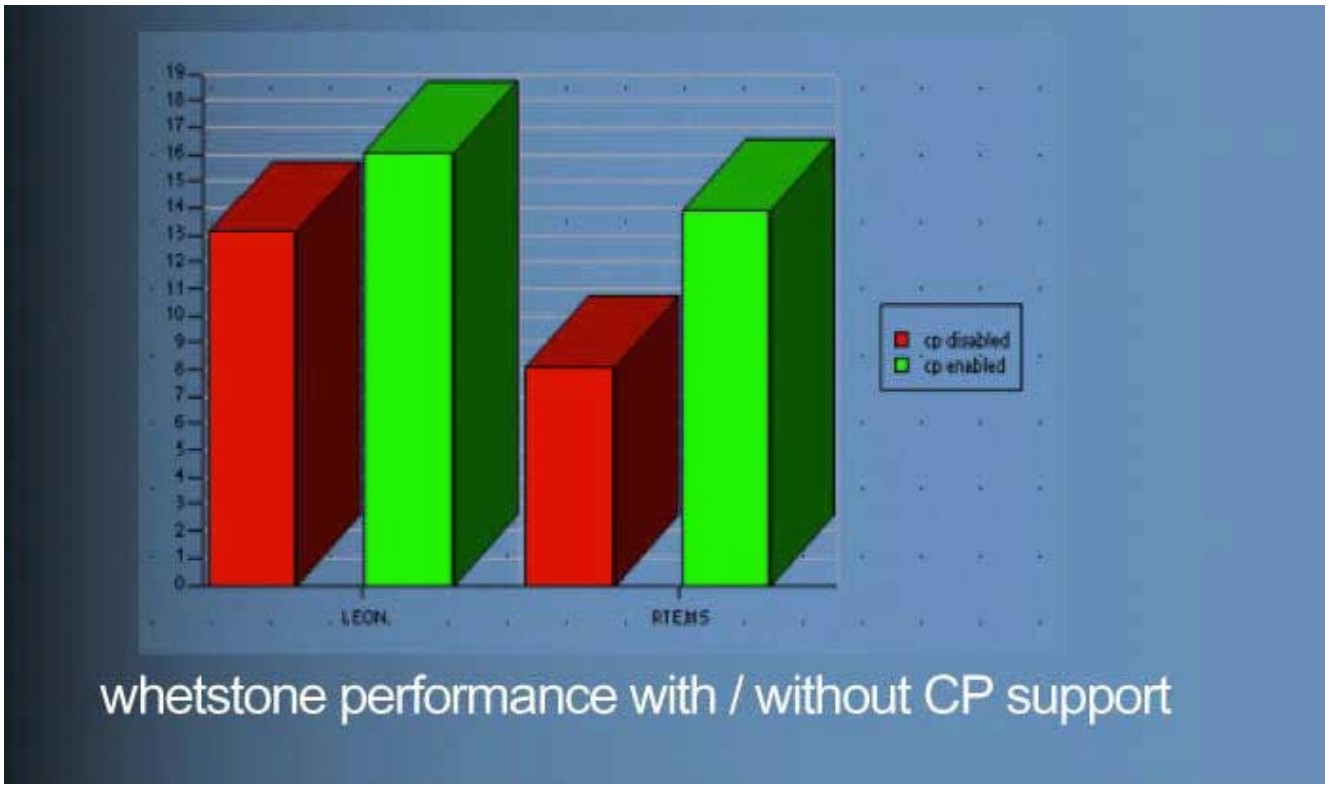
Math Library Example - module 7 of the Whetstone program

Format of the co-processor operate instructions

Command	31-30	29-25	24-19	18-14	13-5	4-0
cpop1	10	rd	110110	rs1	opc	rs2
cpop2	10	rd	110111	rs1	opc	rs2



CP Performance Results



XSV800 board				
	LEON		LEON/RTEMS	
	cp-disabled	cp-enabled	cp-disabled	cp-enabled
time (in s)	65.75	53.70	106.47	60.05
KWIPS	15.21	18.62	9.39	16.12
improvment	22.42%		71.67%	

simulation		
	LEON	LEON/RTEMS
time (in s)	43.50	133.88
KWIPS	22.99	7.47

Co-processor Summary

- A 32-bit maths co-processor VHDL core is developed for a SoC OBC based on the LEON SPARC V8 IP core -
  - **aimed at speeding up computationally intensive on-board applications, traditionally implemented in software, e.g ADCS.**
- The co-processor is fully compliant with the IEEE 754 floating-point standard and implements 17 functions:
  - **add, sub, mul, div, + sqrt, + sin, cos, tan + $\sin^{-1}$, $\cos^{-1}$, $\tan^{-1}$ + sinh, cosh, tanh, + $\tanh^{-1}$ + exp, ln.**
- The co-processor occupies half the size of a Virtex XCV800 chip.
- The co-processor operates at 2.5MHz, when integrated with the LEON IP core, at 25 MHz - when standalone.
- The co-processor accelerates execution of floating-point calculations on the Leon processor:
  - **the Whetstone benchmark runs 70% faster on Leon+RTEMS+CP compared with the time it takes on Leon+RTEMS.**

Credit-Card Size OBC System

Components:

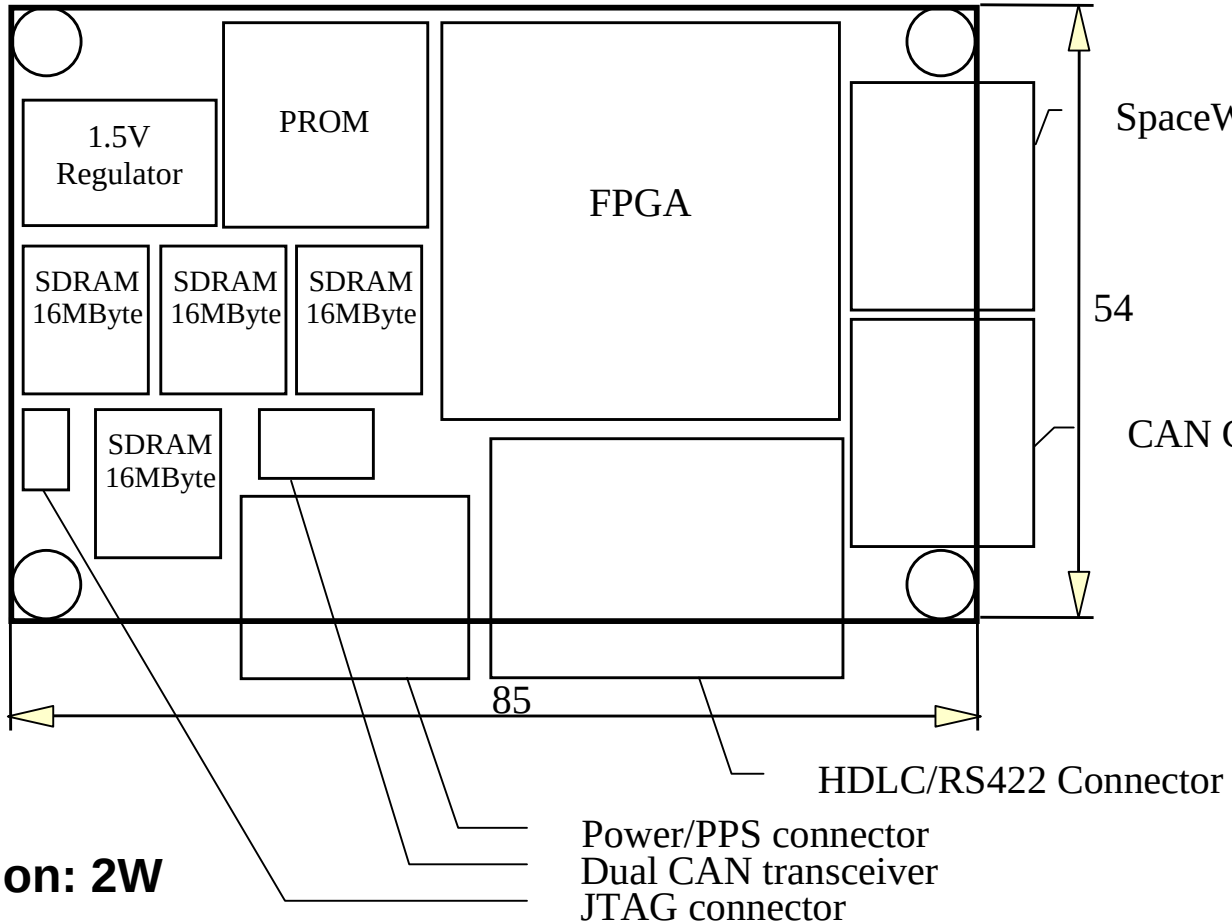
FPGA

Memory

Clock Generator

Power Supply

Transceivers



Requirements:

Power consumption: 2W

Mass: 50g

Size: 85mm × 54mm

Temperature range:

–20°C to +50°C

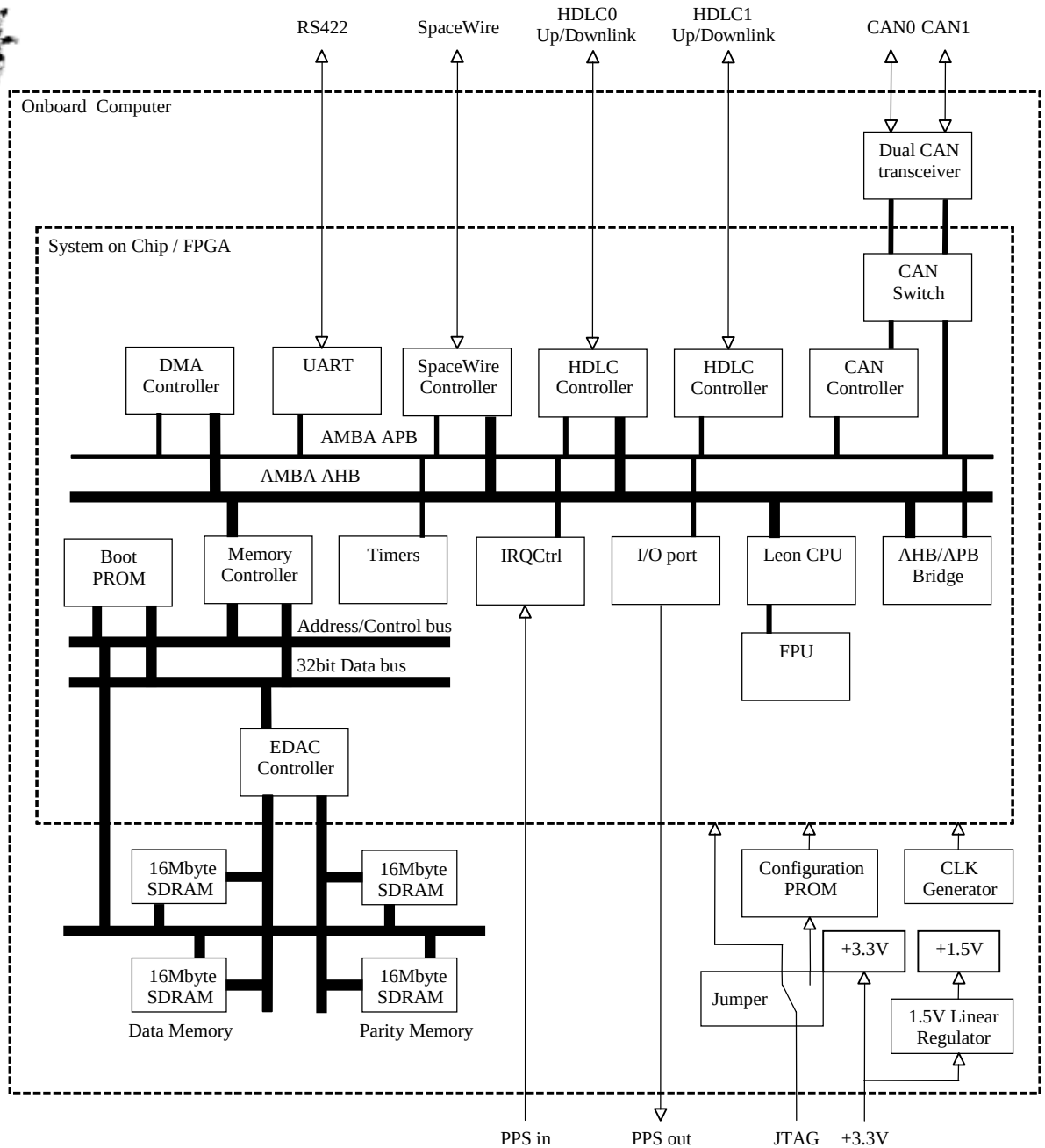
Candidate FPGAs:

Xilinx XQR2V3000

3 x 10^6 sys. gates; 1.5 V

Actel RTAX2000S

2 x 10^6 sys. gates; 1.5 V

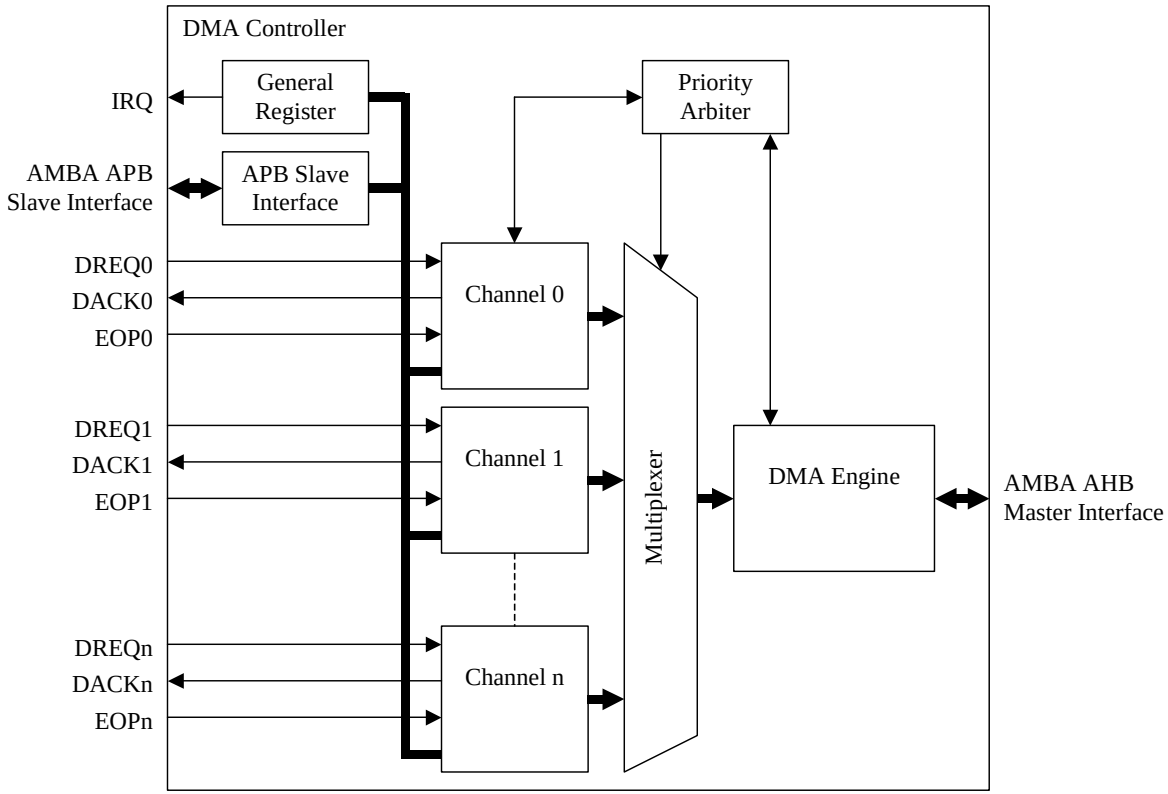


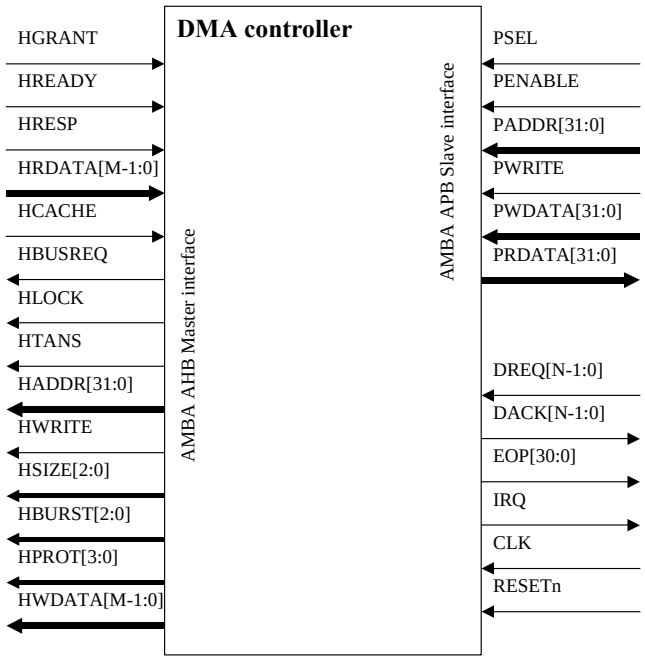
Credit-Card Size OBC System Detailed Diagram

IP Cores

LEON-2 CPU v.1.0.13
Math Co-processor
DMA Controller
CAN Controller/Switch
EDAC Unit
HDLC Interface
RS422 Interface
SpaceWire Interface
Boot Loader

DMA Controller





N - number of channels
M - width of AMBA AHB

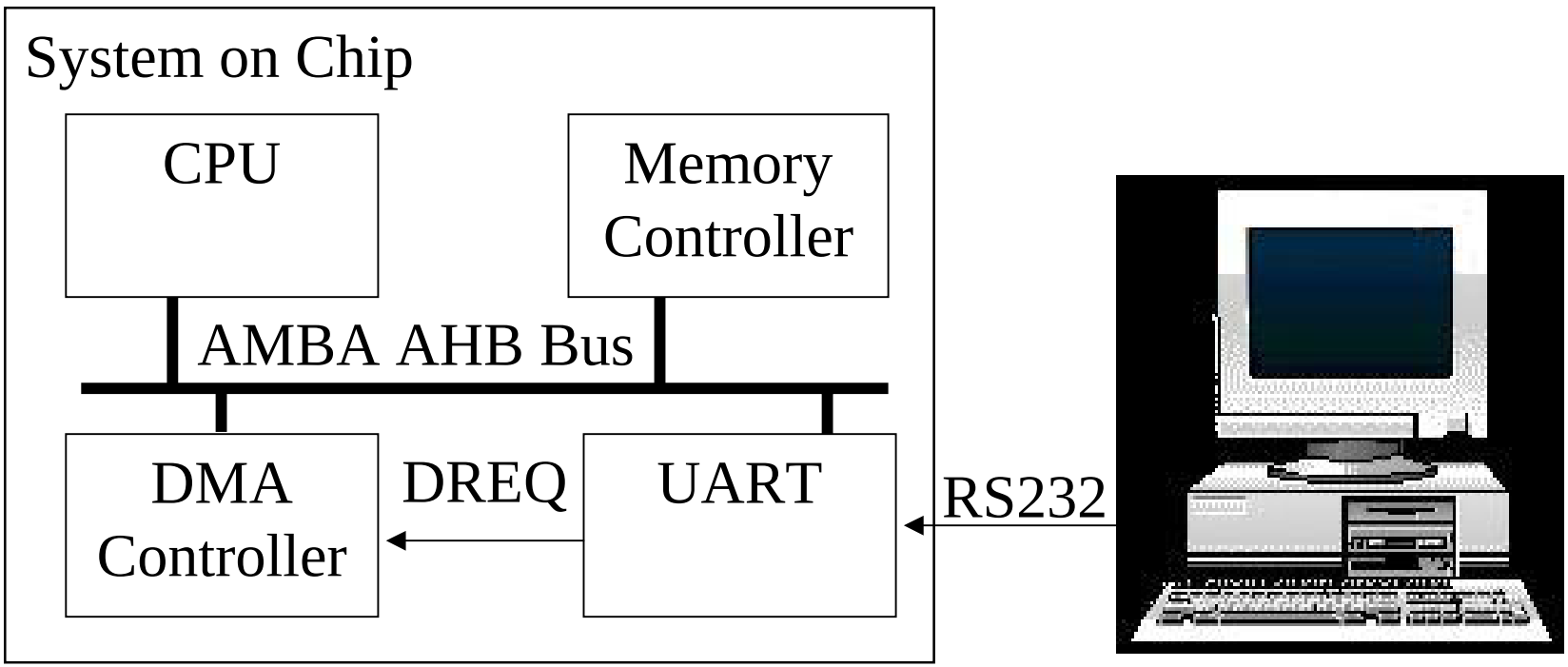
Virtex-II V2MB1000 development board from Memec:

- **XC2V1000-4FG456C FPGA**
- **32 MByte DDR SDRAM (MT46V16M16TG-75 IC from Micron)**
- **24 & 100 MHz clock generator**

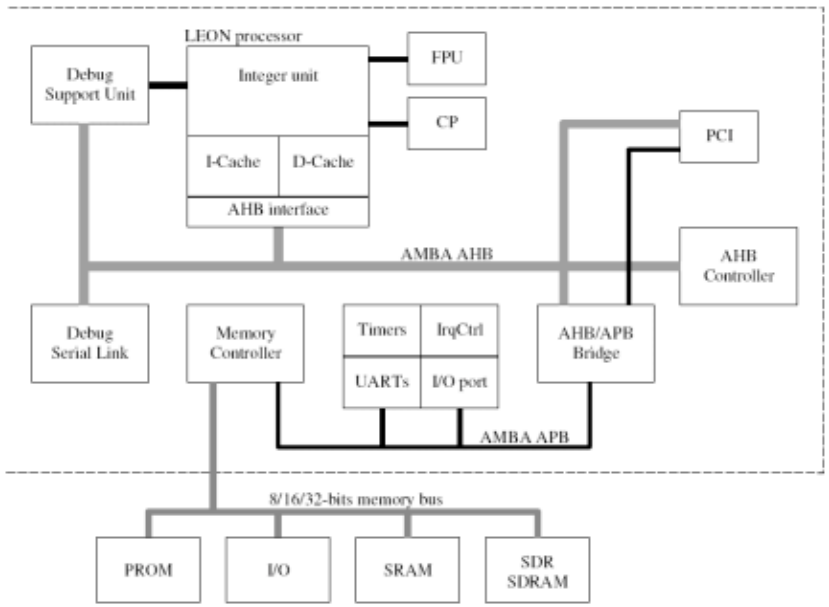
DMA Controller - Features

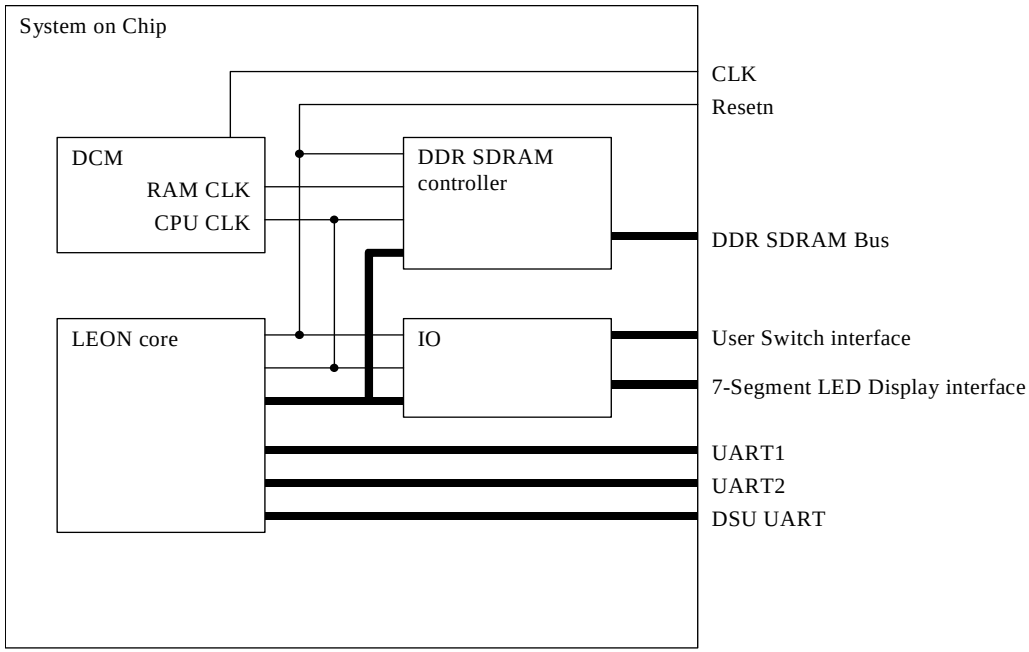
- Variable number of independent DMA channels (1 up to 32) - priority of the channels is fix; Channel 0 has the highest priority.
- Supports single transfer and block transfer
- Supports burst transfer with programmable burst length to maximize data bandwidth
- Programmable data width
- Supports both hardware initiated transfer and software initiated transfer
- Several transfer types:
  - Peripheral → Memory
  - Memory → Peripheral
  - Peripheral → Peripheral
  - Memory → Memory
- Interrupt generation on transfer completion or on transfer error
- Handles wait state insertion by any slave devices
- Supports all slave device responses: OKAY, RETRY, SPLIT, and ERROR
- Designed for the AMBA® 2.0 Bus.

DMA Controller Integration Test



LEON-2 IP Core and DDR SDRAM



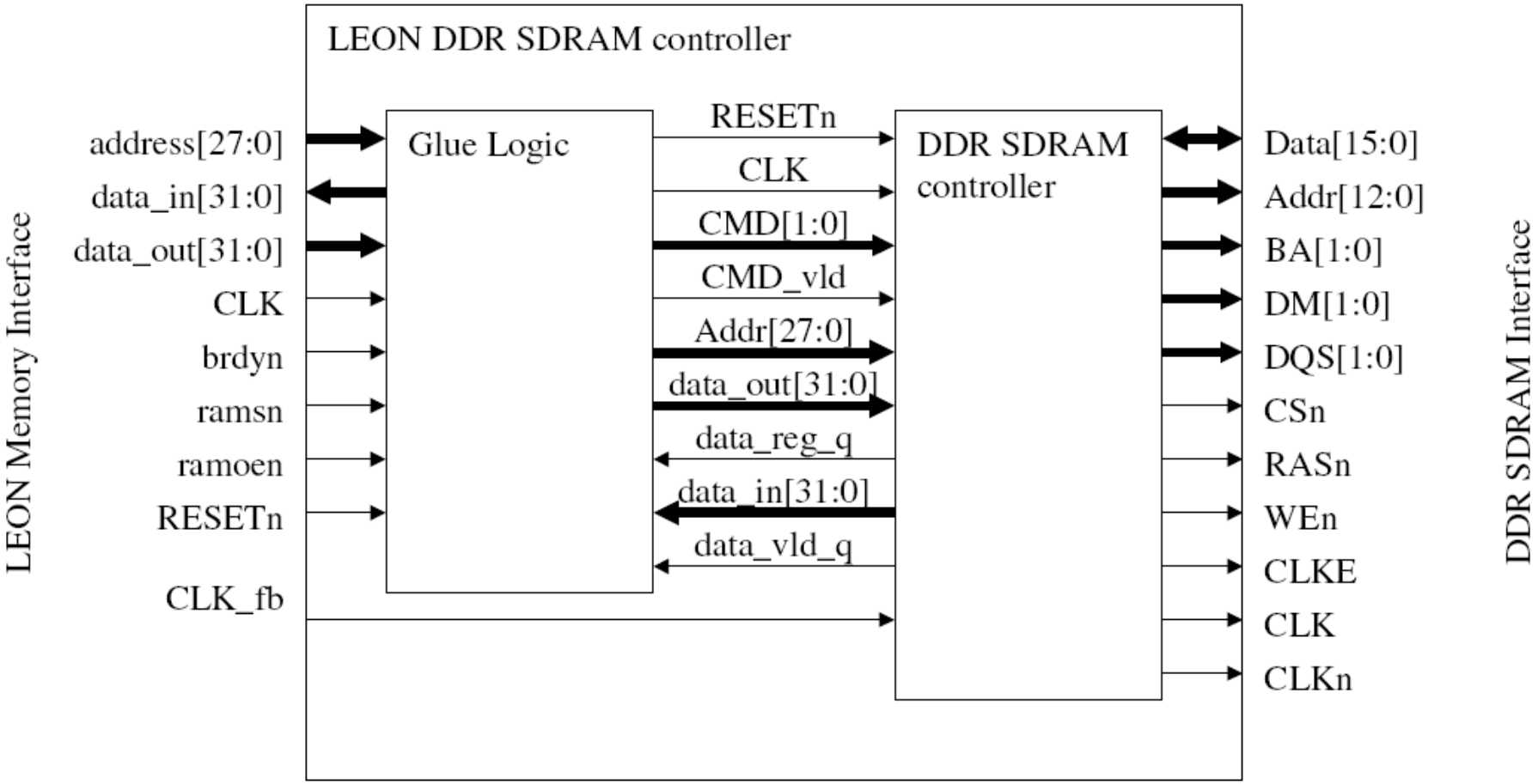


The memory controller integrated in the LEON core does not support DDR SDRAM memory.

DDR SDRAM controller from Array Electronics, Germany
(OpenIPCore General Public License)

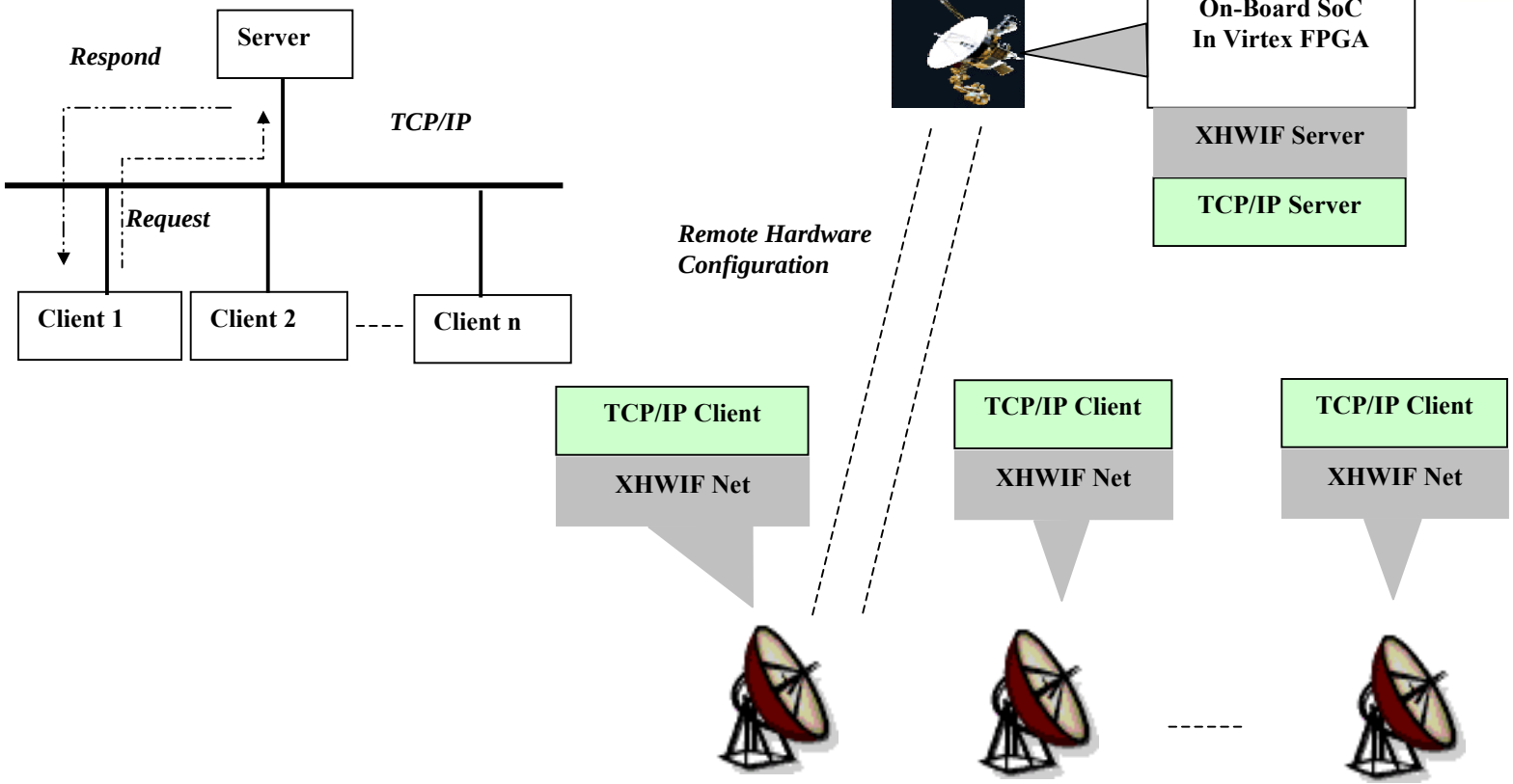
- **Integrated bank management; it does not need the CPU to initialise the memory IC.**
- **Adjusted to the LEON memory interface via addition of a glue logic unit.**

DDR SDRAM Controller



The glue logic output signals to the memory controller are synchronous with a 100 MHz clock. The glue logic output signals to the LEON CPU are synchronous with a 24 MHz clock. Two finite state machines are included in the glue logic block to match the frequencies.

Reconfigurability



- The SoC-OBC can be reconfigured remotely if implemented on a Virtex FPGA.
- The Java Runtime Environment JBits is used communicating with the ground station via Internet protocols (TCP/IP).
- The RSC-OBC acts as an equivalent to an application server allowing client Java programs to run on the server and use its resource.

Summary of SoC Research

- High-density FPGAs can serve as an appropriate medium for SoC implementation.
- A downsized configuration of the single-chip OBC consisting of LEON+CAN+EDAC has been implemented on a Virtex FPGA.
- The developed CCSDS s/w + single-chip OBC + a thin-layer h/w interface can provide a cost-effective and flexible communication solution for low-cost small satellites.
- A 32-bit floating-point co-processor based on the CORDIC algorithm which is IEEE 754 compliant has been developed and integrated with the LEON CPU:
  - 17 functions - add, sub, mul and div + 13 elementary functions
- A credit-card size OBC system based on the SoC OBC has been specified.
- A 32-channel DMA controller has been designed and incorporated with the LEON CPU together with a DDR SDRAM controller.
- A feasibility study on the SoC remote reconfigurability via TCP/IP protocols using JBits is in progress.
- Specialised peripheral cores e.g, an image compression core, are in a process of development.

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  - Daixun Zheng
  - David Eamey
  - Sven Keller
  - Michael Meier

References

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Thank You