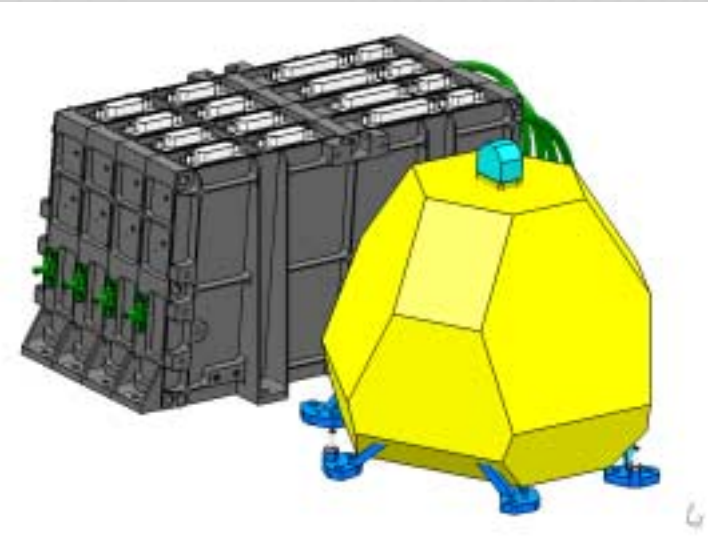
ASTRIX ASIC

Microelectronics Presentation Days

ESTEC, Noordwijk, 4th and 5th February 2004



Matthieu Dollon
matthieu.dollon@astrium.eads.net

Franck Koebel
franck.koebel@astrium.eads.net

Content

1. ASTRIX Product Description
2. ASTRIX ASIC Description
   - Context and development plan
   - Technical definition
3. ASTRIX Validation environment
   - Demonstrator board (FEM)
   - Xilinx board
4. Conclusion

ASTRIX Product description

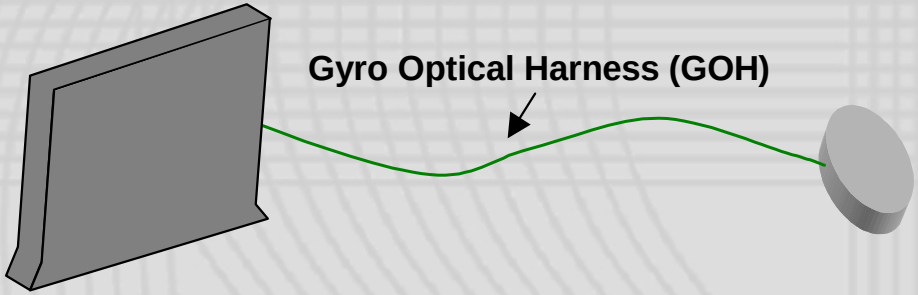
- The astrix product family is developed under ESA and CNES fundings, through Planck, Pleiades and Alphabus programs.

- Astrium willingness is to develop 3 astrix products able to fit LEO observation, LEO science and GEO Telecom applications, and thus, sharing the same core component: the Astrix ASIC.

- A dedicated « astrix product applicable documentation » has been set up for the astrix development

ASTRIX Inertial Measurement Unit

- Each Astrix IMU is the assembly of independent gyroscopic channels
- Each Astrix channel consists in:



Fog Electronics Module (FEM):

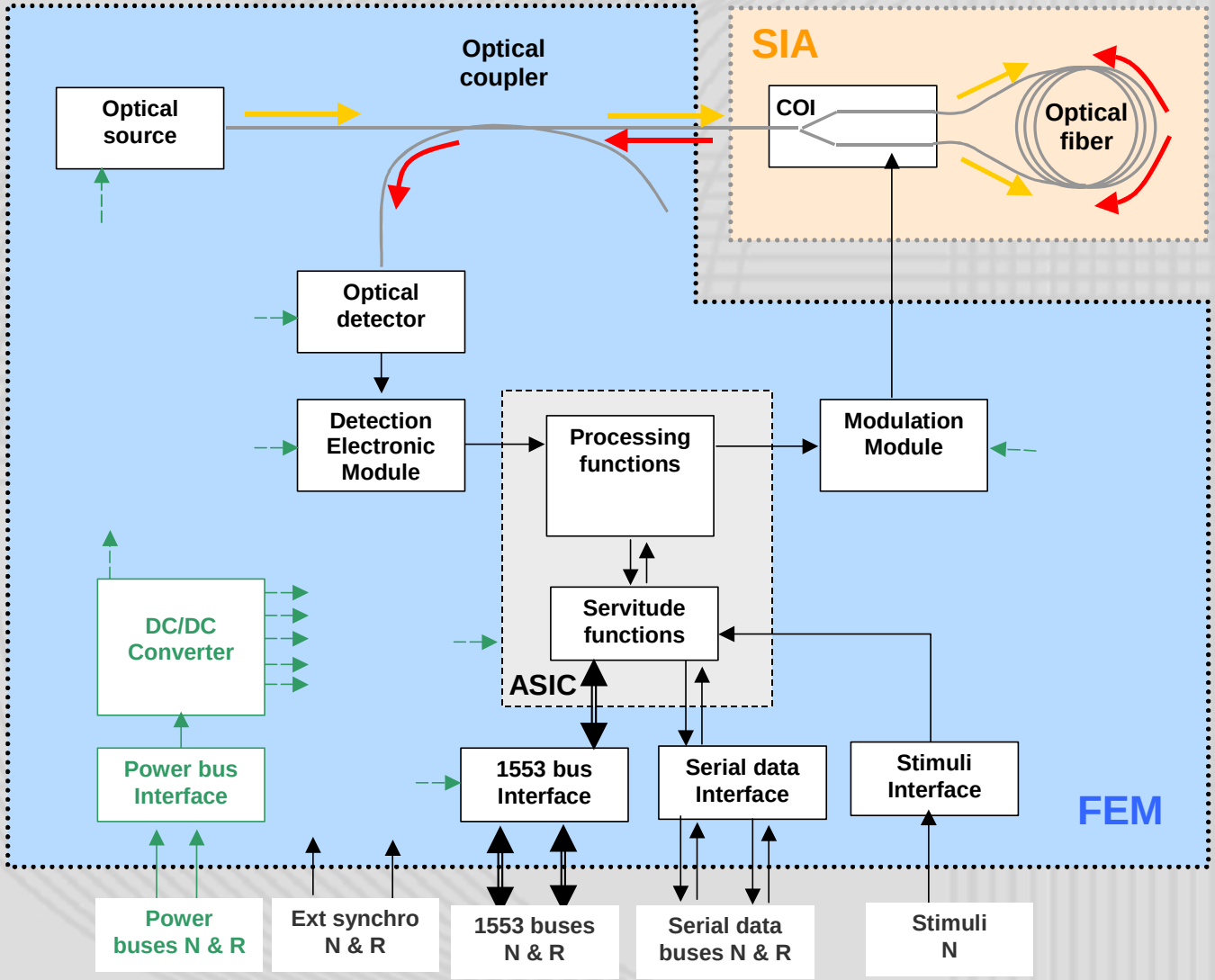
- **Inertial processing**
- **Optical source**
- **Power interface**
- **TM/TC interface**

Sagnac Interferometer Assembly (SIA)

= Inertial Sensor

One astrix gyroscopic channel

ASTRIX Channel Functional Module



ASTRIX ASIC Introduction

- Astrium and IXSEA realize the ASTRIX ASIC:
  - ASIC for Fiber Optical Gyrometer (FOG) application
  - Two main entities are designed:
    - Control part corresponds to the management of servitude functions
    - Inertial processing part corresponds to the management of gyrometer functions

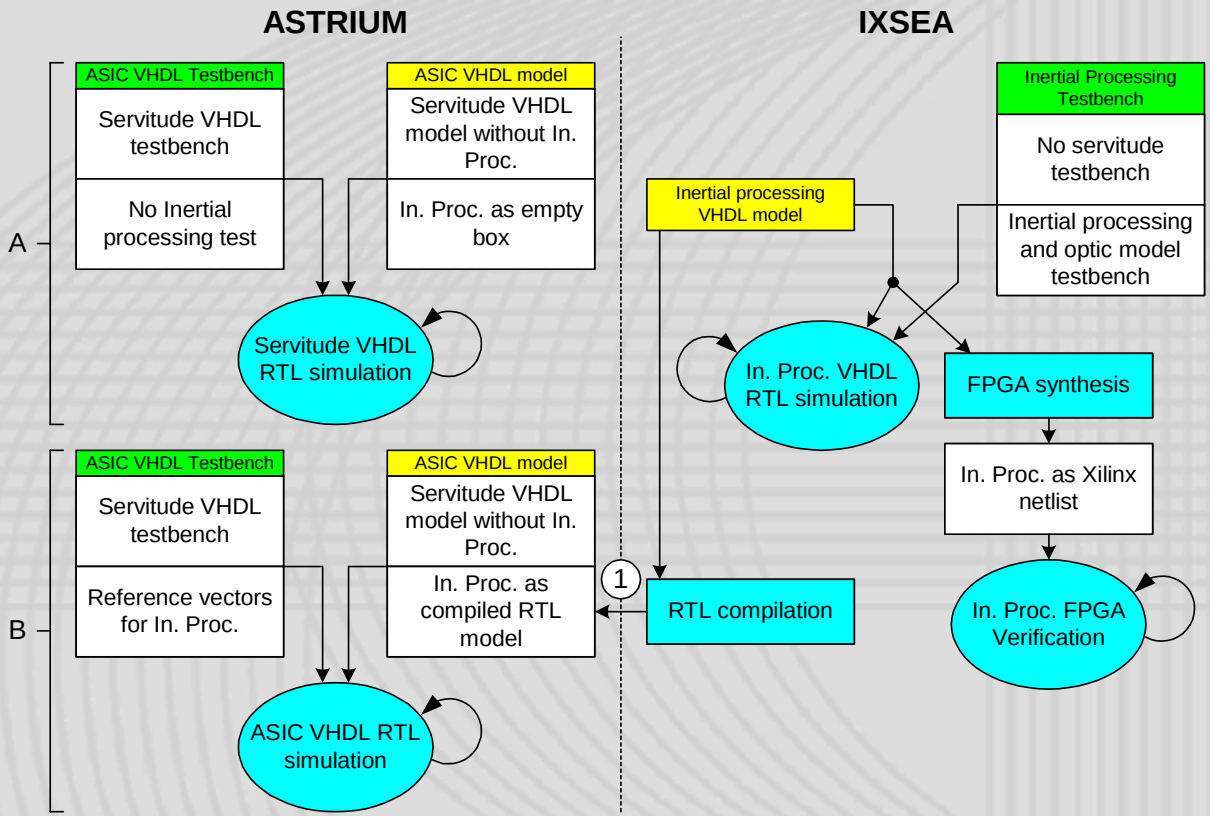
ASIC Technology

- The MG2RT technology from ATMEL is the target chosen for the ASIC
- The Nantes factory is the baseline.
- MG2RT265E is the chosen matrix, 55% gates used.
- ASIC packaging: MQFPF256, 256 pins
- 5V single voltage

Context of the ASIC

- The process followed to design the ASIC is adapted from the official ESA ASIC development since:
  - Two companies are involved
  - There are confidentiality issues that restrict the content of IXSEA reports
- Development plan takes this into account

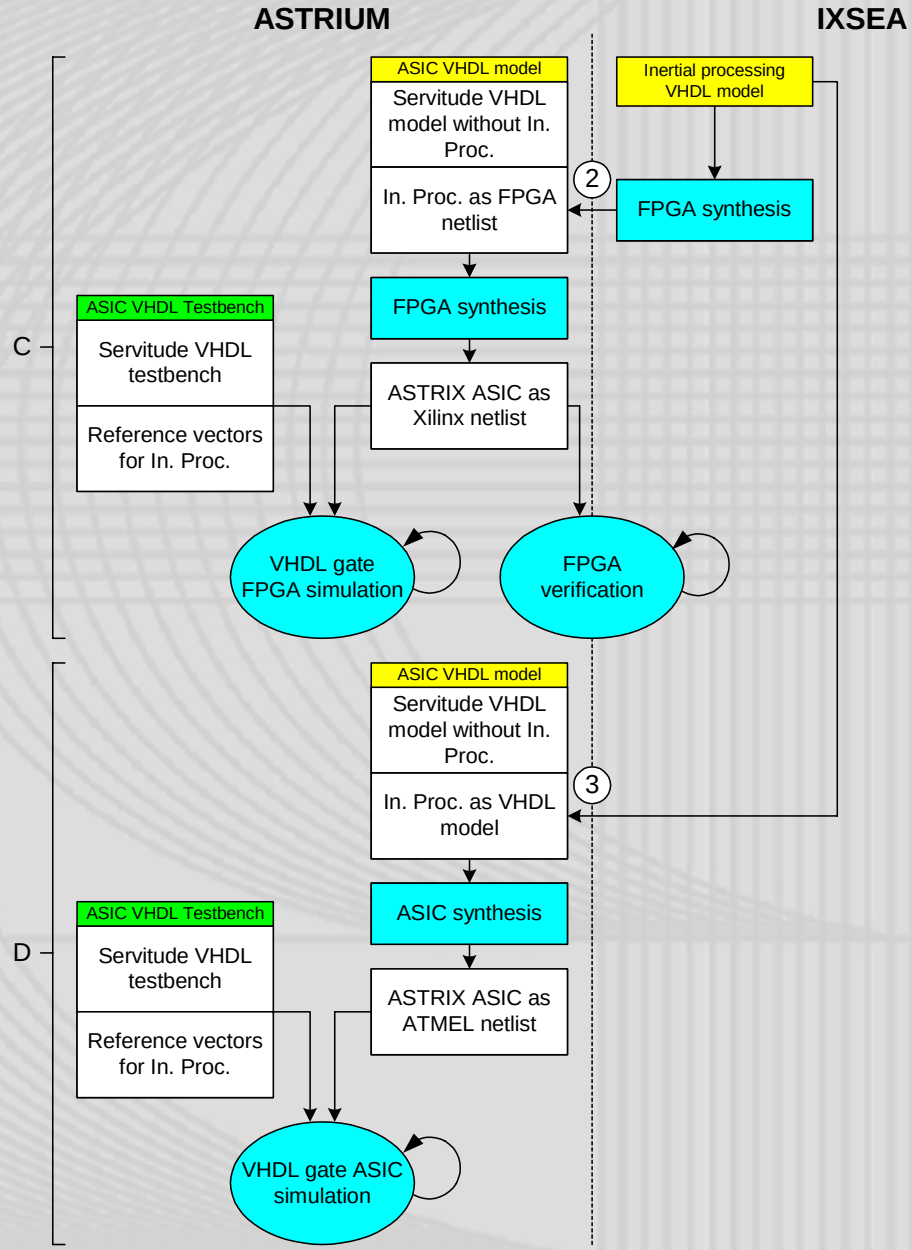
Development plan (1)



- Step A: Each company realizes a RTL verification of its block. IXSEA validates its design on a dedicated board.
- Step B: ASTRIUM starts the verification of the whole ASIC.

Development plan (2)

- Step C: Each company realizes a validation of its block with the whole ASIC as Xilinx netlist on 4 DM boards .
- Step D: ASTRIUM realizes the ASIC gate level design.



ASIC functional description

- **Control section shall interface with:**
  - Analog TM
  - External synchronization links
  - 1553 interface
  - Serial interface
  - Stimuli link
  - 1553 and gyro clock
  - Configuration

- **Inertial processing section:**
  - Fog loop
  - Anti aliasing filters
  - Digital source power control
- **Interface with:**
  - Detection module
  - Modulation module
  - Source module

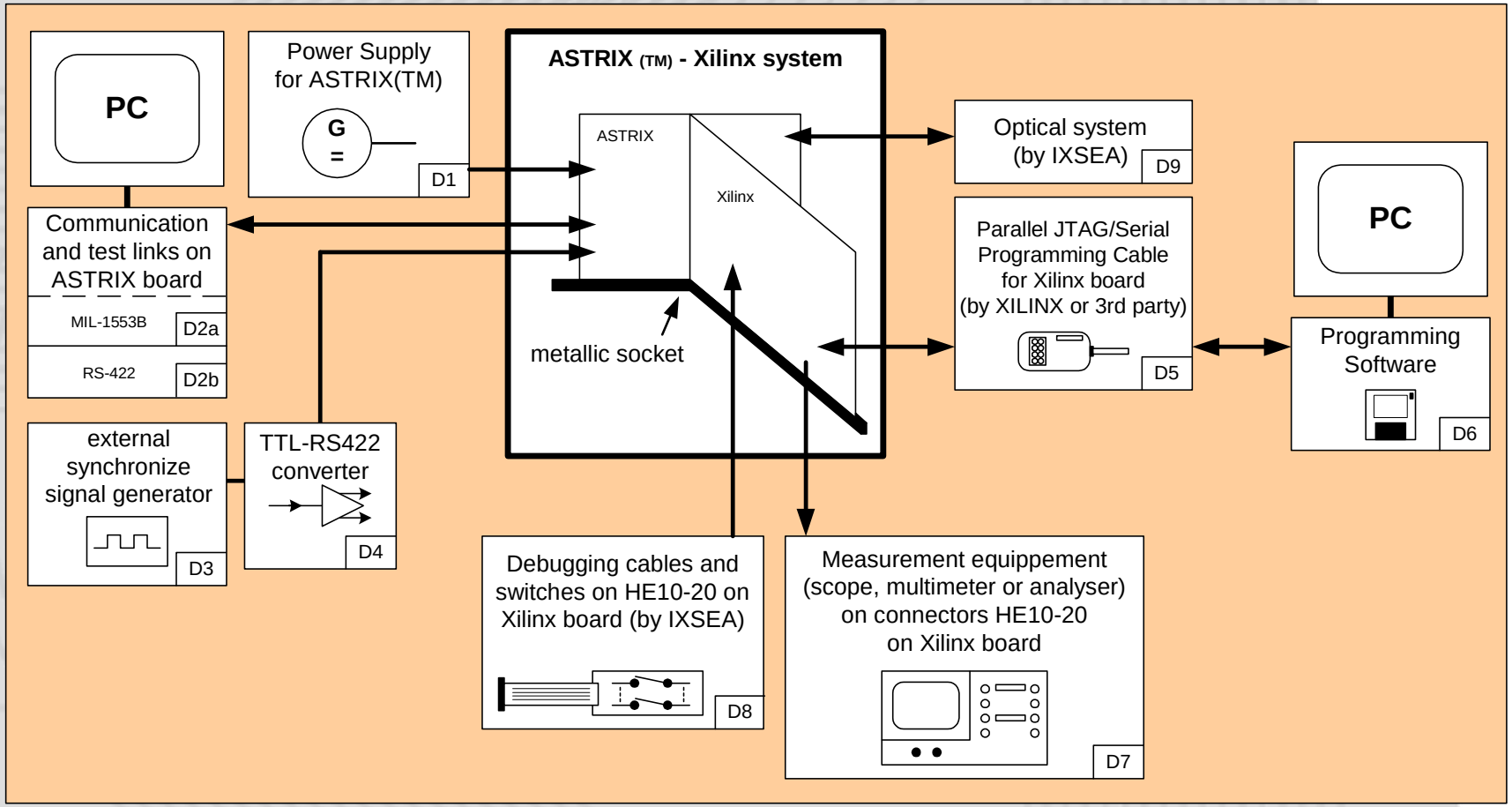
ASIC Control block

- **Control section shall interface with:**
  - Analog TM periodically refreshed
  - External synchronization link (redundant)
  - Stimuli link: UART in reception mode only
- Data links:
  - 1553 redundant buses with TM/TC specific characterization
  - Two redundant UART at 115.2 Kbaud
- Configuration
- Dating
- 1553 and gyro clock

ASIC Inertial processing block

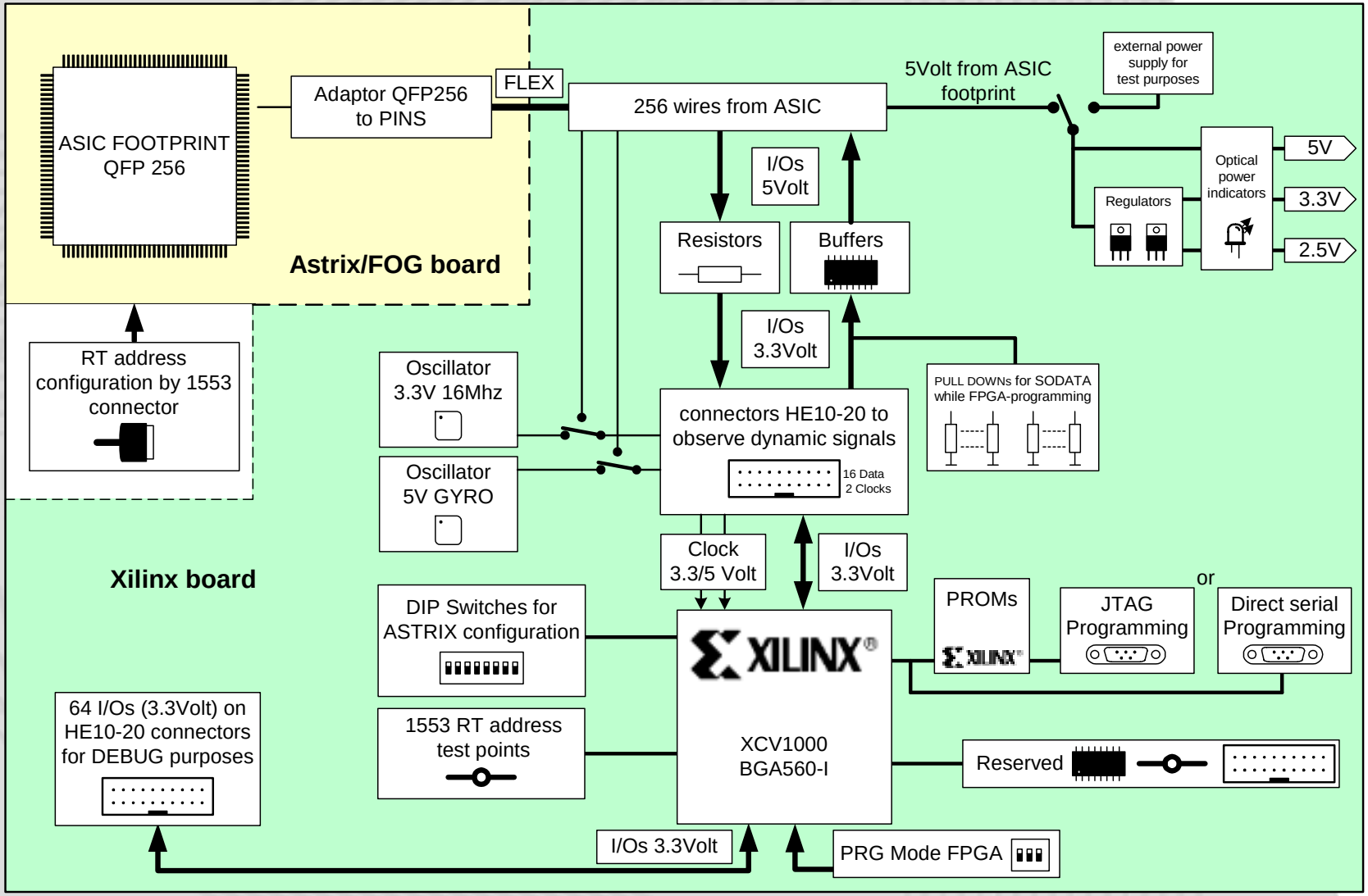
- Fiber optical gyrometer loop
  - Several configurations
  - Several frequencies possible
- Anti aliasing filtering
  - Several configurations
- Digital source power control
  - Direct command
  - Reference point driven
- Status information
- BoardTest for debugging and production tests

ASTRIX Validation environment

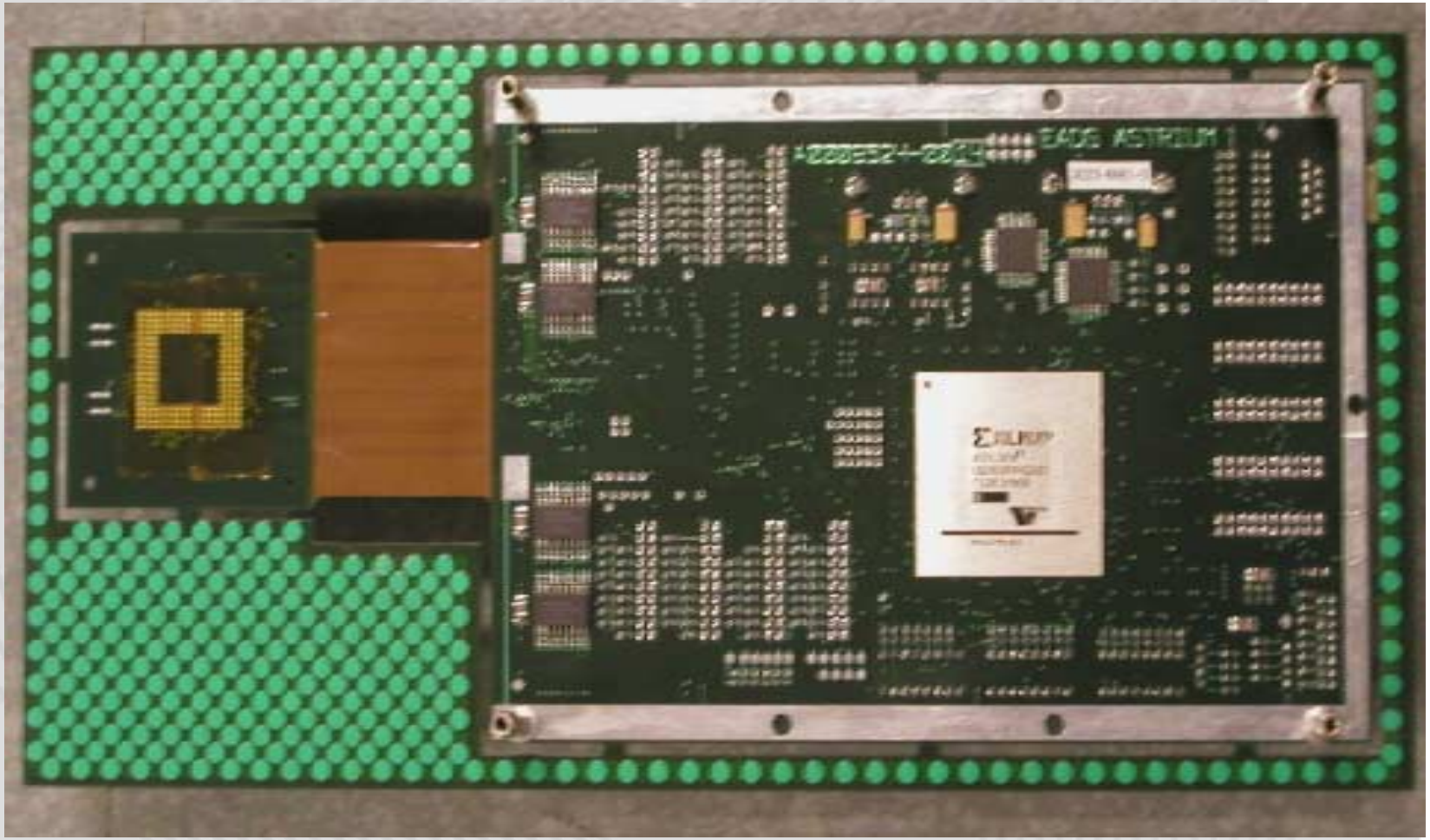


Left intentionally blank

ASTRIX Xilinx board (1)



ASTRIX Xilinx board (2)



Conclusion

- Architectural design finished
- First integration at simulation level successful
- ASTRIX and Xilinx boards manufactured
- Integration of the two entities at board level is in progress this week
- ASIC VHDL will be verified on these boards