AT697 processor prototype development status

AT697 : new generation of Sparc V8 rad hard microprocessor (ESA LEON2-Fault Tolerant model based)

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ESA contract 15036/01/NL/FM managed by TOS/EDD

Presentation Plan

- Introduction
- AT697 prototype definition
- AT697 prototype development status
- Some early design results
- Packaging
- AT697 evaluation board and development tools
- AT697 industrialization plan
- Conclusion

Evolution of the space Sparc processor product line

- European space industry strategy is to maintain an upward compatibility towards the 100 MIPS+.
- Need for more computing power at lower power consumption
- SEU induced error tolerant despite the reduction of transistor size and bias voltage
- An IP for SoC shall be derived from the new processor

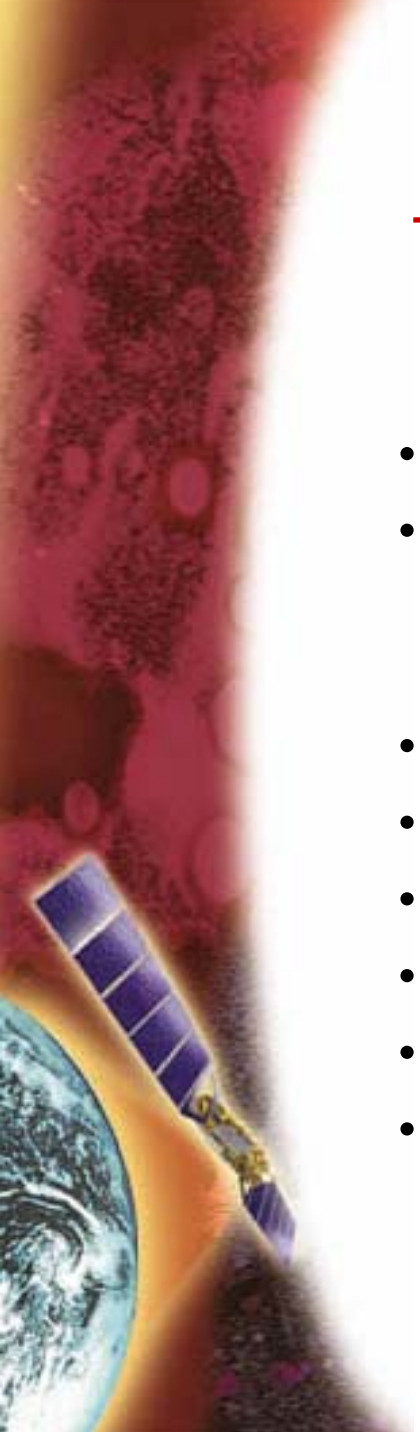
⇨ Development of a new Sparc V8 VHDL model : LEON

- Fault Tolerant (TMR, EDAC…)
- FT model owned by ESA

AT697 prototypes definition

Main characteristics

- The AT697 prototype is developed under the ESA contract 15036/01/NL/FM
  - Design, manufacturing, validation et characterization of LEON2 processor
- Implements LEON2 FT ESA VHDL model
- Heavy ions induced fault tolerance only by design : TMR, EDAC, parity
- ATC18 standard cell commercial library (AT58K)
- Industrial temperature range (-40°C to +85°C)
  - AT697 prototypes will be characterized on military range (-55°C à +125°C), without guarantee of full performance in this range
- 1.8V bias for the processor itself, 3.3V bias for buffers



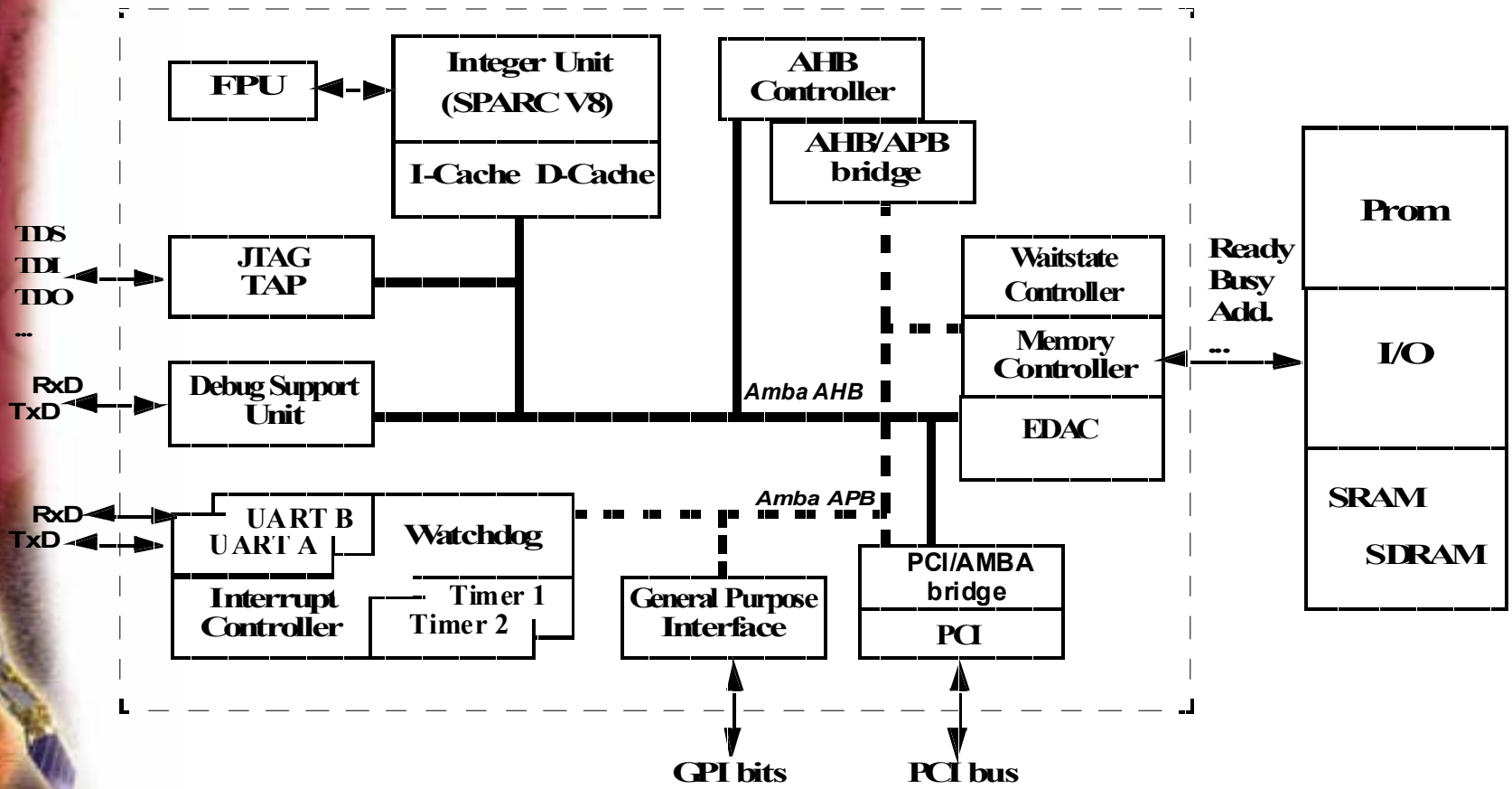
AT697 prototypes definition

Technical characteristics

- SPARC V8 32-bit LEON2-FT IU
- Separate data and instruction caches
  - Instruction cache : 32Kbytes
  - Data cache : 16Kbytes
- Floating Point Unit, same as TSC695F
- Memory interfaces to PROM, SRAM et SDRAM
- AMBA bus
- PCI 2.2 interface
- Debug Support Unit
- JTAG

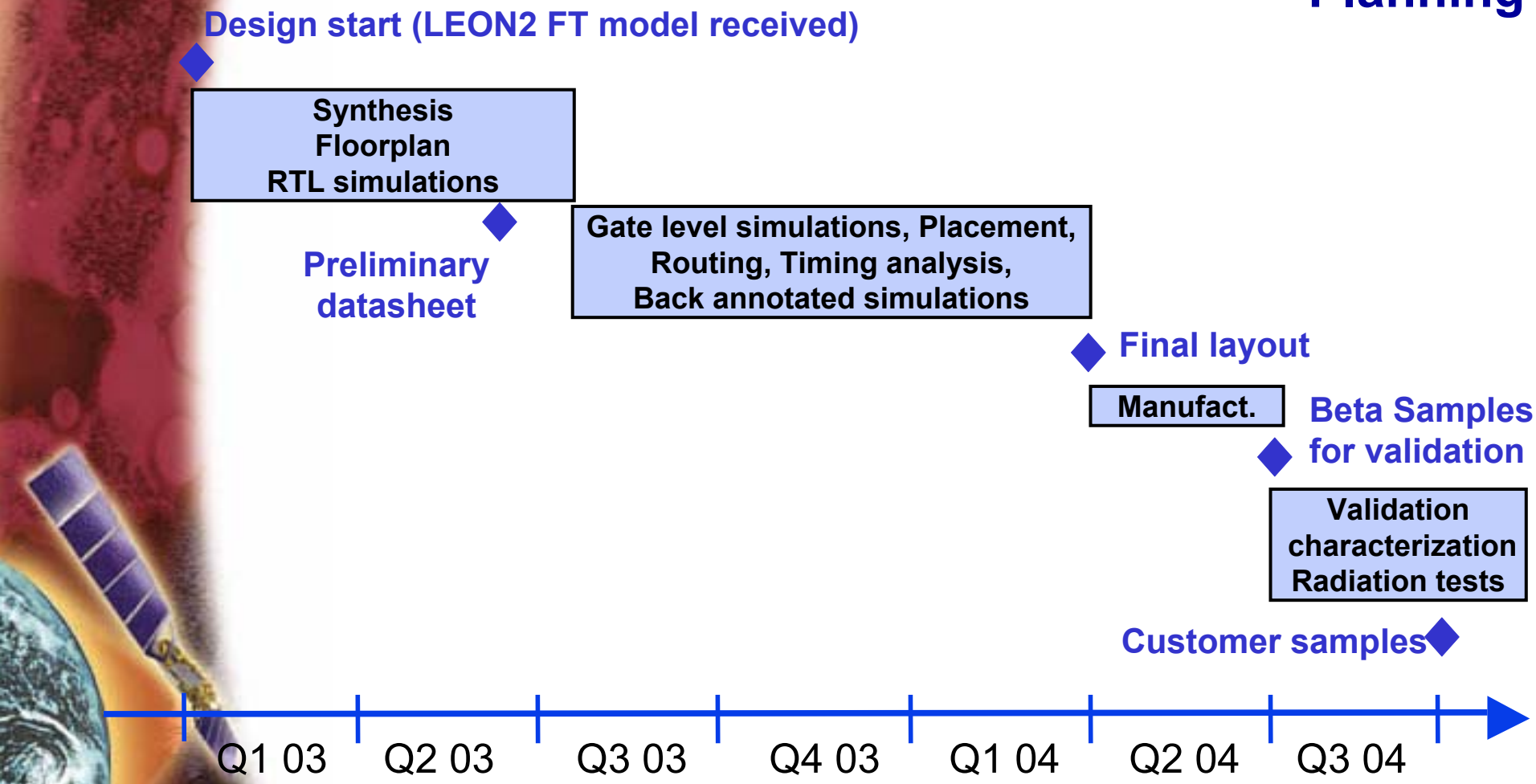
AT697 prototypes definition

Block diagram



Development status

Planning



Design results

Some technical elements

- **Frequency**
  - **Processor : 100MHz**
  - **PCI interface : 33 MHz**
- **Pad pitch : 95um**
  - **Current assembly capability space qualified**
- **Die size : 8.66 mm x 8.66 mm (standard ATC18RHA die size)**
  - **Pad limited**
- **One “bypassable” PLL to generate internal LEON clock**
  - **External direct clock entry also available**

Design results

Gate count and power consumption

- Gate count
  - LEON
    - Logic only : 225 K
    - Logic + memories (caches, regfile…) : 950 K
  - PCI : 80 K
- Power consumption
  - Around 160 MIPS / W nominal at max frequency
    - As a comparison : 20 MIPS / W for TSC695F

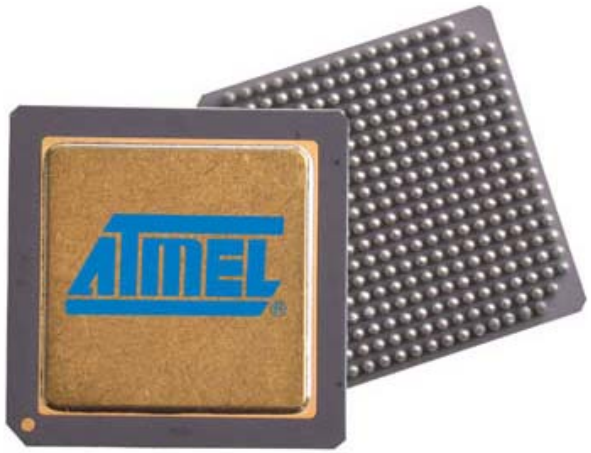
Design results

Some design issues

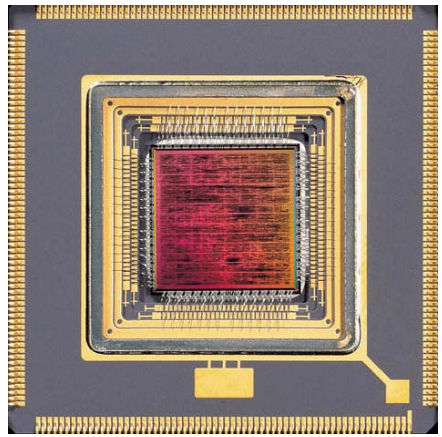
- **Synthesis tool**
  - **Synthesis issue for LEON2 fault tolerant**
- **Testbenches**
  - **RAM initialisation**
  - **Testbenches sensitivity to timings**
  - **Model multiple deliveries (fixes)**
- **Simulations hard to debug**
- **Use of ATC18 design flow**

Packaging

MCGA349

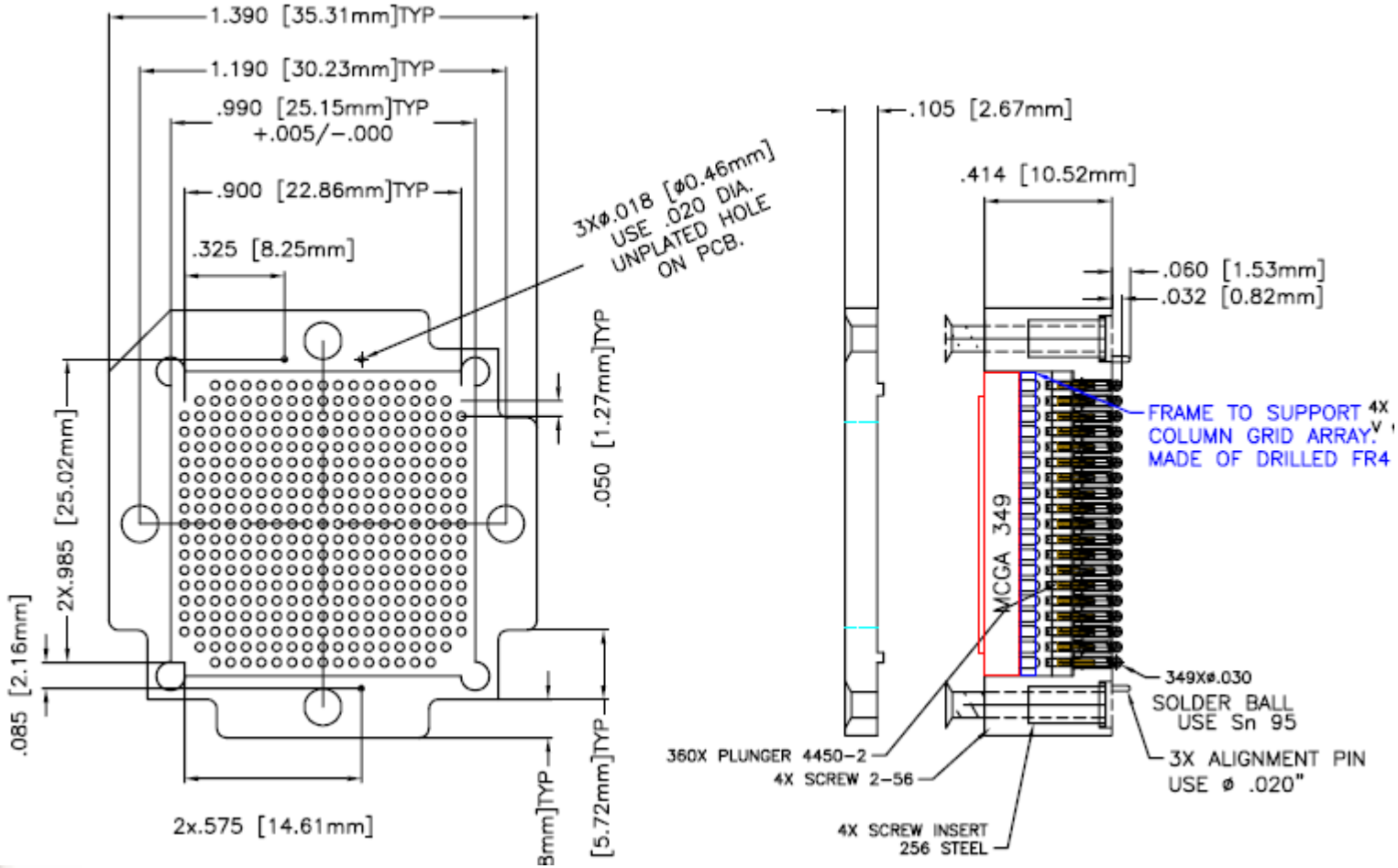


25 mm



Packaging

Socket



Evaluation board

- **Evaluation board dedicated to AT697E**
  - **Some new features compared to TSC695F :**
    - **SDRAM interface**
    - **Debugger based on Debug Support Unit**
    - **PCI interface**
- **Available in the same timeframe than AT697 prototypes**

TSC695F board

AT697 industrialisation plan

- **Validation & characterization feedbacks expected end Q3 04**
  - **From ATMEL internal tests, ESA and alpha-customers**
- **Industrialization in Q4 04 / Q1 05 will include :**
  - **Use of ATC18RHA library characterized for AT58KRHA to mil temp**
  - **Bugs (if any) corrections or simple additions from ESA and alpha customers**
  - **Full electrical characterization**
  - **Qualification, radiation tests for production version**
  - **Hi-reliability specification following the European QML rules**
- **Flight model availability : Q4 05**

Conclusion

A new european space processor

- A processor around 100 MIPS for space applications
- Continuity with existing european space processors
- Good performance versus consumption trade-off
- Protected against heavy ions induced errors
- Paves the way to System-On-Chip