Design of High Speed Pipeline ADC

Väinö Hakkarainen

vjh@ecdl.hut.fi

Electric Circuit Design Laboratory

Helsinki University of Technology

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Outline

- Background
- Resources
- Specifications
- Architecture
  - ADC
  - Clock generation
- Phase 1 test chip
  - Schematics & Simulations

Background

- Wideband high speed ADCs required for satellite comminications
- Target to design and implement high speed ADC to feed poly phase filter
- Project started: 12/2002
- Closing: First half of 2005

Resources

- ECDL (Väinö Hakkarainen, Mikko Aho, Jaana Riikonen, Kari Halonen)
  - ADC design
  - Calibration
- VTT (Arto Rantala, David Comes Martins, Markku Åberg)
  - Clock generation & skew calibration
- Nokia (Paavo Kosonen, Tom Ahola)
  - Measurements

Target Specifications

- Resolution 9-10 bits
- Sample Rate 1.8-2 GS/s
- 500 MHz input bandwidth
- Monolithic ADC
- “Low” power dissipation (<10W)
- Target technology: BiCMOS 0.35 µm (SiGe)

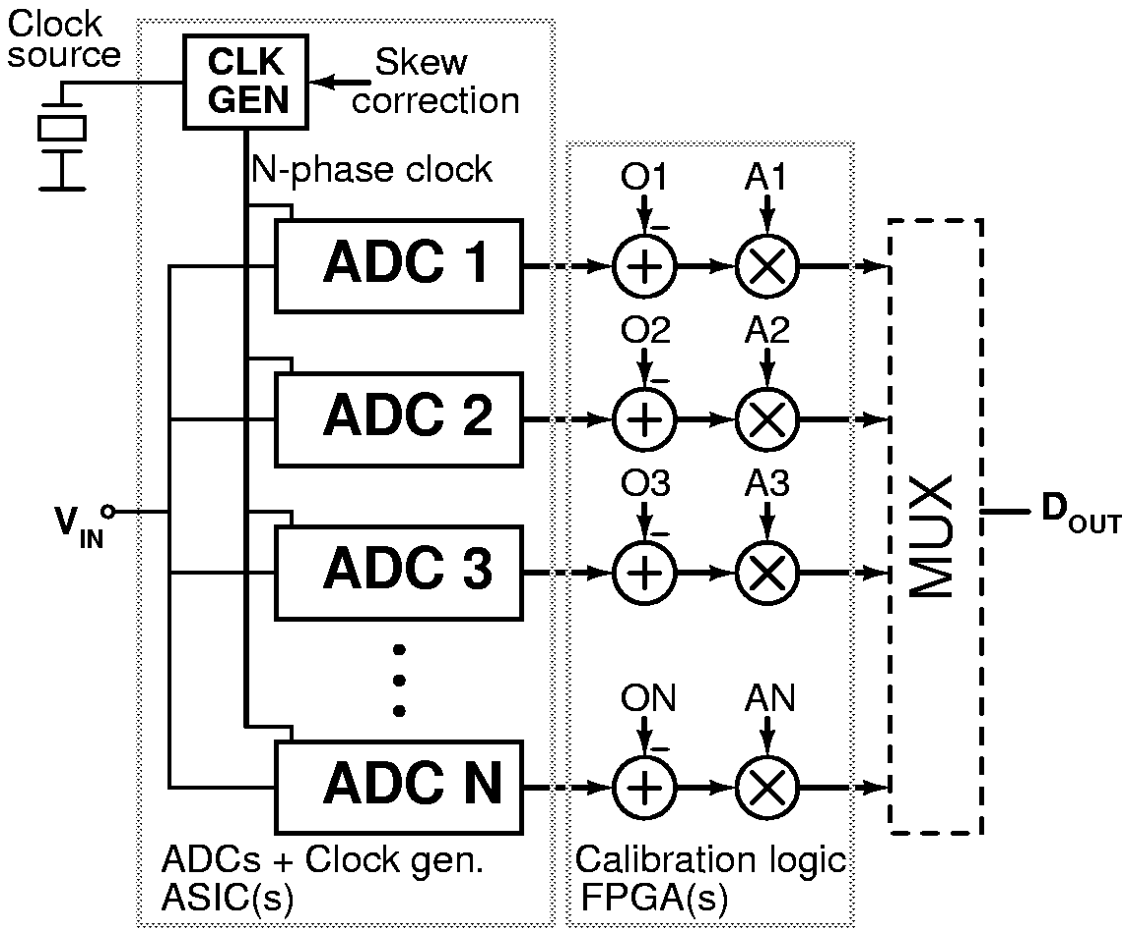
Design Challenges

- Clock generator is the most critical block
  - Jitter specification
  - Resolution of the skew correction
- Calibration
- Area and power dissipation must be controlled
- Measurements @ 2 GS/s Sample rate
- Very tight schedule
  - Test chip + final version within two years

Architecture (1)

- Pipeline topology most suitable
  - Resolution
  - Calibration
  - Double-sampling
  - Time-interleaving
- DLL based clock generation
  - Lower jitter than in PLLs
  - Skew calibration achievable

Architecture (2)

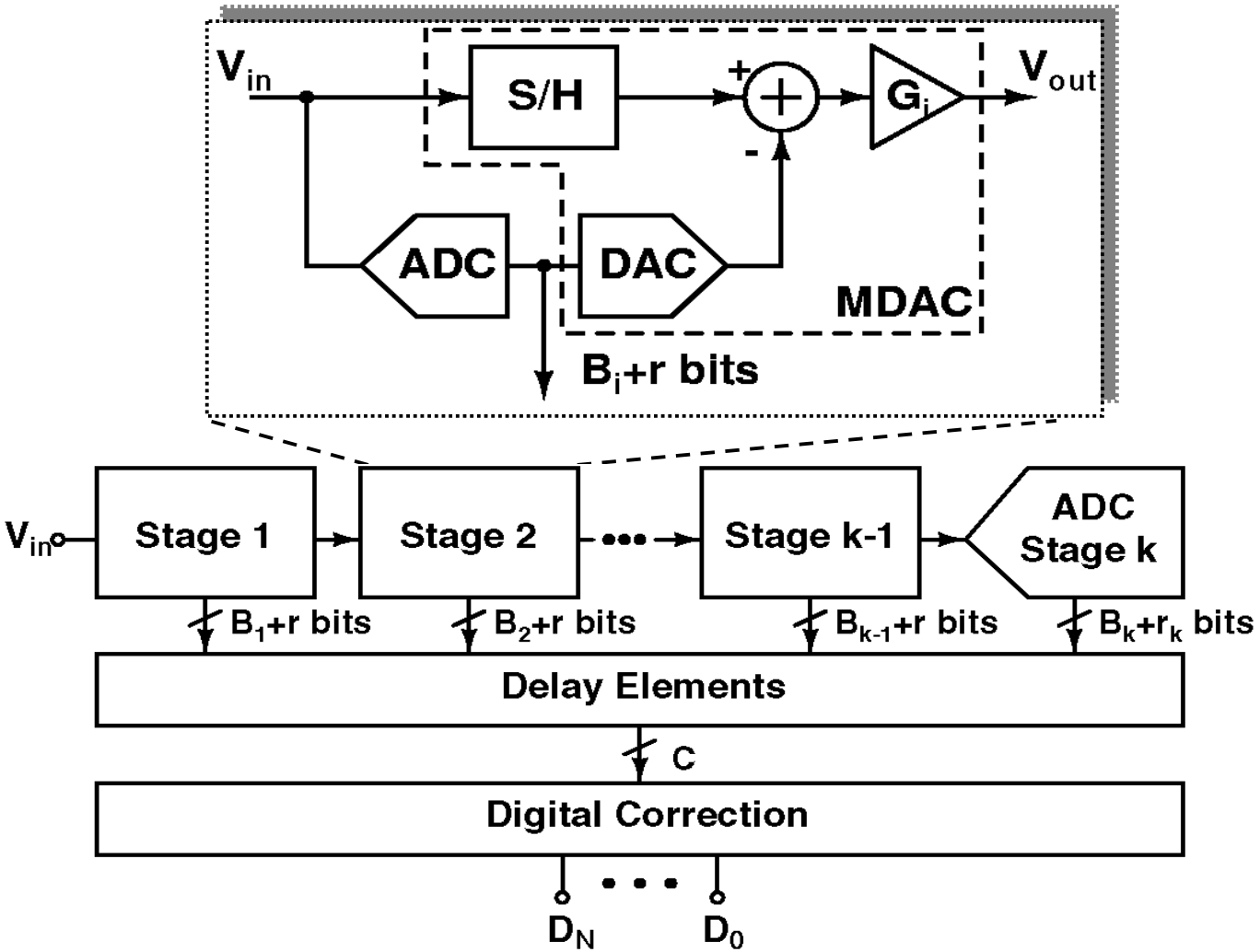


- Time-interleaved parallel pipeline
- Low-jitter clock generator with skew correction
- Digital calibration of channel gain and offset mismatch

Architecture -Summary

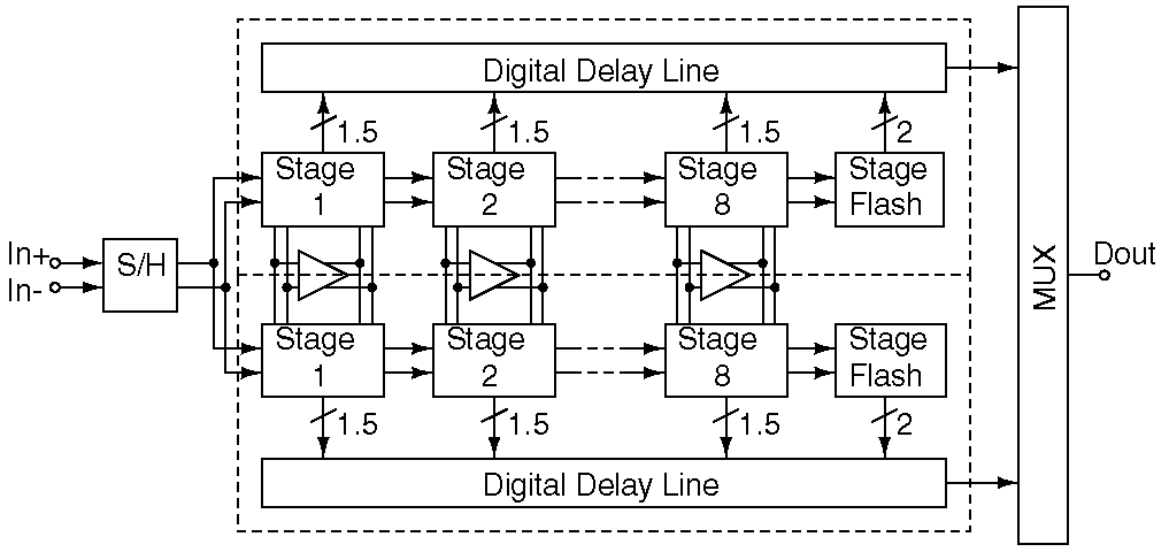
Architecture	Monolithic Time Interleaved Pipeline
Resolution	9-10 bits
Sample Rate	1.8-2 GS/s
Number of Channels	24
Channel Clock Rate	75-85 MHz
Calibration	Digitally with FPGA
Sample Clock Generation	Adjustable DLL
Technology	0.35-µm BiCMOS (SiGe)

Pipeline ADC



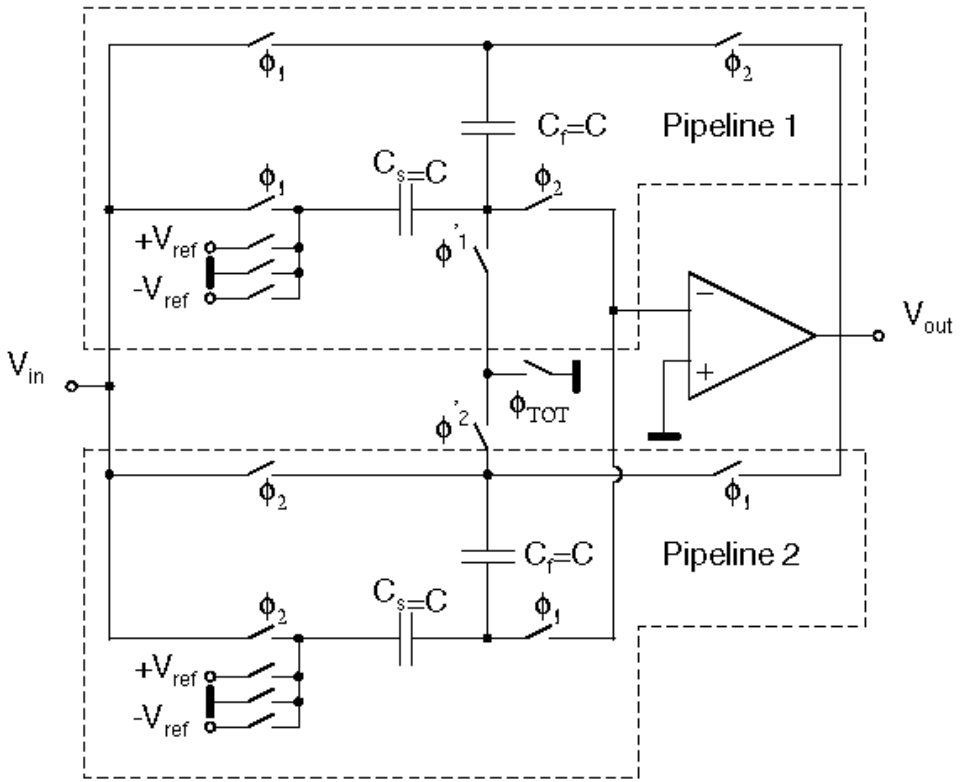
Double-Sampling (1)

- Shared opamp between two pipeline fingers
  - Working in opposite clock phases
- Lower power dissipation but,
- Memory effect could cause error
  - Faster settling required



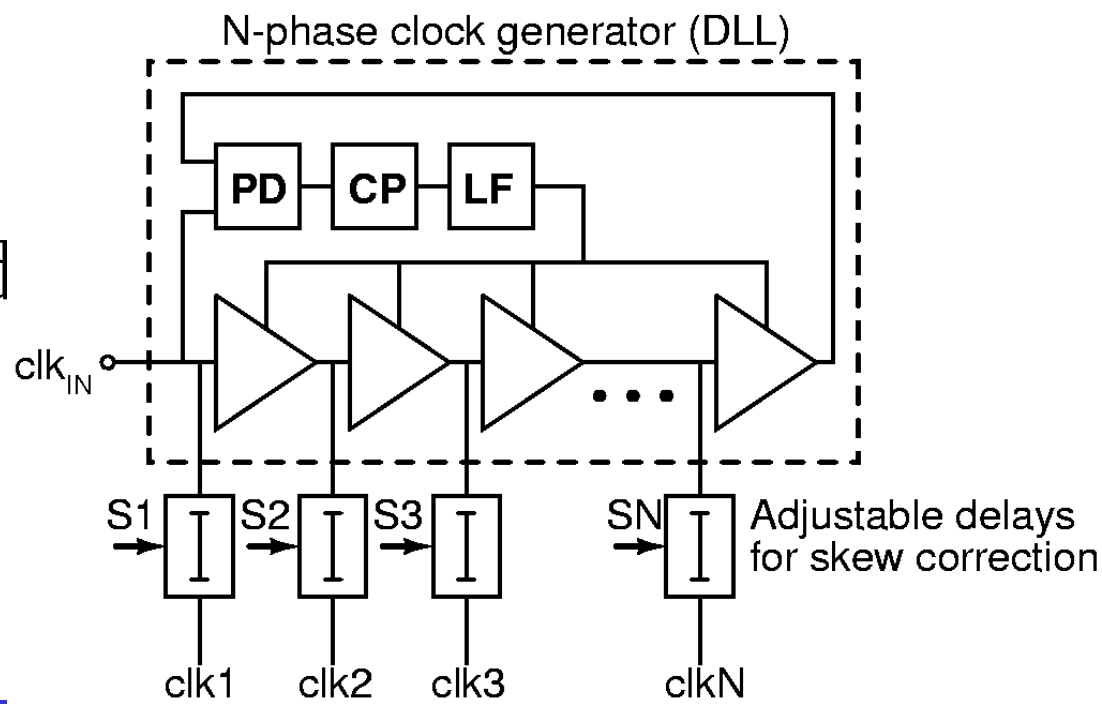
Double-Sampling (2)

- Φ_1 and Φ_2 in opposite phases
- Bottom plate sampling utilized (Φ_1' Φ_2')
- Φ_{TOT} operating at 2*f_s => Skew insensitivity



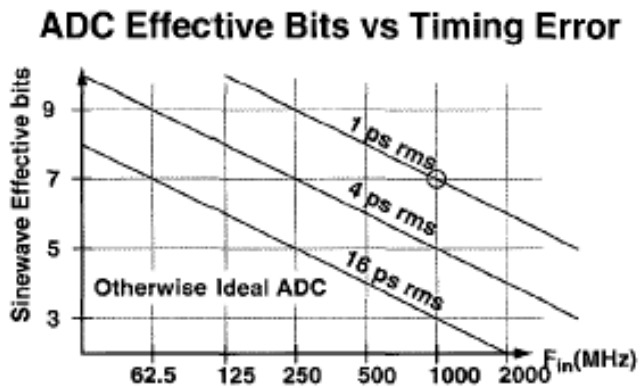
Clock Generation

- Lowest jitter with external crystal oscillator
  - ENOB = 8 bits @ 1 GHz requires $\sigma_a < 0.5$ ps
- Adjustable DLL
- Skew between channels minimized with calibration
- Very careful layout design



Jitter Minimization

- DLL achieves a lower jitter than PLL
  - Also favorable for time-interleaved ADC
- Thermal jitter of a DLL ~ N^2 (N = length of DLL)
  - High-frequency external crystal oscillator
  - Dividers after DLL to get 20 clocks
- Additional jitter from on-chip components minimized
- If not enough, additional steps
  - Combination from several clock signals



Clock Skew Calibration

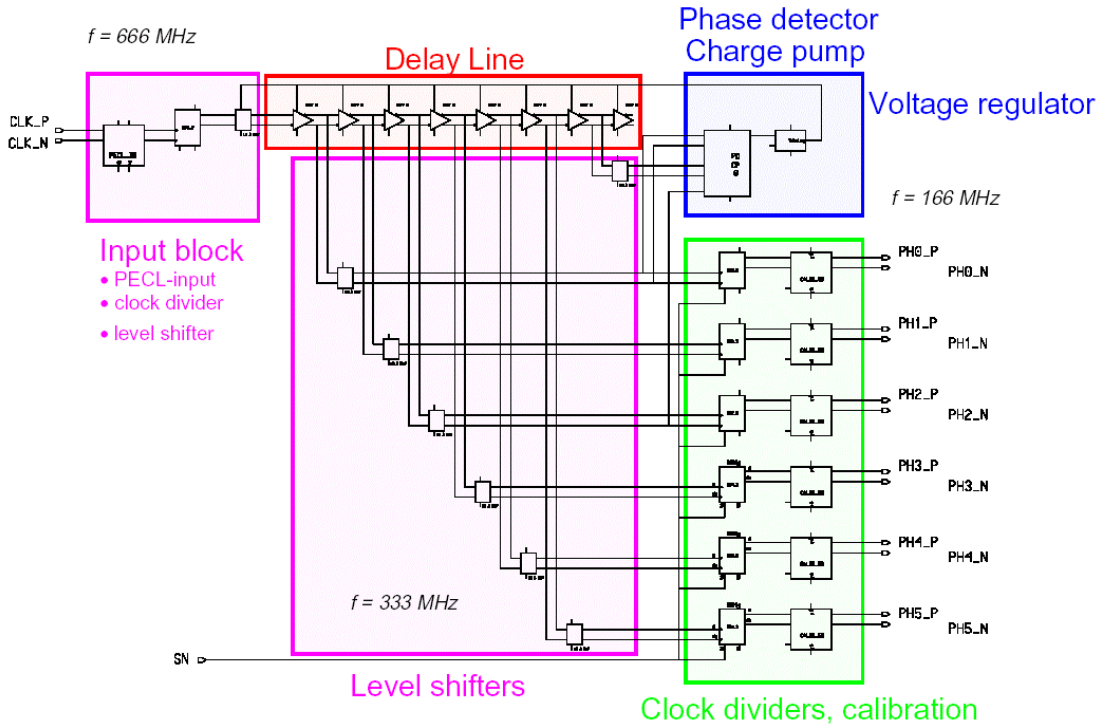
- Digitally controlled delay adjustment circuits after the clock division
  - Coarse adjustment required before division
- Skew calibration with PC
- Possible skew measurement strategies
  - Phase difference with inverse FFT
  - Phase difference from sine-fit test
  - In time domain from a ramp input signal to ADC

Clock Generator (1)

- A combined divider and delay-locked loop (DLL) clock generator
- Supply controlled delay elements (cross-coupled inverters)
- Digital counters at the output of the DLL provides 12 evenly spaced phases
- A skew calibration is applied to the output phases

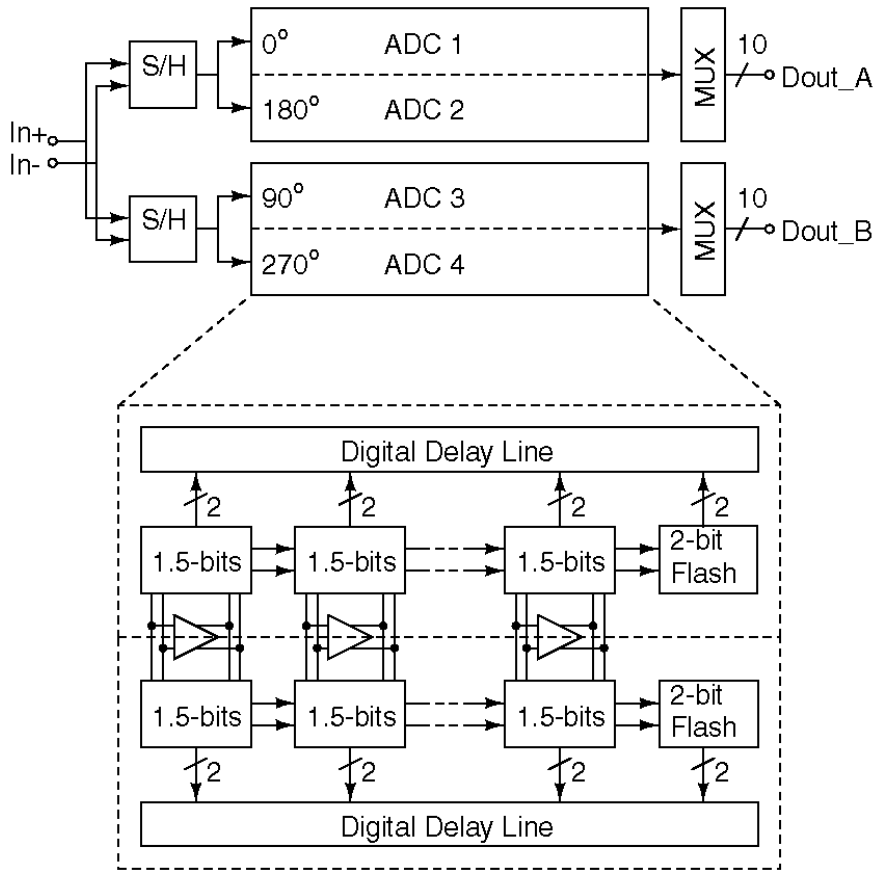
Clock Generator (2)

- A high frequency external clock is phased with a short DLL
- Clock phases detected by Edge Compiner
- Output spectrum is analyzed to find out the best calibration code

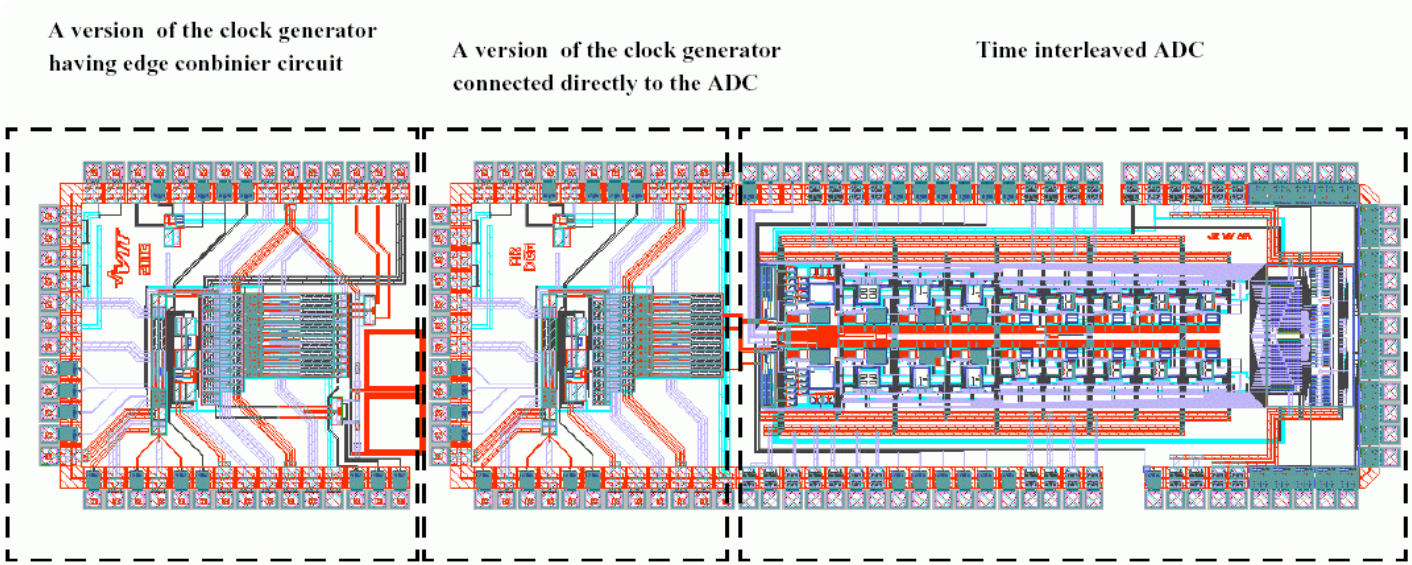


Specifications -Phase 1 Test Chip

- Sampling frequency
  - Single channel : 75-100 MS/s
  - Number of channels : 4
  - Total : 300-400 MS/s
- Resolution
  - Stage : 1.5 bits+ 2 bits (flash)
  - Number of stages : 8+1
  - Total : 10 bits
- Test DLL Blocks
  - Driving ADC
  - Jitter determination

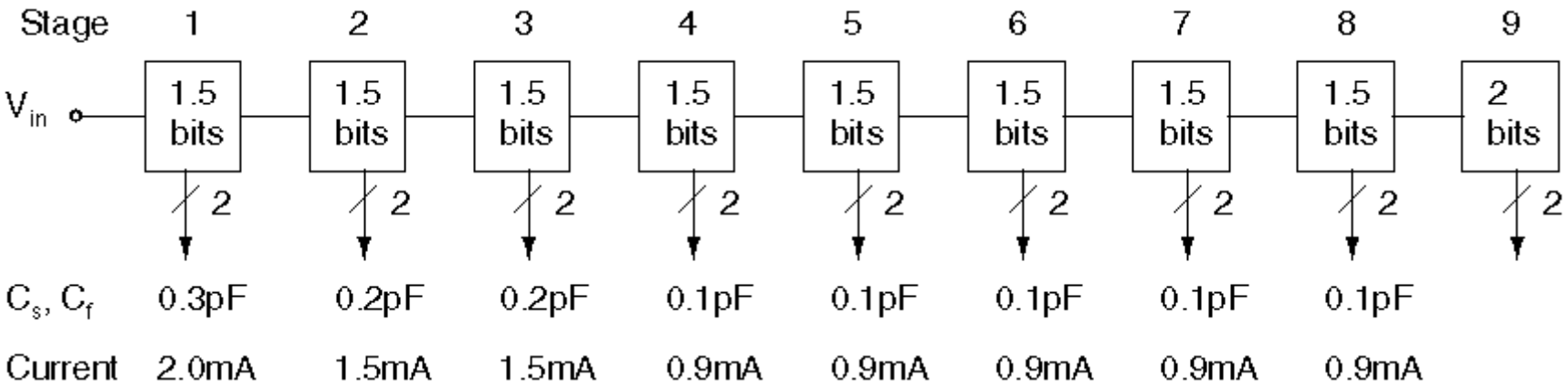


Layout Phase 1Test Chip



- Two skew-insensitive double-sampled ADC fingers
- Test DLLs
- Area: 1.7 x 6.8 mm^2
- Sent to process June/03, Received Nov./03.
- Measurements running

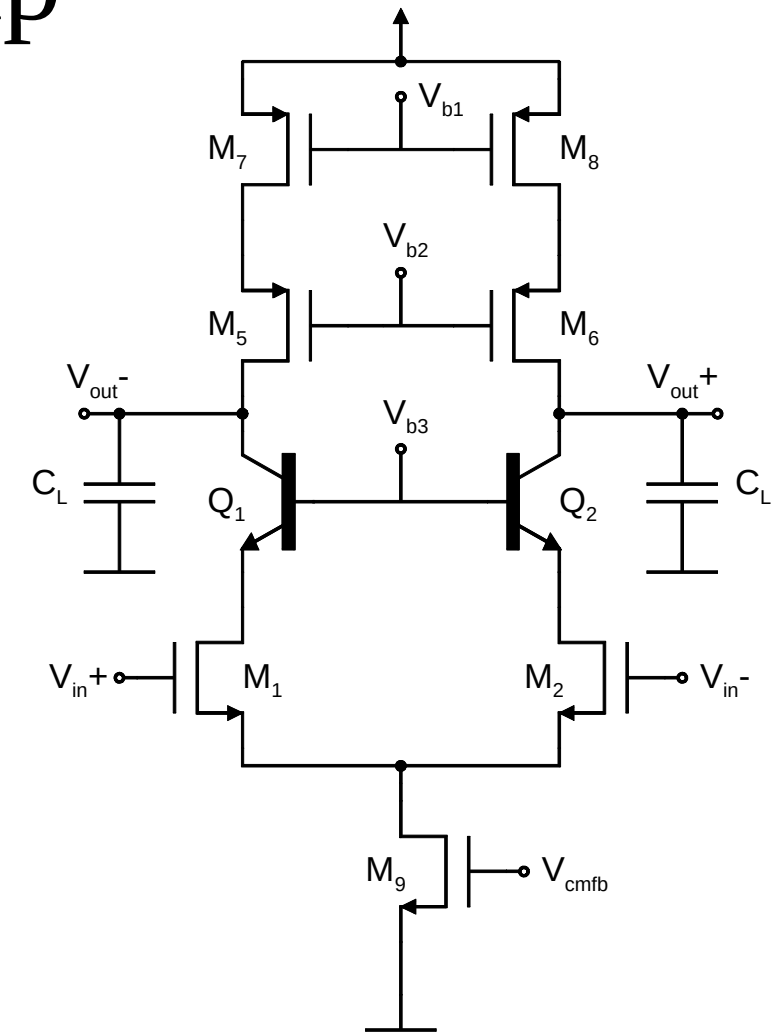
Channel ADC Phase 1



- Capacitors minimized
  - Lower power consumption but
  - Increased thermal noise
- Input bandwidth 500MHz ⇒ S/H circuit needed

OpAmp

- BiCMOS telescopic OTA
- Relative low current consumption (max 2mA)
- Bipolars used to achieve enough gain
- Pure CMOS requires two stage OpAmp

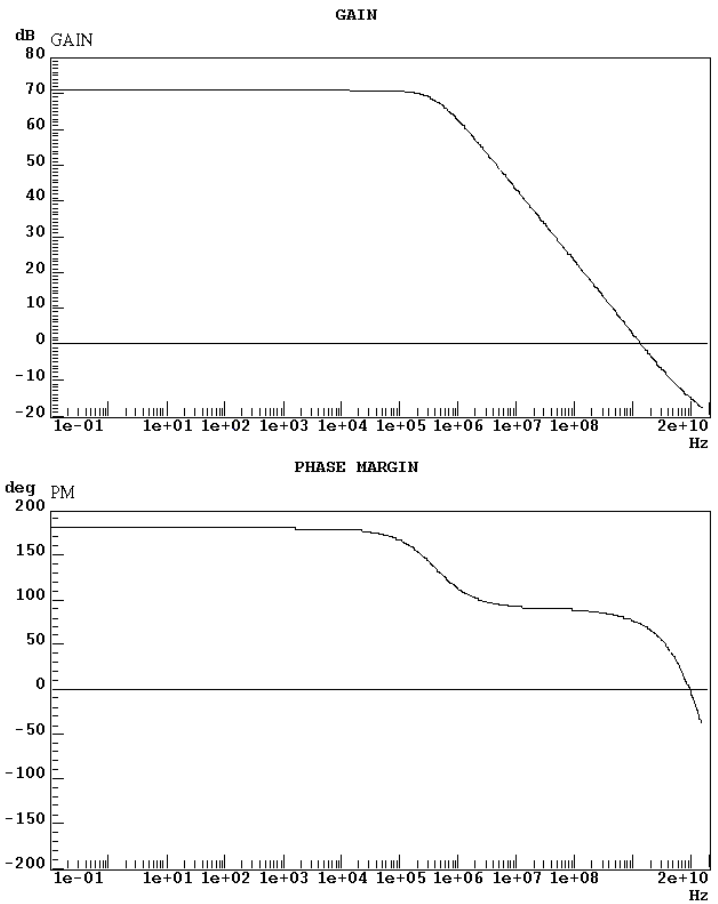


Simulations

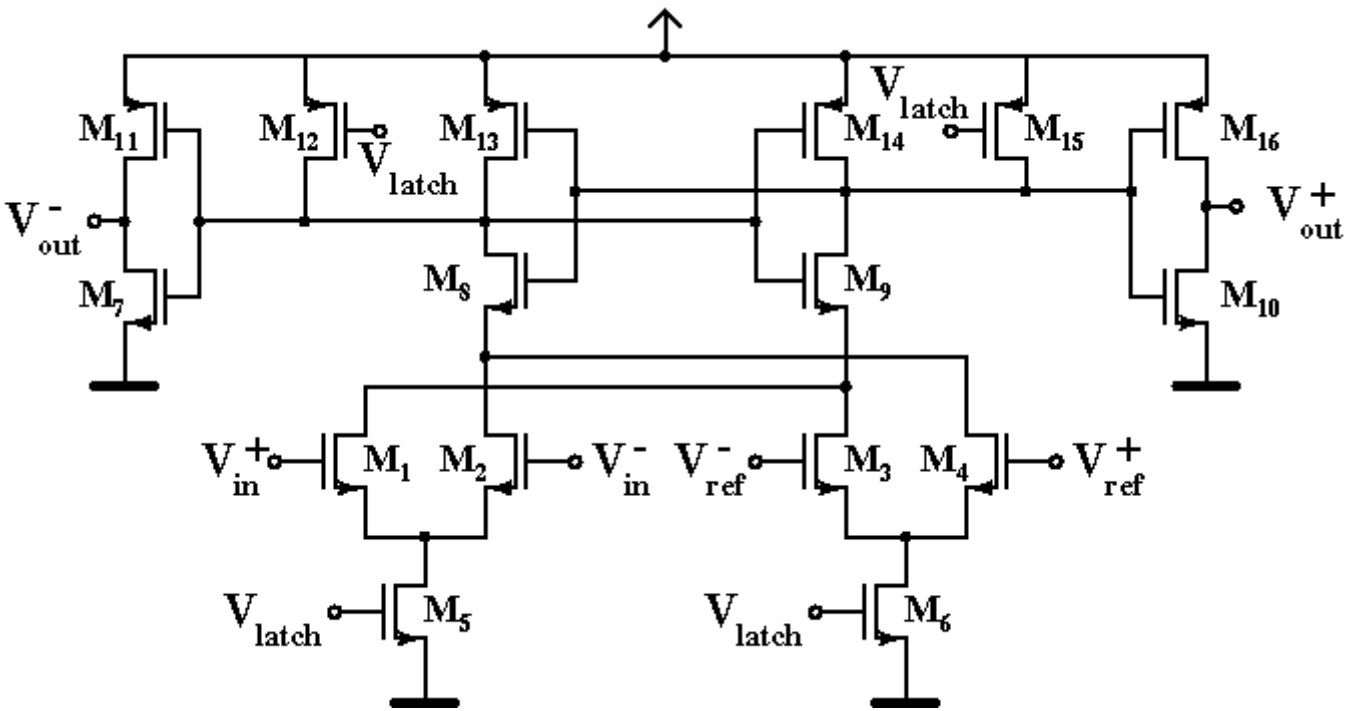
OpAmp

- 1st stage OpAmp

A_0	71 dB
GBW	1385 MHz
$V_{in,pp}$	0.5V
PM	72.4^o

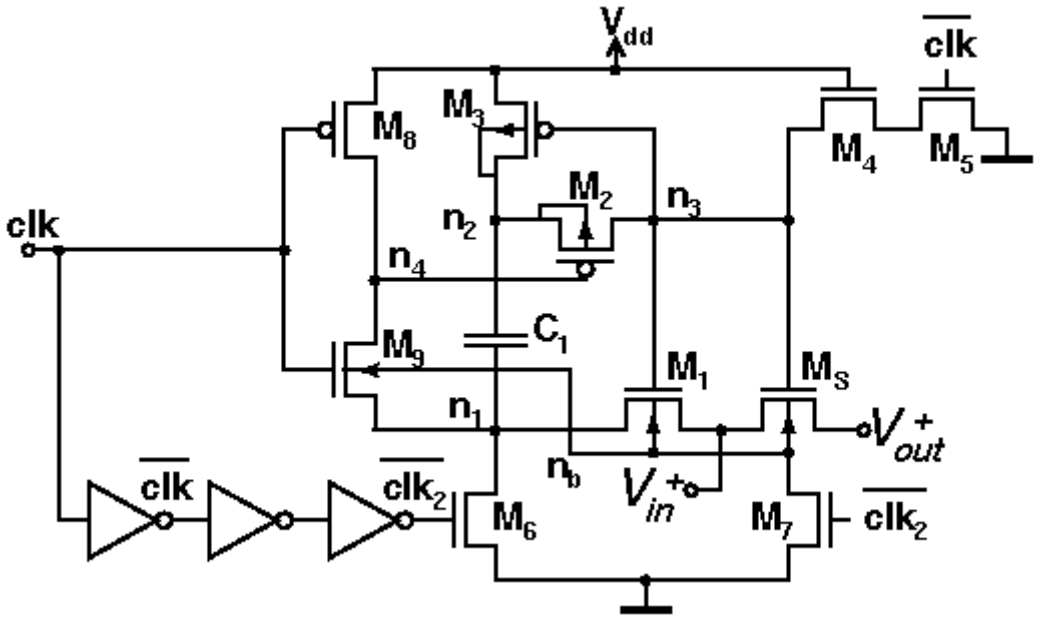


Dynamic Comparator



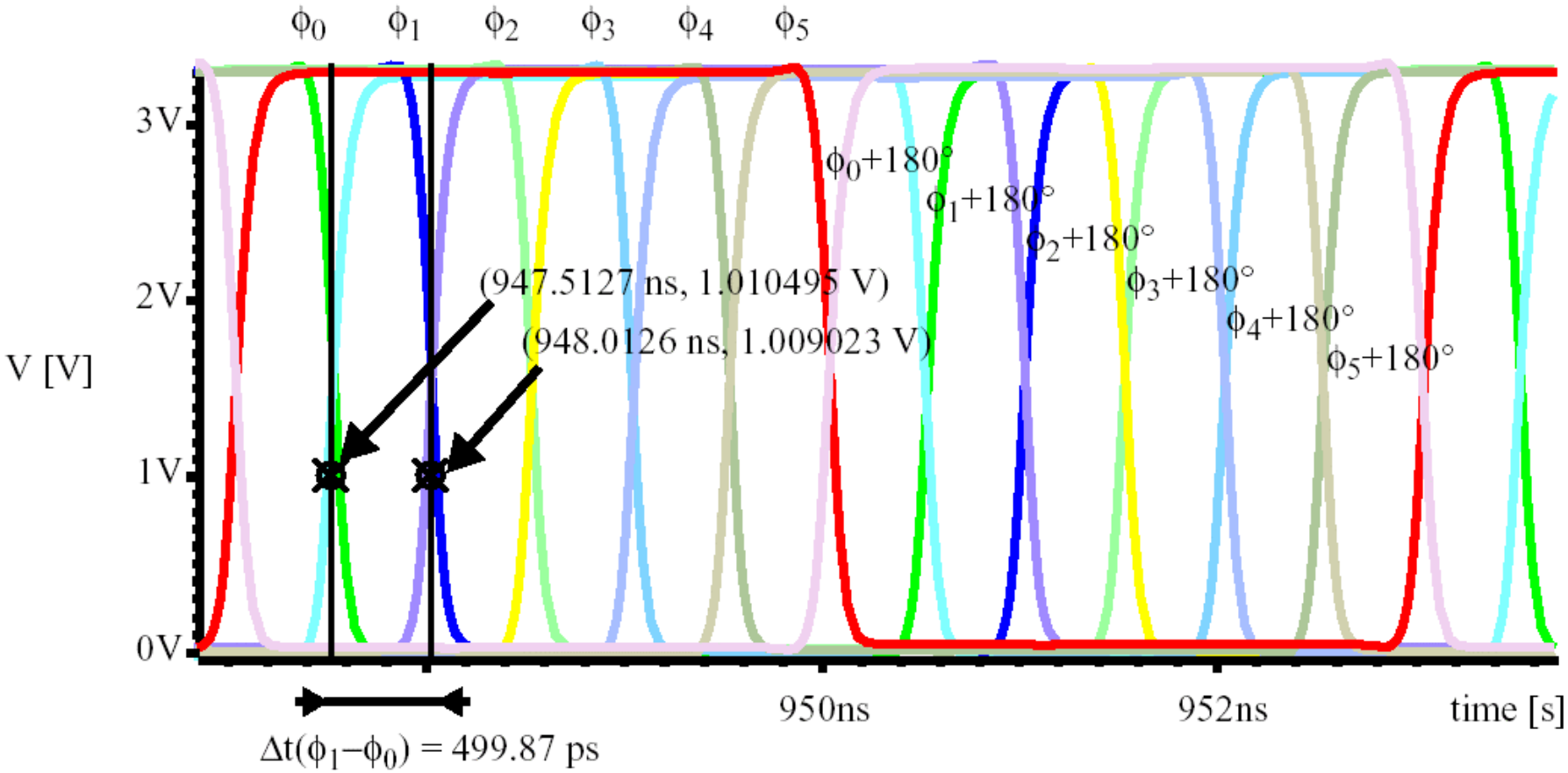
Bootstrapped Input Switch

- Insensitive to input voltage amplitude
- Used in first stage as sampling switch



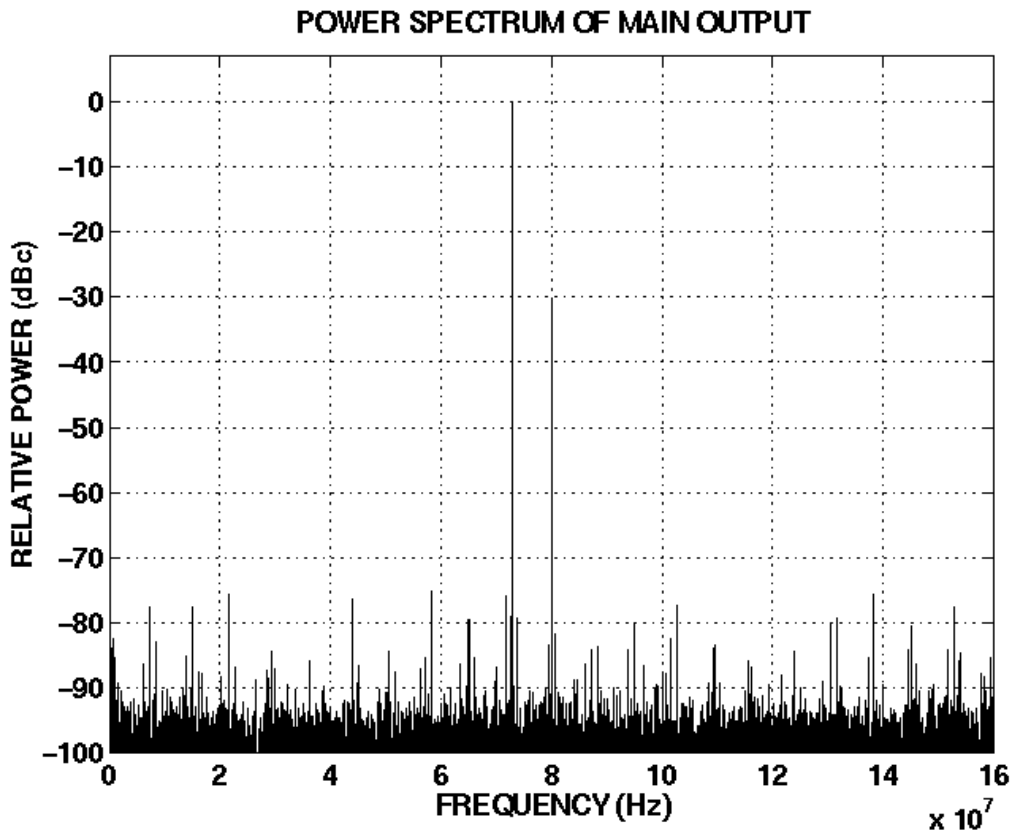
Simulations

Clock generator



Simulations

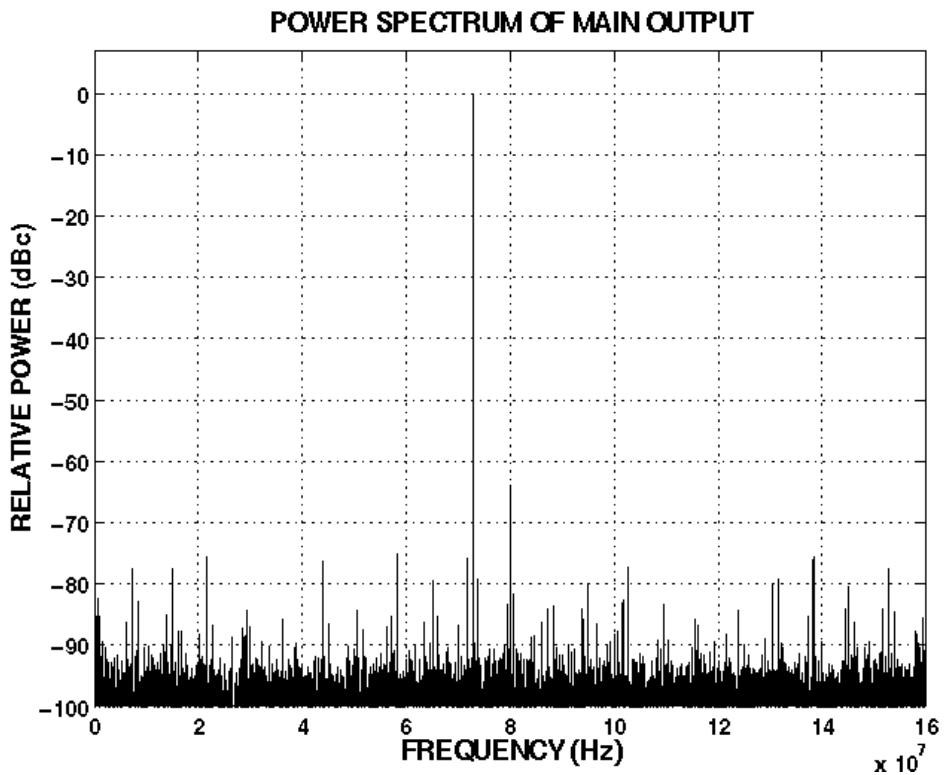
Uncalibrated 4-Channel



f_{in}	72.8 MHz
f_{clk}	80 MHz
f_{tot}	360 MHz
SFDR	30.5 dB
SNDR	30.5 dB
ENOB	4.8 bits

Simulations

Calibrated 4-Channel



f_{in}	72.8 MHz
f_{clk}	80 MHz
f_{tot}	360 MHz
SFDR	64.1 dB
SNDR	57.1 dB
ENOB	9.1 bits

Simulations

Summary

	Behavioral		Transistor level			
	4-chan uncalib.	4-chan calib.	1st 1.5-bit	Channel ADC	Channel Pair	Input Switch
f_{in}	72.8 MHz	72.8 MHz	9.1 MHz	9.1 MHz	9.1 MHz	913 MHz
f_{clk}	80 MHz	80 MHz	80 MHz	80 MHz	80 MHz	100 MHz
SFDR	30.5 dB	64.1 dB	72 dB	64 dB	63.5 dB	81 dB
SNDR	30.5 dB	57.1 dB		56.5 dB	56.5 dB	
ENOB	4.8 bits	9.1 bits		9.1 bits	9.1 bits	
$V_{in,pp}$	-1 dBFS	-1 dBFS	0.5 V	0.5 V	0.5 V	0.5 V

Drawbacks

- MPW runs of current BiCMOS 0.35 µm-process stopped => Forced to change vendor
- Problems with PCBs => Measurements delayed
- New test chip to process 4/2004
- Target tape out of final version moved to 11/2004