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date/*date*	02-April-2004	ref./*réf.* TOS-EDM/005.04/RW	page/*page* 1 / 12
from/*de*	Roland Weigand	visa/*visa*	
to/*à*	Public Distribution to LEONUMC Users	copy/*copie*	

Subject/*objet* **LEONUMC-Datasheet**

Introduction

LEONUMC has been developed as a test- and prototype-chip, and no self-contained datasheet has been edited. As the chip was developed from existing IP-cores, the present document references the IP-documentation, while giving additional information concerning their configuration and other issues, which are not covered by the existing documents.

References

All references are posted at the following WWW location:
http://www.estec.esa.int/microelectronics/leon/leonumc-datasheet.zip

RD1 LEON2 User's Manual (*leon2-1.0.4-configured.pdf*): This manual describes the functionality of the LEON2 v-1.0.4 model as configured for manufacturing on the Atmel ATC25 process, in the frame of the ESA LEON development.

RD2 PCI Interface for LEONUMC (*pci4leonumc.pdf*, issue 3-leonumc): This document describes the PCI functionality of LEONUMC.

RD3 LEON-PCI Verification Study, GR-TECH-021, Issue 1.3, Gaisler Research, February 2003 (*pcival-1.3.pdf*)

RD4 PGA299 Package drawing (*PGA_299_page_[1|2|3].pdf*)

RD5 Bonding diagram (*LEON_PCI_PACK_FLAT.pdf*)

RD6 LEON-PCI-UMC Development Board Test Report, rev 1.2, Gaisler Research Pender Electronic Design (*LEONUMC-seu-report-1.2.pdf*)

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Functional Description

The block diagram of LEONUMC is depicted in Figure 1. Detailed descriptions of the LEON blocks (i.e. all blocks except PCI) can be found in RD1. In this document, the choices made for some hard-configurable features (e.g. cache sizes, see the LEON Configuration Register in section 5.6) are indicated in brackets (). This configuration was selected for the Atmel-LEON implementation in July 2002. Please note that the specification of the Atmel component AT697 has evolved since then, and any users are invited to check carefully the differences, when using LEONUMC as a prototype for AT697. In particular the cache configuration has undergone modifications in size (going from 16 to 32 Kbytes instruction cache) and strategy (going from direct-mapped to multi-set cache), and the DSU trace buffer has been increased from 256 to 512 lines.

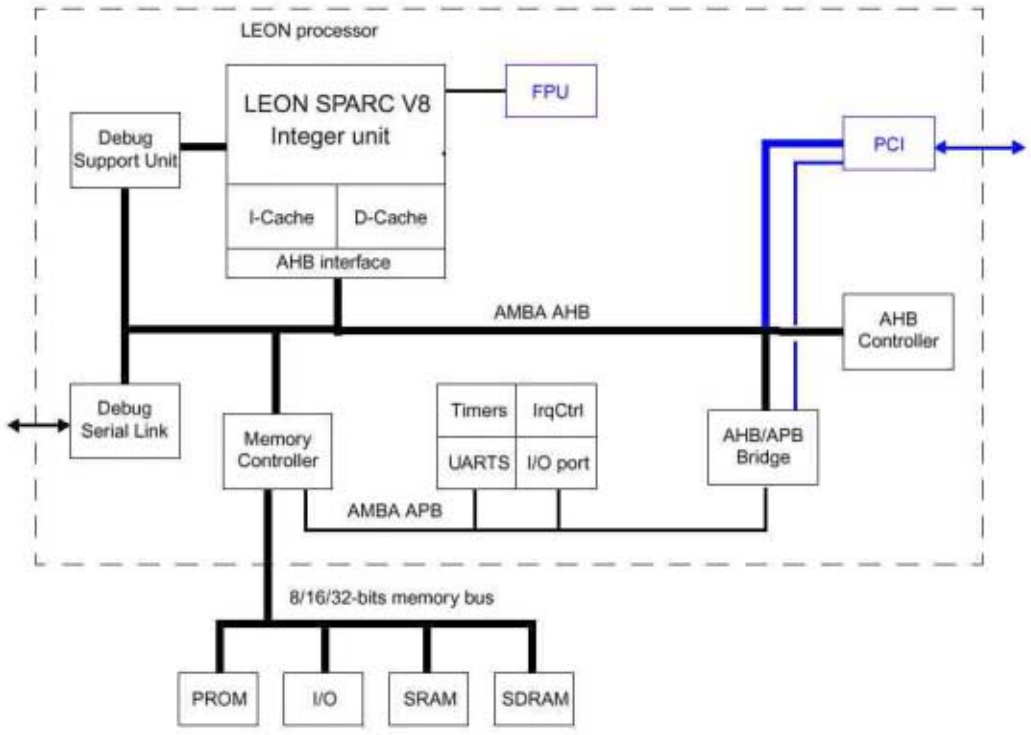

Figure 1 – Block diagram of the LEONUMC

LEONUMC implements the following deviations from RD1 and leon2ft-1.0.4:

- External address bus: has been reduced to 22 bits.
- Removed the SDRAM clock enable (sdcke pin)

- Master-checker logic is implemented for radiation tests. This is for radiation test purposes only, and in normal operation, the master input shall be tied to zero
- Additional pins for scan-test as described below in the pin-list
- PLL's on the LEON and PCI clock domains as described below
- Reset synchronisation as described below

The LEONUMC implements a PCI bridge as depicted in Figure 2. Based on the PCI core from InSilicon (now Synopsys), it provides LEON with a memory-mapped PCI-initiator access (InitSlave), a DMA function for PCI requests from external PCI initiators (TargetMaster), and a DMA function which acts as a master/initiator on both, the internal AHB bus and the external PCI bus (InitMaster). The memory-mapped PCI interface is connected in LEON to the addresses 0xA0000000 – 0xFFFFFFFF, the complete space of the local AHB bus can be accessed through the DMA function.

Details of the PCI implementation including pin- and register list can be found in RD2. This document refers to non-public documentation (the original documents of the PCI core), however these are deemed not necessary in normal operation.

The chip also contains a PCI arbiter for up to 4 bus agents. This function and can be used independently of the PCI bridge itself, however, it is also documented in RD2.

Since tapeout of LEONUMC, the design of LEON and PCI (baseline for AT697) has evolved in certain points. Bugs as reported in RD3 have been fixed, and certain features modified. The most important points are given here:

- Added second memory base address register (BAR), default mapped to the DSU.
- Implemented both memory BAR's as '32-bit' types
- Removed the 'retry on read-parity error' feature in the PCI AHB slave (retry_perr bit in mas_rs is not available any more)
- Removed the 'undetermined length write burst' feature in the PCI AHB slave
- Generating AHB error on forbidden PCI loopback scenario
- Fixed the problems with the DMA reported in RD3.

Results of Verification/Validation activities including SEU test are in RD3 and RD6.

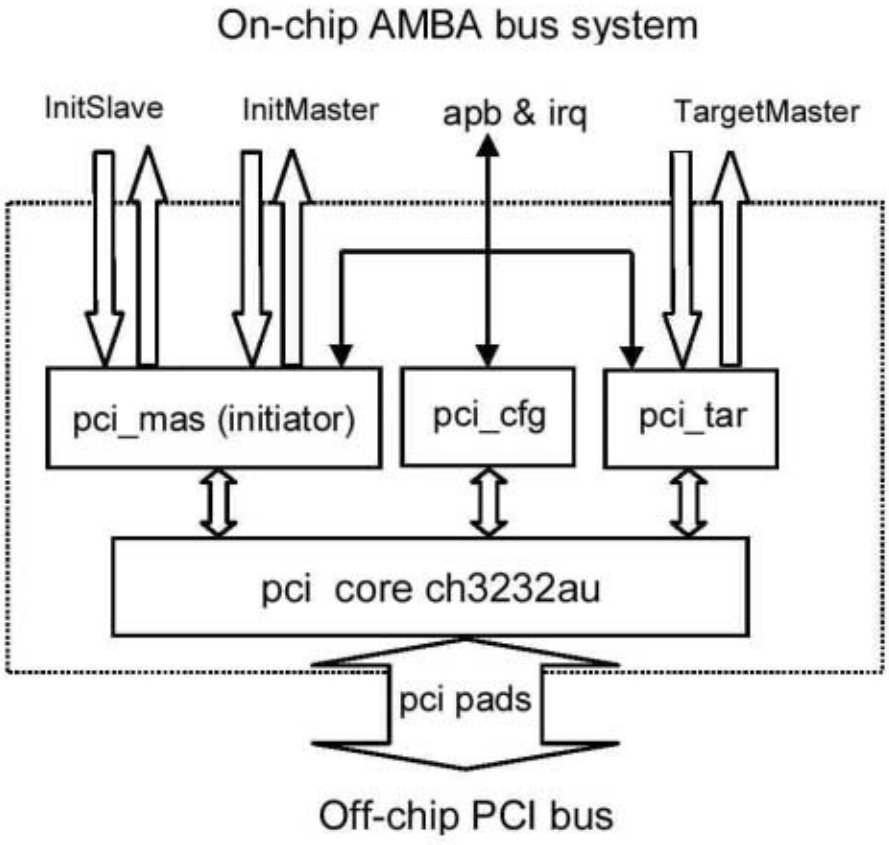

Figure 2 – Block diagram of the AMBA-PCI Bridge

Clocking and Reset

LEONUMC has two clock domains: The processor clock at pin *clk* and the PCI clock at pin *pci_clk_in*. Both clocks are equipped with a PLL. The processor PLL quadruples the clock, whereas the PCI PLL has a conversion ratio of one and serves to advance the phase of the PCI clock to relax the timing of the PCI signals. Both PLL can be disabled applying a logical 'high' level to their bypass inputs (*bypass_clk, byp_pci* respectively). The PLL's also have separate power pins. It is recommended to power the PLL's with the core voltage through an RC network as shown in Figure 3. This filter should be placed close to the PLL pins on the board. Note that vssa is connected internally, it does not have to be connected to the ground plane, and it should be used as ground net for the filter.

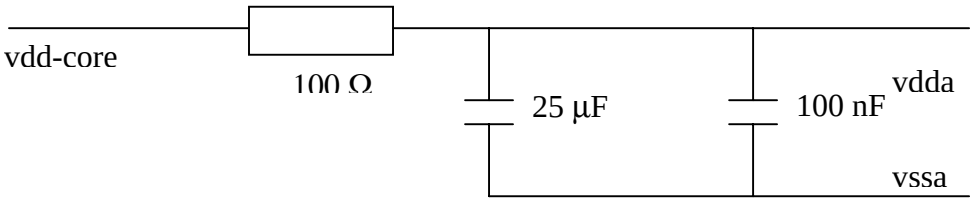

Figure 3 – Power filtering of the PLL supply

The circuit has two resets, one for the PCI-, and one for the processor clock domain. The rising edges of both resets are synchronised in their respective clock domains by the circuit in Figure 4. Please note, that the processor reset also resets the AMBA interface dedicated to the PCI (clocked by processor clock), and the PCI reset also resets some registers (in the synchronising FIFO's), which are clocked by the processor clock. This is not critical, assuming that there will be no PCI activity at release of reset. It is recommended to activate both resets together.

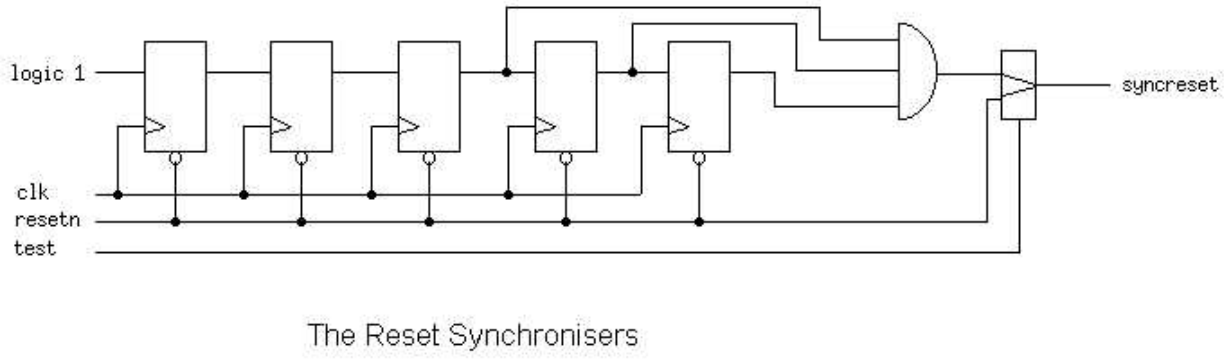

Figure 4 – Reset circuit implemented in LEONUMC

Operating Conditions

Parameter	**Recommended Value (min/max)**
Junction Temperature	25°C (0°C/125°C)
IO Supply Voltage at pins VDD-IO	3.3V (3.0V/3.6V)
Core Supply Voltage at pins VDD-CORE	1.8V (1.62V/1.98V)
PLL Analog Supply Voltage (VDDA)	1.8V (1.62V/1.98V)
Max. Processor Clock at pin clk	100 MHz (under nominal conditions)
Max. PCI Clock at pin pci_clk_in	33 MHz (under nominal conditions)
Power consumption	4.5 mW/MHz(clk) at 33MHz PCI clock

Table 1 – Address Space of LEONUMC

Registers and Memory Space

The memory space is allocated as in Table 2, and the registers are summarised in Table 3. For details, please refer to RD1 and RD2.

Address range	Size	Mapping
0x00000000 - 0x1FFFFFFF	512 M	Prom
0x20000000 - 0x3FFFFFFF	512 M	Memory bus I/O
0x40000000 - 0x7FFFFFFF	1 G	SRAM and/or SDRAM
0x80000000 - 0x8FFFFFFF	256 M	On-chip registers (see Table 3)
0x90000000 - 0x9FFFFFFF	256 M	Debug support unit
0xA0000000 - 0xFFFFFFFF	1.5 G	PCI interface

Table 2 – Address Space of LEONUMC

Address	Register	Address	Register
0x80000000	Memory configuration register 1	0x800000A0	I/O port input/output register
0x80000004	Memory configuration register 2	0x800000A4	I/O port direction register
0x80000008	Memory configuration register 3	0x800000A8	I/O port interrupt register
0x8000000C	AHB Failing address register	0x800000C4	DSU UART status register
0x80000010	AHB status register	0x800000C8	DSU UART control register
0x80000014	Cache control register	0x800000CC	DSU UART scaler register
0x80000018	Power-down register		
0x8000001C	Write protection register 1	**PCI Registers**	
0x80000020	Write protection register 2	0x80000100	device_id
0x80000024	LEON configuration register	0x80000104	status_command
0x80000040	Timer 1 counter register	0x80000108	class_revision
0x80000044	Timer 1 reload register	0x8000010C	bist_head_lat_cacheline
0x80000048	Timer 1 control register	0x80000110	mem_base_address
0x8000004C	Watchdog register	0x80000114	dac_address
0x80000050	Timer 2 counter register	0x80000118	iobar
0x80000054	Timer 2 reload register	0x8000012C	subsystem_id
0x80000058	Timer 2 control register	0x80000130	exp_rom_base_addr
0x80000060	Scaler counter register	0x80000134	cap_ptr
0x80000064	Scaler reload register	0x8000013C	latency_interrupt
0x80000070	Uart 1 data register	0x80000140	retry_trdy
0x80000074	Uart 1 status register	0x80000144	config_ben
0x80000078	Uart 1 control register	0x80000148	mas_address
0x8000007C	Uart 1 scaler register	0x80000150	mas_wc
0x80000080	Uart 2 data register	0x80000158	mas_rs
0x80000084	Uart 2 status register	0x8000015C	tar_pa
0x80000088	Uart 2 control register	0x80000160	tar_sc
0x8000008C	Uart 2 scaler register	0x80000164	int_en
0x80000090	Interrupt mask and priority register	0x80000168	int_st
0x80000094	Interrupt pending register	0x8000016C	int_test
0x80000098	Interrupt force register	0x80000178	dma_address
0x8000009C	Interrupt clear register	0X80000280	PCI Arbiter register

Table 3 – Registers of LEONUMC

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Pin List

This list gives the pinning of the chip. Relevant for board layout is the first column 'Array Coordinates'. Translation of chip, lead frame and array coordinates is according to the package and bonding diagrams in RD4 and RD5. For vectored ports, the first three columns contain the pins in the order 'Width-1 downto 0'. The pads selected from the eSi-Pad60 (60mm pad pitch) library from Virtual Silicon are CMOS/LVTTL pads operating at 3.3V, some of them with open drain. 5V-tolerant pads were used for the PCI bus.

(1) wdogn, errorn and pci_serr_n are open drain (O-OD) pads, and an external pull-up of 10 kOhm (TBC) is required. Rising edge of these pins may extend over several cycles.
(2) Pull-up required for these PCI signals, please refer to the PCI standard.
(3) Analog power supply for PLL, see above (Figure 3).

Array Coordinates (4)	Lead Frame Pin (4)	Chip (4)	Name	W	I/O	Pad Cell	Function	Act-ive
System interface signals								
T13	145	144	clk	1	IN	WC3I40	Processor clock input, internally multiplied by 4 by a PLL, if byp_clk = '0'	n.a.
U14	144	145	byp_clk	1	IN	WC3I40	Bypass PLL on clk: PLL is disabled, when byp_clk = ‘1’.	High
X15	146	147	resetn	1	IN	WC3I42	Processor clock reset	Low
T11	157	156	errorn	1	O-OD	WCD3B20T	System error (1)	Low
D10 B11 B12 B13 A14 C13 C12 B14 A15 E12 D13 E13 A16 C15 C16 D16	32 33 35 37 39 41 40 43 45 44 46 48 50 51 54 56	32 33 35 36 38 40 41 42 44 45 47 49 50 51 53 54	pio	16	IO	WC3B42	Parallel I/O port	n.a.
X13	158	158	wdogn	1	O-OD	WCD3B20T	Watchdog output (1)	Low
X14	152	153	dsuact	1	OUT	WC3O10	DSU active	High
W14	150	151	dsubre	1	IN	WC3I40	DSU break	High
V14	148	149	dsuen	1	IN	WC3I40	DSU enable	High

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Array Coordinates (4)	Lead Frame Pin (4)	Chip (4)	Name	W	I/O	Pad Cell	Function	Act-ive
U12	151	150	dsurx	1	IN	WC3I40	DSU link input	High
V12	153	152	dsutx	1	OUT	WC3O10	DSU link output	High
Memory bus signals								
W4 X4 V6 X5 W6 W7 T8 V8 U8 E5 E6 C3 E7 B3 C4 A5 B4 C6 B6 D7 A6 B7	184 182 180 179 178 174 175 172 173 2 4 1 8 3 5 12 9 13 14 15 16 19	182 181 180 179 178 175 174 173 172 1 2 4 5 6 8 9 11 13 14 15 17 18	address	22	O	WC3B40	Memory address	n.a.
U9	169	168	bexcn	1	IN	WC3I40	Bus exception	Low
W9	166	167	brdyn	1	IN	WC3I40	Bus ready strobe	Low
R4 U4 P5 U2 V2 U1 U3 T2 P3 N5 N4 P2 N3 M4 P1 M3 L2 K2 J2 H1 K3 J3 H3 J4 F1 F2 E1 D2 D3 E2 G4 B2	198 193 200 202 197 204 199 205 211 210 212 215 217 216 219 218 225 227 229 231 230 232 235 234 242 243 245 249 251 246 248 255	195 196 197 199 200 201 202 205 210 211 213 214 216 217 218 219 225 227 228 230 231 233 234 235 242 243 244 246 248 249 251 252	data	32	IO	WC3B40	Memory data	n.a.
A7 C8 E9 B8 A8 C9 C10 E10	21 23 22 25 27 26 28 30	20 22 23 24 26 27 29 31	cb	8	IO	WC3B40	Memory EDAC checkbits	n.a.
X7	170	171	iosn	1	O	WC3B20	I/O select	Low
V10	165	164	oen	1	O	WC3B20	PROM and I/O output enable	Low
W12 R2 L4 G3 F5	160 209 224 241 256	160 208 224 240 256	ramoen	5	O	WC3B20	SRAM output enable	Low

Array Coordinates (4)	Lead Frame Pin (4)	Chip (4)	Name	W	I/O	Pad Cell	Function	Act-ive
U11 T1 L5 H4 E4	159 207 222 238 254	159 207 223 239 255	ramsn	5	O	WC3B20	SRAM chip-select	Low
W8	168	169	read	1	O	WC3B20	Read strobe	High
W11 U10	162 161	163 161	romsn	2	O	WC3B20	PROM chip-select	Low
R3 M2 J5 G5	206 223 236 250	206 222 237 253	rwen	4	O	WC3B20	SRAM write enable	Low
W10	164	165	writen	1	O	WC3B20	PROM and I/O write enable	Low
V3	192	189	sdcasn	1	OUT	WC3O20	SDRAM column address strobe	Low
U13	147	146	sdclk	1	OUT	WC3O10	SDRAM clock output (after PLL)	n.a.
V4 W5	188 181	185 184	sdcsn	2	OUT	WC3O20	SDRAM chip-select	Low
R5 T5 T6 U6	196 194 191 189	194 193 192 191	sddqm	4	OUT	WC3O20	SDRAM data mask	Low
U7	185	188	sdrasn	1	OUT	WC3O20	SDRAM row address strobe	Low
W3	190	187	sdwen	1	OUT	WC3O20	SDRAM write enable	Low
PCI signals								
D14	57	60	pci_clk_in	1	IN	WC3I40	PCI clock, 33 MHz, internal phase adjustment by a PLL, if byp_pci = '0'	n.a.
D17	64	61	byp_pci	1	IN	WC3I40	A ‘1’ bypasses the 1xPLL on pci_clk	High
A17	53	56	pci_rst_in_n	1	IN	WC3I40	Asynchronous reset for the PCI clock domain	Low
E16 F16 F17 G16 C19 E18 E19 E17 G17 H16 F19 G18 J16 F20 G19 J18 M16 P20 N18 N16 P19 R20 R19 T20 T17 T19 T18 V19	66 68 70 72 67 74 76 71 79 81 80 82 85 84 86 89 107 106 108 111 110 112 114 115 122	65 66 67 69 70 71 73 74 79 80 81 83 84 85 87 88 106 107 109 110 111 113 114 115 119 120 122 123	pci_ad	32	IO	WC3B60T	PCI multiplexed address and data bus	n.a.

Array Coordinates (4)	Lead Frame Pin (4)	Chip (4)	Name	W	I/O	Pad Cell	Function	Act-ive
P17 V18 R17 R16	117 119 126 121 128 125 127	124 125 127 128						
D19 H18 N19 U19	73 88 104 120	75 89 105 118	pci_cbe_n	4	IO	WC3B60T	PCI command during address phase, active low byte enables during data phase	Low
K19	96	96	pci_devsel_n	1	IO	WC3B60T	Device Select: address hit in driving device (2)	Low
K16	93	92	pci_frame_n	1	IO	WC3B60T	Cycle Frame: low from address phase until one cycle before final data phase (2)	Low
E14	59	62	pci_gnt_in_n	1	IN	WC3I40	Bus Grant from arbiter, master access granted, not internally connected to the arbiter	Low
B18	60	57	pci_host	1	IN	WC3I40	'1' = host bridge, PCI config via APB, '0' = satellite, PCI config via PCI bus	High
E20	78	78	pci_idsel_in	1	IN	WC3I40	Initialisation Device Select: Chip select during configuration transactions	High
H19	92	93	pci_irdy_n	1	IO	WC3B60T	Initiator Ready: Low when initiator (master) is ready to transfer data (2)	Low
L16	99	98	pci_lock_n	1	IO	WC3B60T	Lock: I/O pad, but is always input (2)	Low
M18	103	102	pci_par	1	IO	WC3B60T	Even parity across ad and cbe_n. Valid one clock after the address/data phase	Even
L18	101	100	pci_perr_n	1	IO	WC3B60T	Data parity error: asserted 2 clocks after address/data (2)	Low

Array Coordinates (4)	Lead Frame Pin (4)	Chip (4)	Name	W	I/O	Pad Cell	Function	Act-ive
D15	61	63	pci_req_n	1	IO	WC3B60T	Bus Request, not internally connected to arbiter	Low
M19	100	101	pci_serr_n	1	IO-OD	WCD3B10T	Address Parity + System Error (1)	Low
L17	97	97	pci_stop_n	1	IO	WC3B60T	Stop (retry/abort/disconnect) current target is requesting the master to stop the transaction (2)	Low
J19	94	94	pci_trdy_n	1	IO	WC3B60T	Target Ready: Target is ready to accept (write) data or delivers (read) data (2)	Low
T14 U17 U15 T16	136 129 134 130	133 132 131 129	pci_arb_gnt_n	4	OUT	WC3O60	PCI arbiter grant	Low
W16 W18 W17 W19	140 133 138 131	137 136 135 134	pci_arb_req_n	4	IN	WC3I40	PCI arbiter request	Low
Test signals								
X16	141	141	master	1	IN	WC3I40	SEU test mode – tie to 0.	High
V13	154	155	cmperrn	1	OUT	WC3O20	Master-checker error – Ignore in normal operation mode	Low
U16	137	139	senable	1	IN	WC3I40	Scan shift enable – tie to 0.	High
V16	139	140	test	1	IN	WC3I40	Scan test enable – tie to 0.	High
Supply pins								
B16 C18 C5 C7 D11 D12 D20 D9 E3 F4 G1 J17 K17 K4 M17 M5 P18 T10 T15 T4 T7 U18 X6	52 65 10 17 34 42 75 24 247 252 237 87 95 226 105 214 113, 163 132 201 187 124 176	52 68 7 16 34 43 76 25 245 254 236 86 95, 226 104 215 112 162 130 203 190 121 177	v3io	23	VDD-IO	WVV3IO	3.3 V I/O supply	n.a.

Array Coordinates (4)	Lead Frame Pin (4)	Chip (4)	Name	W	I/O	Pad Cell	Function	Act-ive
B10 B15 B5 C11 C2 D18 D6 D8 E15 G20 H17 H2 H5 L19 N17 N2 P16 P4 T9 U20 U5 V11 W2	31 49 11 38 253 69 6 20 63 90 83 233 240 98 109 221 123 208 171 118 186 155 195	30 48 12 39 250 72 3 21 64 91 82 232 241 99 108 220 126 209 170 117 183 154 198	v0io	23	VSS-IO	WVV0IO	I/O round	n.a.
B9 C14 D5 F18 G2 L3 N20 T3 V17 V7 W13	29 47 7 77 239 220 102 203 135 177 156	28 46 10 77 238 221 103 204 138 176 157	vdd	11	VDD-CORE	WVVDD	1.8 V core supply	n.a.
A3 A9, A11, A13, A18 A20 C20 J20 L20 V20 X20 X18 X12 X10 X8 X2 W1 M1 K1 D1 B1			vdd				Package vdd (shielding), not directly connected to a die pad	n.a.
C17 E11 E8 F3 K18 K5 R1 R18 T12 V5 V9	58 36 18 244 91 228 213 116 149 183 167	55 37 19 247 90 229 212 116 148 186 166	vss	11	VSS-CORE	WVVSS	Core ground	n.a.
A2 A4 A10 A12 A19 B20 H20 K20 M20 W20 X19 X17 X11 X9 X3 X1 V1 N1 L1 J1 C1			vss				Package vss (shielding), not directly connected to a die pad	n.a.
D4	257		vss				Substrate connection (vss)	n.a.
B17	55	58	vssa1	1	VSSA	PLL_PCI	Filter for PCI PLL supply (3)	n.a.
B19	62	59	vdda1	1	VDDA	PLL_PCI	1.8 V core supply (3)	n.a.
V15	142	142	vssa2	1	VSSA	PLL_CLK	Filter for clk PLL supply (3)	n.a.
W15	143	143	vdda2	1	VDDA	PLL_CLK	1.8 V core supply (3)	n.a.