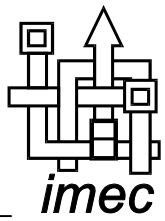

LEONUMC

Summary Report

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Document no.	:	P61285-IM-DL-004
Status	:	Issue 1.1
Date	:	18 May, 2004
ESTEC Contract	:	16201-02-NL-LVH

ESTEC Technical Management: Roland Weigand

European Space Agency
Contract Report

The work described in this report was done under ESA contract. Responsibility for the contents resides with the authors or organization preparing it.

Review list

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Document history record

issue	Date	description of change
1.0	10-06-2003	First version
1.1	18-05-2004	- Wording: “Clock skew problems” changed into “hold time violations” - Added temperature and frequency test results - Reduced sizes of pictures, to get a smaller document

Table of contents

Purpose

This document describes the overall LEONUMC project.

List of figures

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List of abbreviations

ATPG	: Automatic Test Pattern Generation
CMOS	: Complementary Metal Oxide Semiconductor
CTS	: Clock Tree Synthesis
ESTEC	: European Space Research & Technology Centre
GDSII	: Graphical Data Stream
I/O	: Input and output
P&R	: Place & Route
PG	: Power and Ground
PLL	: Phase-Locked Loop
RAM	: Random Access Memory
SEU	: Single Event Upset
TDF	: Top Design Format
TMR	: Triple Module Redundancy
UMC	: United Micro-electronic Cooperation
VST	: Virtual Silicon Technologies
μm	: micrometer

1 LEONUMC project overview

To generate a layout of the LEON_PCI design the following back-end work was performed:

- Scan chain insertion (by Imec);
- Scan Test vector generation (by Imec);
- Verilog to GDSII layout generation using Synopsys (former Avant!) Apollo software (by Imec), including Clock Tree synthesis (CTS);
- Parasitic extraction (by Imec);;
- Post-layout timing checks, simulation and timing sign-off, functional and test modes (by Estec)
- Electrical Rule Check (ERC), Design Rule Check (DRC), Layout Versus Schematic (LVS) check, Substrate - & Antenna checks;
- Manufacturing (via Imec-Europractice at UMC, Taiwan in a shuttle run);
- Test (via Imec- Europractice at Microtest, Italy).

The leon_pci design uses standard cells and I/O cells of the libraries of Virtual Silicon Technologies (VST) and was be processed in the UMC 0.18 μm CMOS technology. It was packaged in a CPGA 299, with a relatively small cavity size (shorter bonding wires).

The initial information handover went through some iteration. This is what we typically see with first-time use for the Imec place & route service. Some of the problems are due to Synopsys Design Compiler quirks, some are due to design style or some place & route flow details that the customer is unaware of. A typical example is the clocking structure supported for clock tree synthesis (CTS).

2 LEONUMC features

Libraries used (VST libraries available at no charge via Imec- Europractice)	
Core library	UMCL18U250T2_2.4
IO library	UMCL18U350T2_1.1
RAM libraries (one for each master)	UMCL18U410T2_1.2 for R128X32M4
	UMCL18U410T2_1.2 for R2048X34M8
	UMCL18U410T2_1.2 for R256X29M4
	UMCL18U420T2_1.3 for RF168X39M1
PLL library	UMCL18U800T2_2.1 for both PLLs
Design Statistics:	
Pad/Core Limited	Pad limited
Number of macro cells:	14
Number of module cells:	90456
Number of IO cells:	254
Number of bondpads:	256
Number of nets:	91673
Number of PLLs	2
Number of RAMs	14
Number of clock domains	2 x 3 (TMR)
Number of synthesized non-clock high-fanout nets	1
Number of supply pins	V3IO and V0IO, 23 of each VDD and VSS, 11 of each
Chip Utilisation*:*	
Total macro cell area:	2180018.71 μm²
Total standard cell area:	3552696.10 μm²
Total pad cell area:	2726800.00 μm²
Core size:	2679.60 μm by 2679.60 μm
Chip size:	4312 μm by 4312 μm
Number of equivalent gates:	291.2 eq. Kgates
Number of transistors:	2565075
Number of standard cell instances	90456

Table 1: LEONUMC features

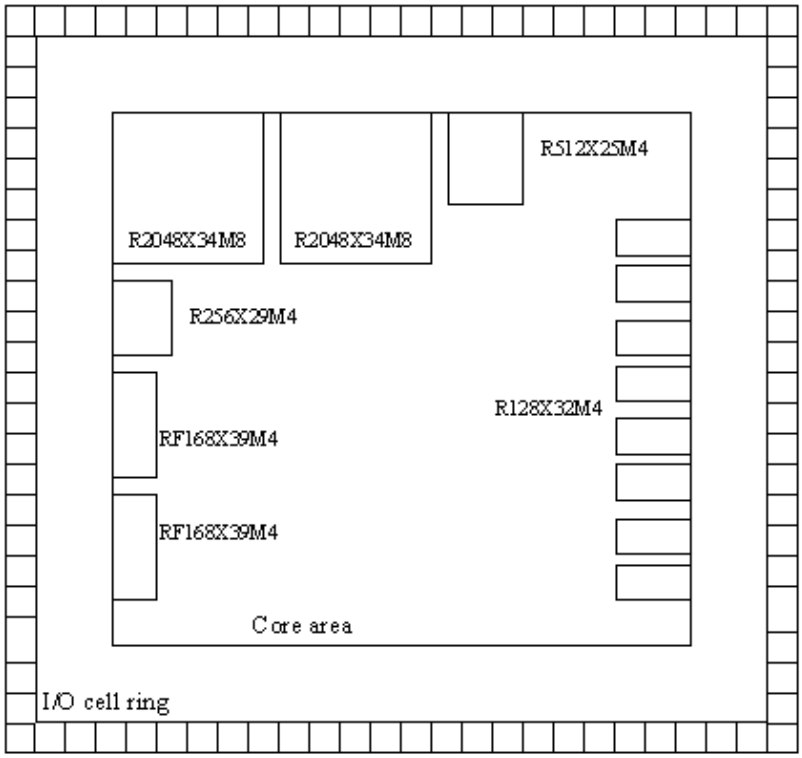

Figure 1: Floorplan

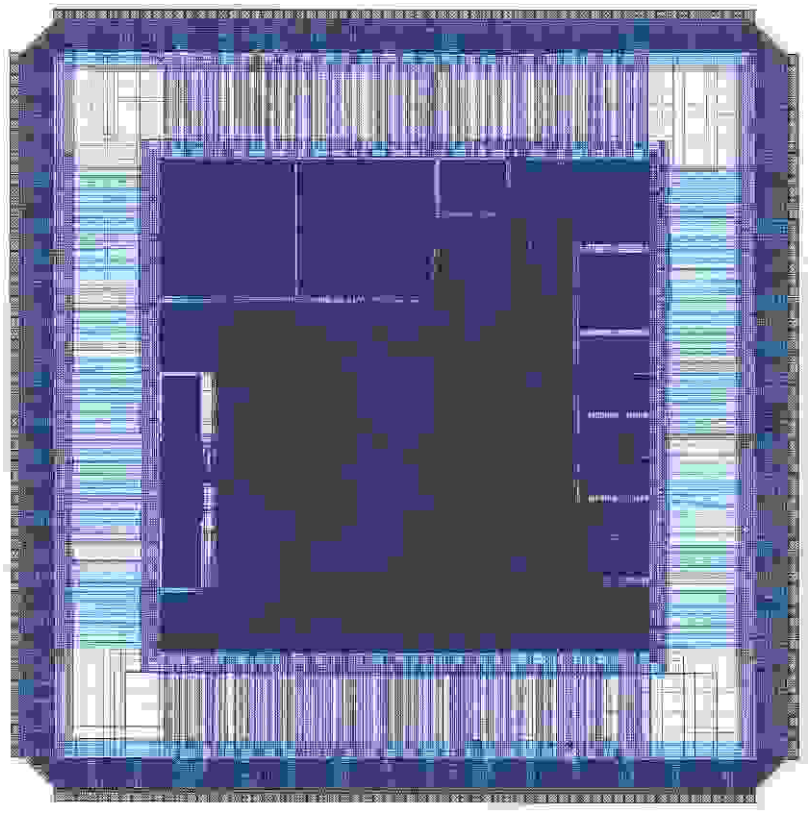

Figure 2: The layout

3 LEONUMC tests

The LEONUMC devices were tested with 3 sets of functional vectors using the load board depicted in Figure 3: Load board, front and Figure 4: Load board, back. Scan testing had to be abandoned due to hold time violations in the chains.
Frequency/Voltage Characterisation, Leakage current measurements and PLL output waveform measurements were also performed.
All in all 51 components were tested. 40 were functional.
A frequency versus supply voltage characterization of 3 samples showed correct operation up to 100 MHz at nominal supply voltage.
A temperature characterization (0, 25, 125 degrees Celsius) passed all test at low and ambient temperature whereas at high temperature, some current leakage failures were observed at high input level and voh-vol functional checks are failing due to slight variation of output levels.

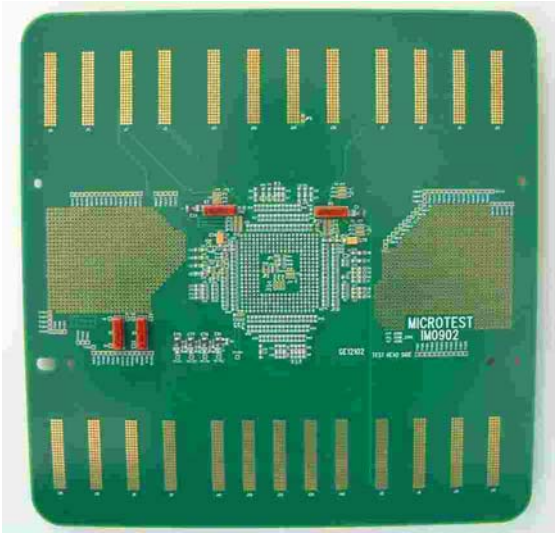

Figure 3: Load board, front

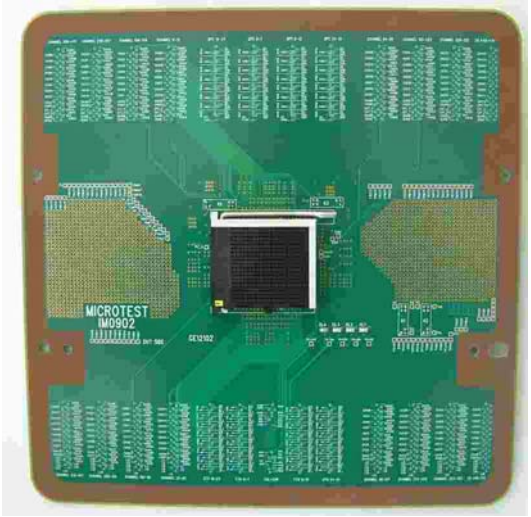

Figure 4: Load board, back