



**PENDER**  
ELECTRONIC DESIGN

# LEON-PCI-UMC Development Board

## Test Report

**GAISLER RESEARCH /  
PENDER ELECTRONIC DESIGN**  
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Gaisler Resarch

LEON-PCI-UMC Development Board Test Report

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## REVISION HISTORY

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1.0	2003- 10- 12	All	New document
1.1	2003- 12- 25		Update according ESTEC comments
1.2	2004- 04- 01		Re-pagination

## SUMMARY

An ASIC incorporating a LEON2-FT design has been designed by ESA-ESTEC and manufactured using the commercial UMC 0.18u process.

Samples of these devices were provided and Pender Electronic Design has developed and manufactured a development board with appropriate memory and interfaces to enable the demonstration and testing of these devices

This board has been used to demonstrate the operation of the ASIC, and in order to perform verification of the SEU performance of the LEON-FT logic implemented on the commercial UMC 0.18u process.

All ASICs provided were found to operate satisfactorily on the board at 100 MHz. One device was subjected to SEU Testing using the ESTEC Californium SEU Test equipment. Numerous SEU events were logged during the testing, including multiple events. All detected events were correctly detected and corrected by the FT logic inherent in the design, and no crashes or anomalous behavior of the device occurred. However, the device was found to be susceptible to latch-up.

Two recommendations are made. Firstly to enable the testing to be performed without manual intervention, the set-up should include a latch up detection and automatic recovery circuit to counter the latch-up condition. Secondly, testing of several of the devices from the batch rather than just a single device could be interesting in order to compare differences in behavior, if any.

# 1 INTRODUCTION

## 1.1 Overview

An ASIC incorporating a LEON2-FT design has been designed by ESA-ESTEC and manufactured using the commercial UMC 0.18u process. This ASIC incorporates a Meiko FPU unit and Insilicon PCI interface.

The LEON-FT design includes fault-tolerance features to withstand arbitrary single-event upset (SEU) errors without loss of data. The processor register file is protected using a 32-bit SEC/DED EDAC. The cache rams are protected using 2 parity bits/word. All remaining flip-flops and latches are configured in TMR (triple-modular redundancy) mode to correct any soft errors. The external memory interface incorporates a SEC/DEC EDAC.

The ASIC is implemented in a ceramic 299 pin grid array and targeted for 100 MHz operation.

Samples of these devices were provided, and Pender Electronic Design has developed and manufactured a development board (GR-PCI-UMC) with appropriate memory and interfaces to enable the demonstration and testing of these devices

This board has been used to demonstrate the operation of the ASIC, and in order to perform verification of the SEU performance of the LEON-FT logic implemented on the commercial UMC 0.18u process.

This report describes firstly the development board operation and the testing performed to demonstrate the operation and characteristics of the ASIC's, and secondly the SEU Testing with its corresponding results.

## 1.2 References

- RD-1 GR-PCI-UMC18\_user\_manual\_rev1-0.pdf, User Manual
- RD-2 GR-PCI-UMC18\_schematic\_rev1-0.pdf, Schematic
- RD-3 GR-PCI-UMC18\_assy\_drawing\_rev1-0.pdf, Assembly Drawings
- RD-4 GR-PCI-UMC18\_bom\_rev1-0.pdf, Bill of Materials
- RD-5 GR-PCI-UMC18\_pcb\_layout\_rev1-0.pdf, PCB Layout Drawings

## 2 BOARD DESIGN AND DEVICE TESTING

### 2.1 Board Design

The GR-PCI-UMC18 board design specially implemented for this ASIC, was adapted from the GR-PCI-XC2V design, and incorporates SDRAM, SRAM and FLASH memory, PIO and DSU interfaces.

The board is capable of operating stand-alone or as PCI plug-in card. The mechanical design of the board allows access to the die cavity to enable SEU/Radiation testing.

The board design and configuration is described in the User Manual, RD 1 and further detail information is given in documents RD 2 through RD 5. Photos of the board are provided in RD 1.

### 2.2 Device Testing

Ten ASIC devices were provided by ESTEC, and tested in combination with three GR-PCI-UMC boards. The ASIC devices were labeled with the serial numbers S/N 31 through 40. Testing of the operation of the devices was performed with a small suite of programs testing:

- RAM Test (SRAM and SDRAM pattern tests)
- PROM Test (Execution of program from Prom memory and boot operation)
- Applications (Stanford, Paranoia, Navigation application; testing of general operation and FPU performance)

Testing was performed at several clock frequencies (25, 33, 40 without internal PLL, and 100, 133, 160MHz with x4 internal PLL clock multiplier).

Testing was performed both in a stand-alone configuration, and installed in a PC. No testing of the board as a PCI Host in a passive backplane was performed as no suitable test infrastructure was available.

All devices operated at all tested frequencies up to and including 100 MHz, both stand-alone and as PCI plug-in cards. No devices were able to execute programs at any of the tested frequencies greater than 100 MHz (110, 120, 133, 160MHz), although simple communication and interrogation via the DSU interface was possible.

Although zero wait state operation of programs using the SRAM memory was perfectly feasible in most cases (all but one device operated at 100MHz, zero wait states without problems), bearing in mind the 15ns specified access time of the SRAM chips, one wait state for operation of programs out of SRAM is recommended.

Measurements of the operational current required by the board were made for all devices at several clock frequencies, as graphed in the following figure. This is the current measured at the input to the board, and includes both the quiescent and active current of the ASIC plus the current of the Memory/Peripherals.

Based on the above measurements, the calculated standby current of the board is estimated to be about 140 mA, while the current consumption of the Leon chip is about 2.5 mA/MHz. (equivalent to 4.5mW/MHz for 1.8V core voltage).

The Leon chip has very little difference between power-down and full load. Most extra current when running programs comes from the memory - a program with

100% cache hit (and no memory writes) only consumes about 10% more current than the power-down mode (even with a high FPU load). As the power consumption of the memories, being the main contributor to the device's power consumption, seems to depend on the clock frequency and is mostly independent of read/write cycles being performed, some attention should be paid to the design of memory power down modes for future designs.



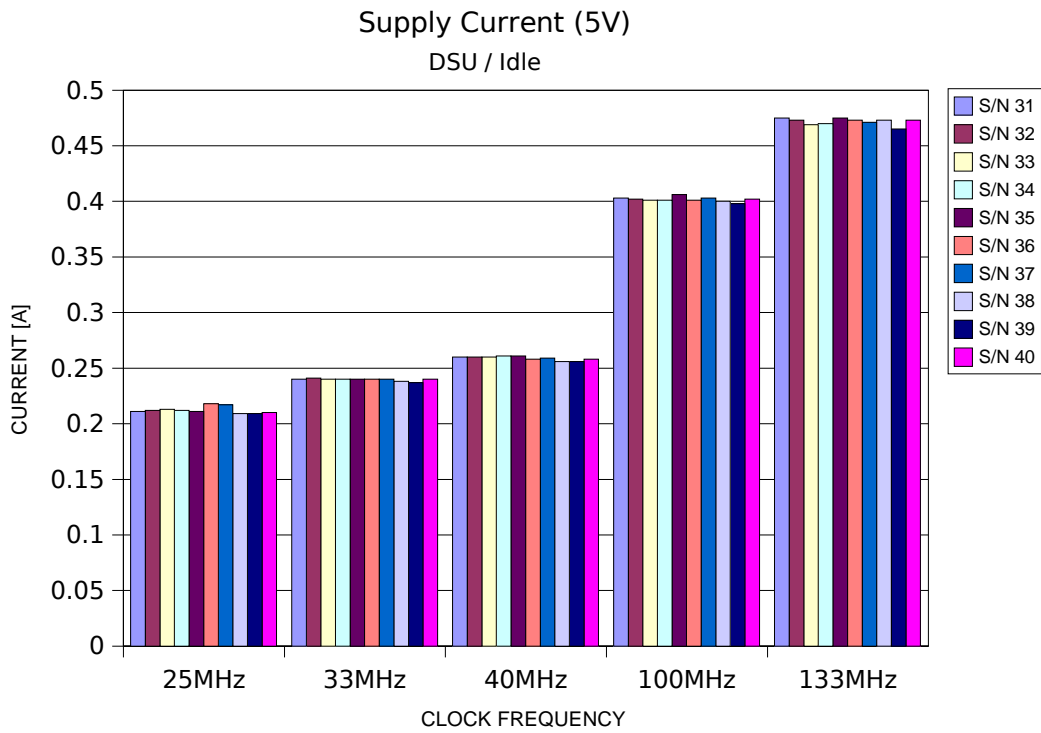


Figure 2- 1: Board Supply Current Versus Frequency (processor halted)

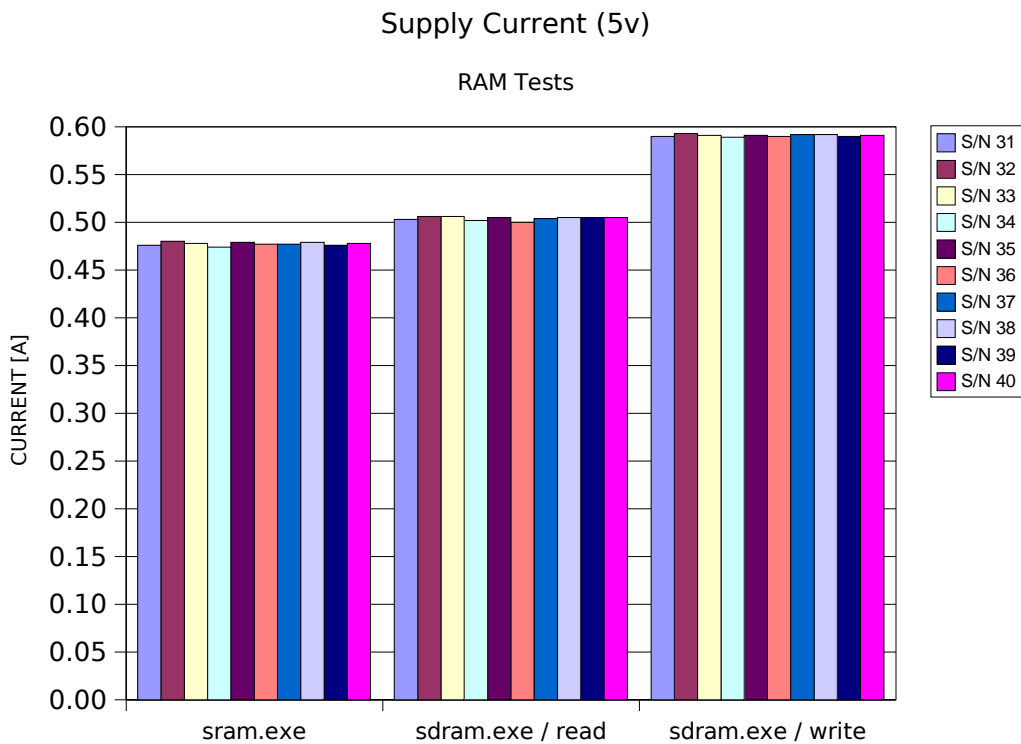


Figure 2-2: Board Supply Current versus Type of Memory access (100MHz)

## 3 SEU TESTING AND RESULTS

### 3.1 Test Set- Up

#### 3.1.1 Physical Test Set- up

The SEU Testing was performed using the ESTEC Californium (Cf-252) source and test set-up. The device must be de-lidded, and the die is exposed to the fission products emitted by a californium source. The testing must be performed under vacuum.

Board S/N 002 with ASIC S/N 032 were used for the SEU Testing.

The test equipment consists of the following items as shown in Figure 3- 1:

- Board with Device Under Test
- Vacuum Chamber and Vacuum pump
- Californium 252 radiation source
- Laptop for data logging
- Laboratory Power Supply
- Multimeter/Ammeter
- Assorted Cabling



Figure 3- 1: ESTEC Californium SEU Test Set-up

The UMC ASIC is packaged in a 299 pin Pin Grid Array, with the cavity on the bottom of the device. This requires that the design of the board incorporates an appropriate cut-out, and that the source irradiates from the 'bottom' of the PCB.

Additionally, as the chip is socketed, the resulting minimum distance to die is rather larger than would be preferred (at ca. 15mm). However satisfactory results were

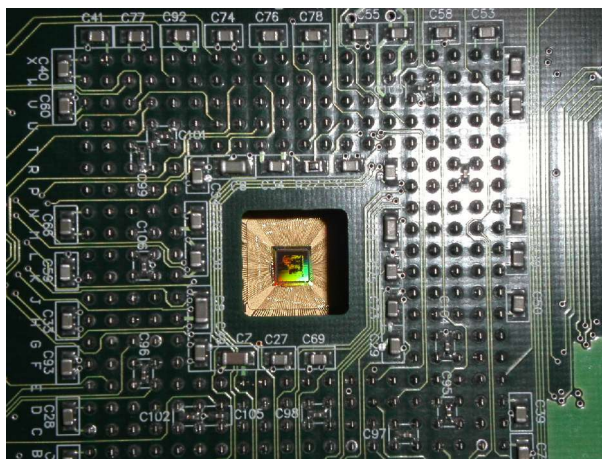


Figure 3- 2: View of exposed die through PCB cut-out

obtained with this configuration.

The Californium test source used was labeled as 480-87-1A with an indicated activity of 1.781uCi (27 April 1995). The corresponding flux was calculated to be 800 particles/cm<sup>2</sup>/min at 1.5cm distance. All testing was performed at normal incidence to the die. The mean LET value for all fission particles from the Cf source is given in literature as 43 MeV.mg<sup>-1</sup>.cm<sup>2</sup>

A vacuum in the pressure range  $1 \times 10^{-2}$  to  $6 \times 10^{-3}$  mBar (ca. 1 Pa) was achieved during testing.



Figure 3-3: Cf-252 source placement above die cavity

### 3.1.2 Test Software

Test software for the exercising of the processor and logging of the results was provided by Gaisler Research.

This software consists of two parts, a program stored in the Flash Prom of the Board Under Test, and a program installed on a laptop which logs the data and allows user control to start/stop tests.

Communication between the Laptop and Board Under Test is via a standard serial link.

The test suite running on the Board Under Test includes a small set of programs which can be test different aspects of the processor operation:

- IU Integer Unit test
- Paranoia runs the paranoia test program for floating point behavior. This program runs mainly from the caches
- GTB runs the a orbit navigation calculation software, requiring intensive calculation, and operating both from cache and using external memory.

When running, the programs continually loop, and at the end of each iteration the FT error count registers are read to determine the number of corrected errors which have occurred.

The results passed via the serial link to the laptop where they are displayed on the screen and logged to a text file for later review and analysis.

The number of correctable errors which have occurred and their location errors are indicated by the software as:

- ite => instruction cache tag errors
- ide => instruction cache data errors
- dte => data cache tag errors
- dde => data cache data errors
- rfe => register file error

An uncorrectable error will lead to an error trap occurring, and will be reported to the host by the target software. The board is then automatically reset and testing is resumed.

Each test program is self-checking, i.e. a checksum is calculated based on performed calculations and compared against a reference value after each pass of the program. An undetected SEU error can either lead to a checksum error or an unexpected trap. In both cases, the event is reported by the test software and the board is reset. The correctness of the software has been validated in earlier tests on the LEON1-FT device (2001), and also by deliberately inserting errors through the DSU interface.

Soft and Hard resets can be differentiated by the logging software.

A soft reset is indicated if either the software or the Watchdog timer has caused a reset of the board to be commanded.

A hard reset is indicated if the power to the board is manually cycled.

## 3.2 Test Results

### 3.2.1 Latch-up

Latch-up of the board as a result of the exposure to the Californium source was observed to occur approximately every 20 to 30 minutes of operation.

The input power supply for the board was limited to approximately 150% of the normal current (0.70A v's 0.45A), and the input current to the board and ASIC were therefore limited to this value.

A simple reset of the board was not sufficient to be able to recover the control, and the power to the board required to be cycled. After all these events, the board/ASIC was found to operate again without noticeable degradation after cycling the power to the board.

From the testing performed, it is not possible to identify the element(s) within the ASIC susceptible to the latch up.

The fact that the board stops operating is a result of the current limiting of the power supply, with the corresponding drop in input voltage, rather than the latch-up itself.

Considering the ASIC was able to draw 200mA additional current without damage, it would seem unlikely that the latch-up is occurring in a single element or circuit on the ASIC. Typically we might consider that the latch-up is occurring either in bulk to the substrate or perhaps on or at a pad element.

To try to eliminate the PLL circuit as a possible cause of the latch-up, additional tests of the device were performed with the PLL disabled (i.e. at 25MHz clock frequency). However, similar latch-up events were seen in this configuration. However, as the PLL remained powered during these subsequent tests, no real conclusion can be drawn with respect to this configuration.

Since a manual recovery from the latch-up condition was necessary, it was not possible to run the testing unattended. Unfortunately this reduced the total running time possible for collecting data during the testing.

For future testing, assuming the 'future' device is able to withstand without damage the latch-up condition, it is recommended to include a current detection and power interruption circuit to allow automatic recovery from the latch-up condition.

To localise the element(s) of the design susceptible to the latch-up, ESTEC has proposed to examine the ASIC device under the microscope to see if any change or damage due to the excess current is evidenced on the die.

### 3.2.2 Single Event Upsets

SEU testing was performed on a single device, S/N 032.

A number of test runs were performed, and the results logged as listed in Table 3-1.

Test runs were performed using IU, GTB and Paranoia test programs, and both using the clock PLL (100MHz operation) and without the PLL (25 MHz operation).

A total of 539 corrected errors were seen, distributed over the instruction cache, data cache and register file.

No uncorrected errors or unexplained crashes were detected.

As evidenced by the logs, a significant number of dual errors (51 times) and triple errors (22 times) occurred. These multiple events are indicated during a single loop of the test program, suggesting that they are multiple flips caused by single particle upset. This may suggest a susceptibility of the cache memories to multiple flips, which may or may not be a consequence of the physical structure and organisation of the register elements in the silicon design. It is also interesting that, despite these multiple flips, no uncorrectable errors were observed. This may be explainable taking account of the layout and organisation of the memory elements in the device. However, no information concerning the physical layout of the transistors in the design is available.

Based on the start and stop times for each test reported in the log files, an attempt has been made to calculate the observed software cross-section, as indicated in Table 3-2. However, as the number of observed errors (ca. 500) is relatively small, the statistical accuracy of these results cannot be considered to be very high.

The calculated average cross-sections are:

IU	0.0018 cm <sup>-2</sup>
GTB	0.0013 cm <sup>-2</sup>
PARANOIA	0.0008 cm <sup>-2</sup>

Test	Test Type	No. of runs	Corrected Errors	Error Location					Comment
				ite	ide	dte	dde	rfe	
Monday, 20 <sup>th</sup> October									
1	IU	268	0						System not under vacuum. No upsets.
2	IU	1661	0						System not under vacuum. No upsets.
3	IU	13984	15		9	1	3	2	
4	IU	365	2				2		
5	PARANOIADP	1049	0						
6	IU	985	1			1			
7	IU	13037	25	2	7	3	10	3	
8	IU	4446	7	1	2		4		
9	IU	0	0						Manual reset/Check
10	IU	0	0						Manual reset/Check
11	IU	0	0						Manual reset/Check
12	IU	0	0						Manual reset/Check
13	IU	0	0						Manual reset/Check
14	IU	854	0						Manual reset/Check
15	IU	1598	1				1		
16	IU	41060	54	3	17	1	33		
17	IU	297	0						
18	GTB	33	0						
Tuesday 21 <sup>st</sup> October									
19	GTB	7208	12	1	3		7	1	
20	IU	1341	1		1				
21	IU	17337	26		8	1	17		
22	GTB	582	27	3	6	4	13	1	
23	GTB	234	9	1	2	1	5		
24	GTB	618	26	1	16		9		
25	GTB	95	4		2		2		
26	GTB	206	9		3		5	1	
27	GTB	32	4		3	1			
28	GTB	442	22		9	1	12		
29	PARANOIADP	9396	1		1				
30	PARANOIADP	8553	10	1	4		2	3	
31	PARANOIADP	3326	2				2		
32	PARANOIADP	4055	3		2			1	
33	IU	615	2		2				Change to 25MHz clock (PLL switched off)
34	IU	8131	42		19	2	19	2	
35	IU	72	0						



Test	Test Type	No. of runs	Corrected Errors	Error Location					Comment
				ite	ide	dte	dde	rfe	
36	IU	1765	12	1	6		5		
37	GTB	13	5	1	2		2		
38	GTB	123	33	5	9	1	17	1	
39	GTB	0	0						
40	GTB	82	23		8	5	7	3	
Wednesday 22 <sup>nd</sup> October									
41	GTB	0	0						Manual reset
42	GTB	15	0						
43	IU	1575	7		2		4	1	
44	IU	3812	13		9		4		
45	IU	2388	7		3		4		
46	IU	1111	7		3	1	3		
47	IU	8166	43	5	15		23		
48	IU	5189	24	2	14	1	7		
49	IU	2330	5	1	2		2		
50	IU	2772	15		5		8	2	
51	IU	4580	23	3	10		10		
52	IU	457	1				1		
53	IU	3084	16	1	6		9		
TOTAL			539	32	210	24	252	21	

Table 3- 1: Summary of Errors detected during SEU Testing

Test	Test Type	No. of runs	Corrected Errors	Error Rate [s <sup>-1</sup> ]	Calculated Upset Cross-section [cm <sup>-2</sup> ]
1	IU	268	0	N/A	
2	IU	1661	0	N/A	
3	IU	13984	15	0.019	0.0014
4	IU	365	2	0.095	0.0072
5	PARANOIADP	1049	0	N/A	
6	IU	985	1	0.018	0.0014
7	IU	13037	25	0.034	0.0025
8	IU	4446	7	0.028	0.0021
9	IU	0	0	N/A	
10	IU	0	0	N/A	
11	IU	0	0	N/A	
12	IU	0	0	N/A	
13	IU	0	0	N/A	
14	IU	854	0	N/A	
15	IU	1598	1	0.011	0.0008
16	IU	41060	54	0.023	0.0018
17	IU	297	0	N/A	
18	GTB	33	0	N/A	
19	GTB	7208	12	0.029	0.0022
20	IU	1341	1	0.012	0.0009
21	IU	17337	26	0.027	0.0020
22	GTB	582	27	0.013	0.0010
23	GTB	234	9	0.011	0.0008
24	GTB	618	26	0.011	0.0009
25	GTB	95	4	0.011	0.0009
26	GTB	206	9	0.012	0.0009
27	GTB	32	4	0.031	0.0024
28	GTB	442	22	0.014	0.0010
29	PARANOIADP	9396	1	0.002	0.0002
30	PARANOIADP	8553	10	0.012	0.0009
31	PARANOIADP	3326	2	0.013	0.0010
32	PARANOIADP	4055	3	0.016	0.0012
33	IU	615	2	0.014	0.0011
34	IU	8131	42	0.023	0.0017
35	IU	72	0	N/A	
36	IU	1765	12	0.030	0.0022
37	GTB	13	5	0.024	0.0018
38	GTB	123	33	0.019	0.0014

Test	Test Type	No. of runs	Corrected Errors	Error Rate [s <sup>-1</sup> ]	Calculated Upset Cross-section [cm <sup>-2</sup> ]
39	GTB	0	0	N/A	
40	GTB	82	23	0.019	0.0015
41	GTB	0	0	N/A	
42	GTB	15	0	N/A	
43	IU	1575	7	0.019	0.0015
44	IU	3812	13	0.015	0.0011
45	IU	2388	7	0.013	0.0010
46	IU	1111	7	0.027	0.0020
47	IU	8166	43	0.023	0.0018
48	IU	5189	24	0.020	0.0015
49	IU	2330	5	0.009	0.0007
50	IU	2772	15	0.024	0.0018
51	IU	4580	23	0.022	0.0017
52	IU	457	1	0.009	0.0007
53	IU	3084	16	0.023	0.0017
TOTAL			539		

Table 3-2: Calculated upset cross-section per test run

## 4 CONCLUSIONS

All ASICs provided were found to operate satisfactorily on the development board at 100 MHz. One device (S/N 032) was subjected to SEU Testing using the ESTEC Californium SEU Test equipment. Numerous SEU events were logged during the testing, including multiple events. All detected events were correctly detected and corrected by the FT logic inherent in the design, and no crashes or anomalous behavior of the device occurred. However, the device was found to be susceptible to latch-up.

Since no anomalous behaviour was seen, it can be said that the TMR structures and Failure Tolerance implemented in the design are efficient in mitigating the radiation induced upsets.

Two aspects which remain undetermined are 1) a definite conclusion as to why although multiple errors were seen, no uncorrectable errors occurred, and 2) quantitative statements concerning the efficacy of the skewing of the TMR clock lines in to mitigate the effects of SET.

For the first point, it is possible that the physical layout of the cells within the memory sections of the device mitigate multiple effects, if the adjacent bits of words are not physically located close together.

Further designs meant to test the radiation behaviour of this technology should take into account the possibility to configure the skew between the clock branches in order to test the effectiveness of the SET behavior and mitigation.

Additionally, two recommendations concerning the testing are made. Firstly to enable the testing to be performed without manual intervention, the set-up should include a latch up detection and automatic recovery circuit to counter the latch-up condition. This would allow longer uninterrupted operation and correspondingly more measurements to be performed. Secondly, testing of several of the devices from the batch rather than just a single device could be interesting in order to compare differences in behavior, if any.

## 5 ABBREVIATIONS

DED	Double Error Detecting
DSU	Debug Support Unit
EDAC	Error Detection and Correction
ESA	European Space Agency
FPGA	Field Programmable Gate Array
FT	Fault Tolerant
LED	Light Emitting Diode
LGPL	Lesser GNU Public License
PC	Personal Computer
PCB	Printed Circuit Board
PIO	Parallel Input – Output
PLL	Phase Lock Loop
RD	Reference Document
SEC	Single Error Correcting
SET	Single Event Transients
SEU	Single Event Upsets
SMD	Surface Mounted Device
S/N	Serial Number
typ.	typical
UART	Universal Asynchronous Receiver – Transmitter