The most important thing we build is trust

ADVANCED ELECTRONIC SOLUTIONS | AVIATION SERVICES | COMMUNICATIONS AND CONNECTIVITY | MISSION SYSTEMS

GR740 Processor development

Magnus Hjorth, Cobham Gaisler AB

Space Engineering and Technology Final Presentation Days

24 May 2017

ESA/ESTEC, Noordwijk, Netherlands

COBHAM OFFICIAL SPONSOR

VOLVO OCEAN RACE ROUND THE WORLD

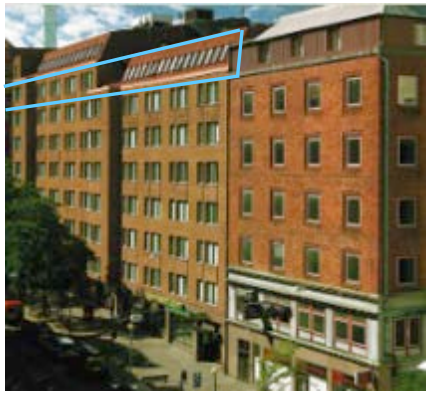
Presentation agenda

- Contents:
  - Brief company introduction
  - European processor background
  - Project overview
  - Work performed in project
  - Results and outputs
  - Related activities
  - Future work
  - Conclusions

Cobham Gaisler AB

Company presentation

- Located in Gothenburg, Sweden
- Fully owned subsidiary of Cobham plc
- Management team with 50 years combined experience in the space sector:
  - Sandi Habinc: General Manager
  - Per Danielsson: Senior Advisor
  - Jan Andersson: Director of Engineering
  - Arne Samuelsson: Proposal/Program Manager
- 25 employees with expertise within electronics, ASIC and software design
- Complete design facilities in-house for ASIC, FPGA and software design
- 9.2 M$ turnover in CY2016



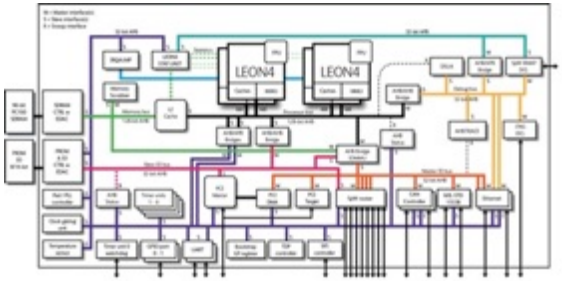
Cobham Gaisler LEON/SPARC history

- Company founded by original developer of the LEON/LEON2
- Now develops, markets LEON3(FT), LEON4(FT) and GRLIB IP library for commercial and space customers.
- Provides and maintains GRLIB-GPL open-source distribution of LEON3 and IP library.
- Software section develops and maintains tools, operating system ports, and drivers. Many contributions to open source projects (Linux, RTEMS, GCC).
- Acquired by Aeroflex (US), that was subsequently acquired by Cobham (UK)
  - LEON-related development is still done in Gothenburg, Sweden.
  - We provide tech support for Aeroflex UT699/UT700 processors

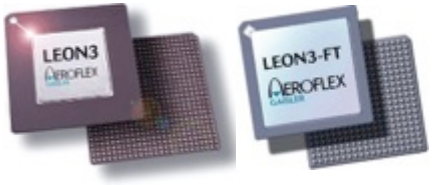
Cobham Gaisler Processor Solutions

One-Stop-Shop

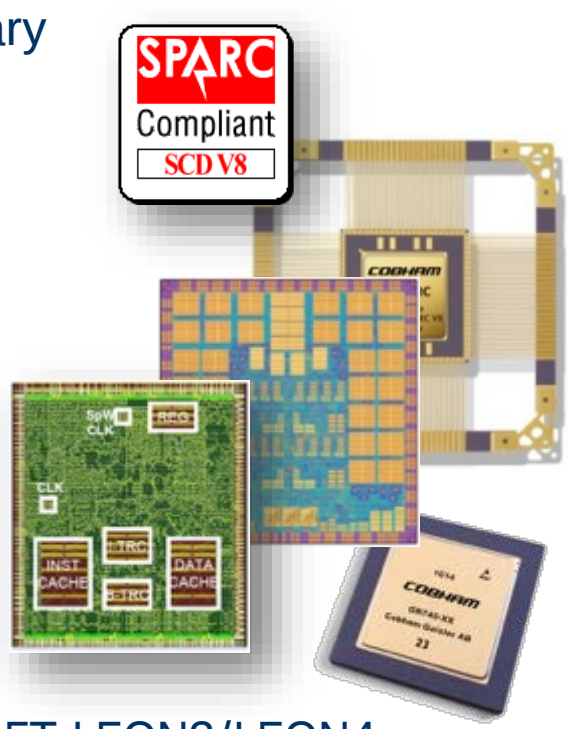
Synthesizable IP Core Library



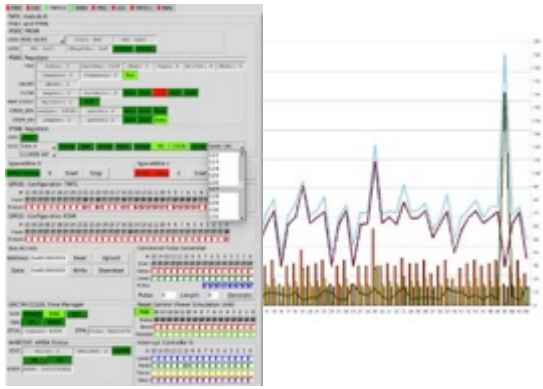
FT FPGA Processors



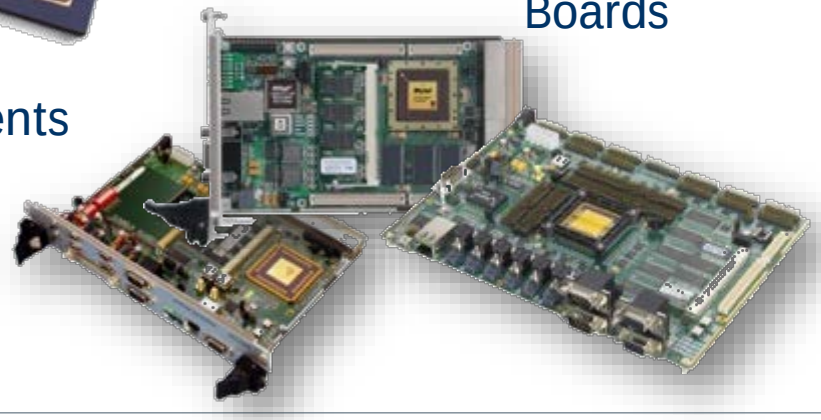
FT LEON3/LEON4 Processor Components



Simulators, Debuggers, Operating Systems, Compilers



Development Boards



System Testbeds

SPARC/LEON Processor Background

An open non-proprietary standard for space

- State of the European space market in 1990
  - 8-bit processors, like 80S32 and 8086
  - 16-bit RISC processors, like MIL-STD-1750, MDC281, MA31750
  - Motorola 68020, 32-bit CISC – Ariane 5 OBC (Launcher)
  - Intel 386, 32-bit CISC – Columbus Laboratory OBC (ISS)
- European Space Agency (ESA) studies
  - RISC Evaluation Study (Saab Space), 1990
  - RISC Architecture and Technology (Sagem), 1990
- Selection criteria for a new architecture
  - Widely supported, Open architecture, License free
- SPARC V7 was selected
- SPARC in Space today
  - More than 10000 flight parts with SPARC inside have been shipped
  - Unique situation with a multitude of silicon sources
  - 25 years of experience, large installed base

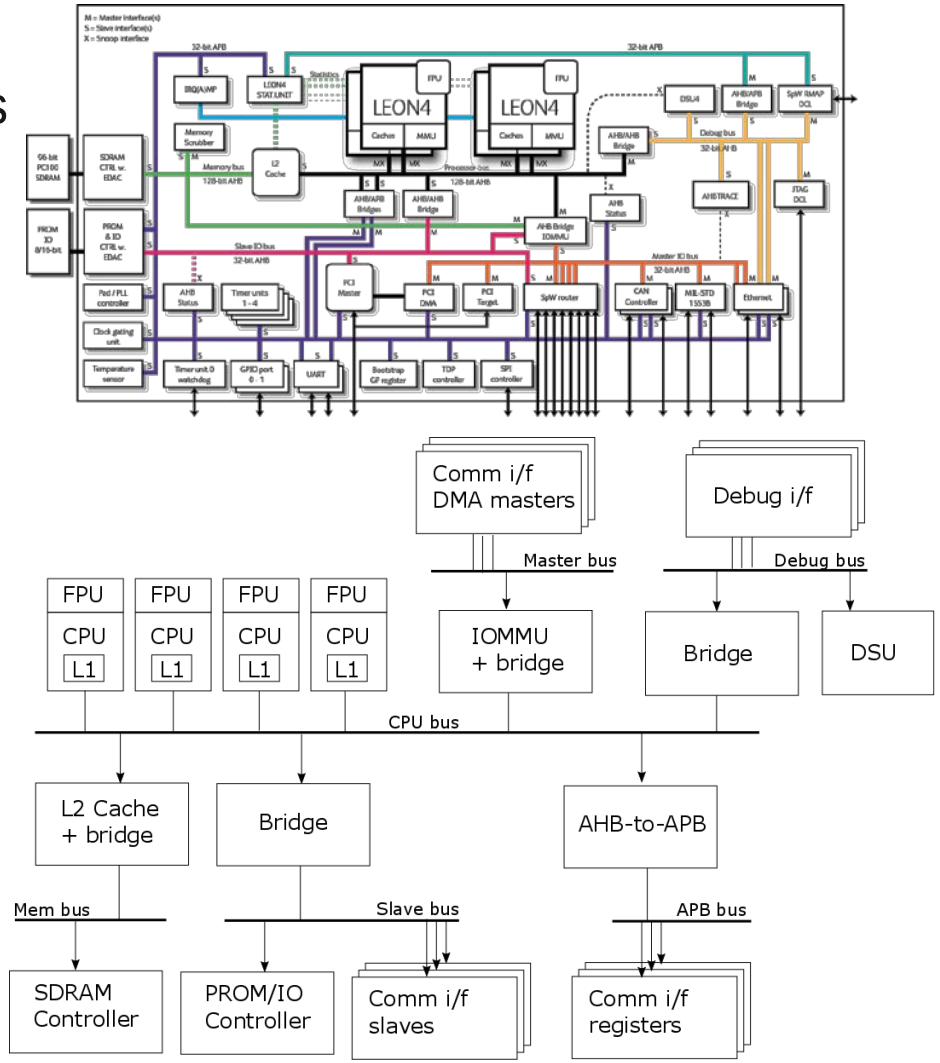
Motivation

- Why develop a new microprocessor?
  - Enable more demanding applications
  - Higher integration enables more flexible, compact, power efficient payloads
  - Allow consolidating multiple applications on same computer chip
  - Moving computation from separate FPGA/DSP/CPU to same chip
  - Ensure unrestricted European supply of microprocessor components free of foreign export restrictions.
- ESA development of Next Generation Microprocessor (NGMP)
  - Cobham Gaisler's bid was selected by ESA in open competitive tender to develop and commercialize the NGMP.
  - European space industry consensus was to continue development based on SPARC architecture.

Device Overview (1)

Internal architecture

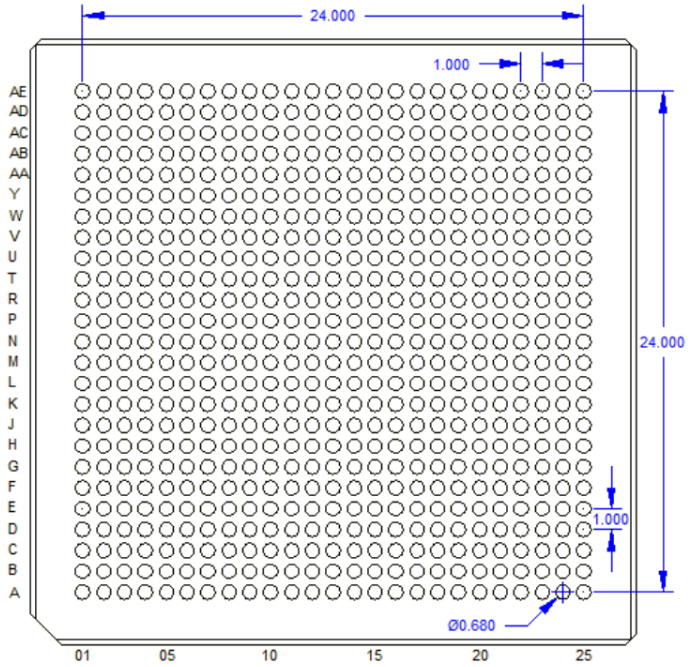
- System-on-chip
  - 4 x LEON4 fault tolerant CPU:s with MMU, FPU
  - 16+16 KiB Level-1 I+D cache, separate per CPU
  - 2048 KiB Level-2 cache, shared between CPUs
  - PLLs for clock generation
  - SDRAM memory controller with EDAC and scrubber
  - PROM memory controller with EDAC
  - Communication interfaces
- Targeting general-purpose payload processing.



Device Overview (2)

Package

- Product name GR740
- Ceramic 625 pin LGA Package
- Flight model will have columns attached (CCGA package)



Business model

- Commercialized by Cobham Gaisler:
  - Component and eval board sales
  - Supporting software (debugger etc)
  - Technical support
  - General point of contact on matters concerning device
- STMicroelectronics manages production, assembly, testing, and qualification (with Cobham Gaisler support when needed)
- Large commercial interest for product
  - Many inquiries and evaluation board sales
  - Interest both within and outside Europe
  - Customers already designing their own boards
  - At least two different customers planning to fly the first silicon

ESA Project overview (1)

Architecture definition phase

- Phase 1 (previous contract) – Architecture definition and prototyping
  - Hardware architecture development
  - Software development (OS, debugger, simulator)
  - FPGA prototypes
  - Functional prototype (“NGFP”) on structured ASIC and development board (parallel contract)
  - Benchmarking and evaluation
  - Requirements input and evaluation of architecture by end user (EADS Astrium)
- European 65nm space ASIC technology development going on (without our involvement) in parallel during phase 1.

ESA Project overview (2)

Porting to Space DSM

- Access to ST 65nm space (C65SPACE) design kit in 2014
  - IO limitations not known earlier meant design had to be revised
  - Extensive pin multiplexing required
  - Use of classic SDRAM instead of DDR memory

- Phase 1 CCN (previous contract) – Layout on C65SPACE
  - Design adaptations to technology library
  - Design upgrades following user feedback
  - ASIC back-end implementation (performed by STM)
  - Post-layout verification
  - Package design (e2v)

ESA Project overview (3)

- Phase 2 (this contract) – Prototype ASIC development
  - ASIC manufacturing (performed by STM)
  - Package manufacturing (NTK)
  - Package+ASIC assembly (e2V/STM)
  - Production test program development (Gaisler/ST)
  - Test pattern generation
  - Production testing (by STM w Gaisler support)
  - Functional validation of processor and interfaces
  - Benchmarking
  - Radiation testing
  - Development board design and production

Outputs from contract

- Materials:
  - Packaged prototypes (10 to ESA)
  - Validation boards (3 to ESA)
- Technical data:
  - Design database
  - Package design files
  - Validation board design files
  - Final test patterns
- Public documents (website):
  - GR740 data sheet
  - Validation board user manual
  - Validation / Benchmarking technical note
- Documents:
  - Layout plot
  - Production test plan
  - Production test report
  - Validation board specification
  - Validation plan
  - Validation report

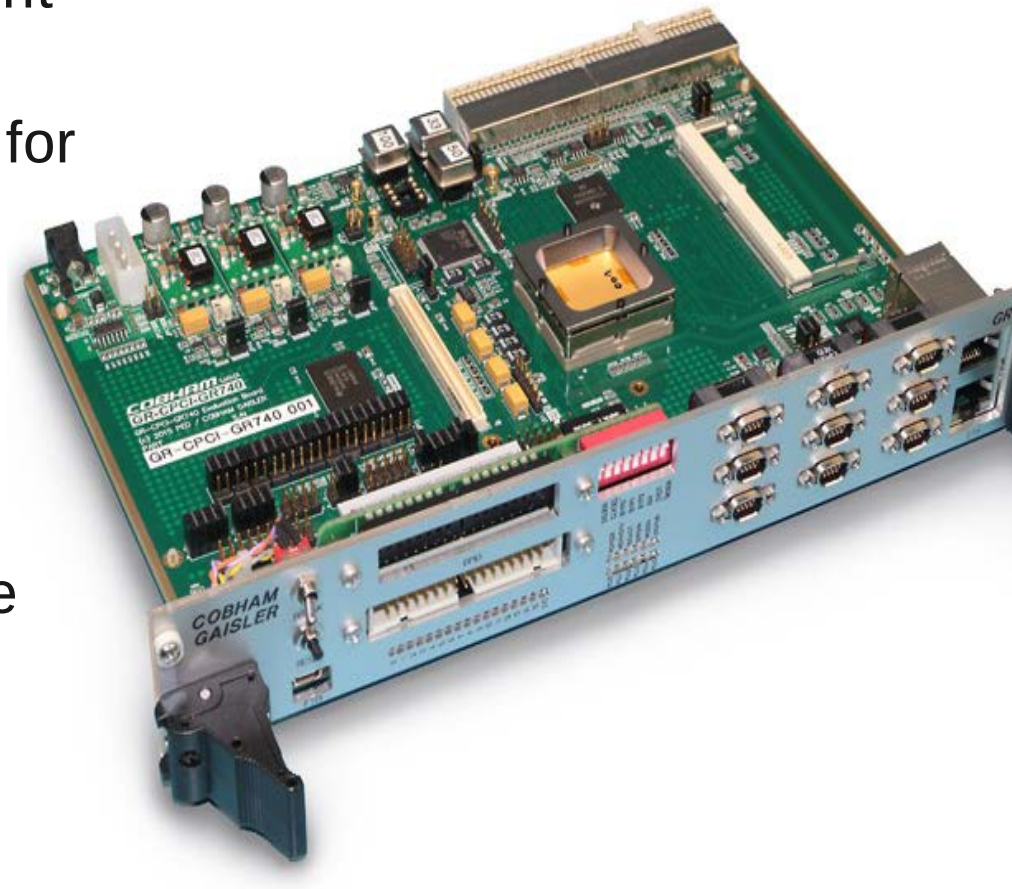
Results – production testing

Test program and bring-up

- Complete production test program developed and implemented on ATE and run successfully at ST Grenoble.
  - Covers all tests that are foreseen to be needed for the flight model.
  - Testing over full temp range and burn-in boards remaining
- Some characterization of devices also performed and trials of testing over temperature
- Functional bring-up of ASIC done at Gaisler
  - Processor system (CPU,FPU,caches) working correctly
  - All interfaces working correctly

Results - GR740 Development board

- A board was developed (with Pender Electronics) to allow benchmarking and development of GR740 software.
- Same board with socket used for ASIC bring-up, and radiation tests
- Version with device soldered available commercially as development board.
- All interfaces of the GR740 are available.



Results – Benchmarking (1)

Overview, single-core scaling

- A number of benchmarks have been ported and run on the GR740.
  - SPEC CPU2000
  - EEMBC CoreMark
  - Dhrystone
  - Whetstone
  - LinPack
- Key results have been published online in technical note
  - www.gaisler.com/gr740
- Technical note also contains power measurements

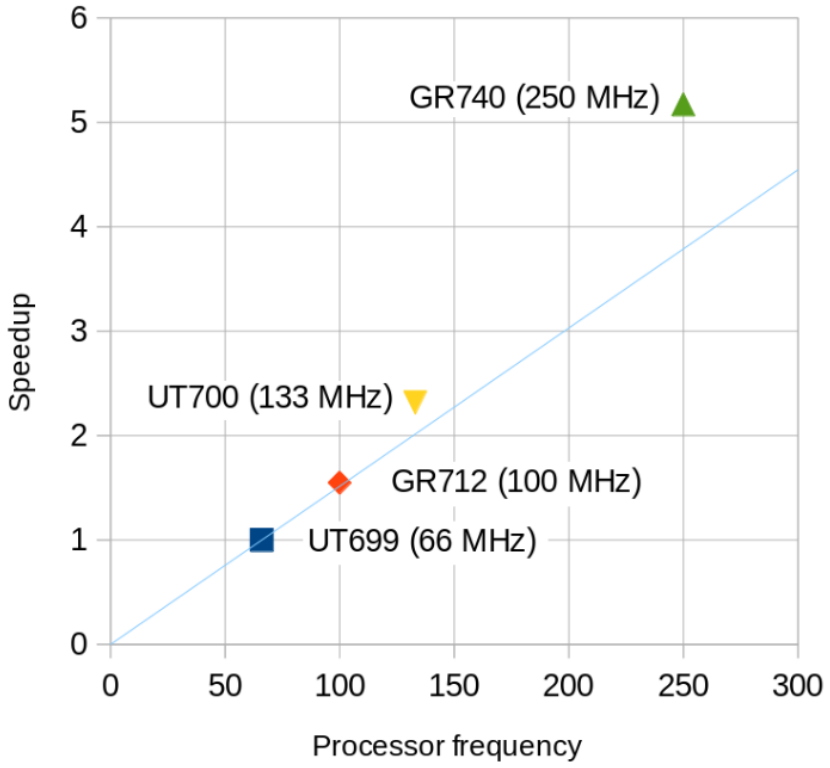
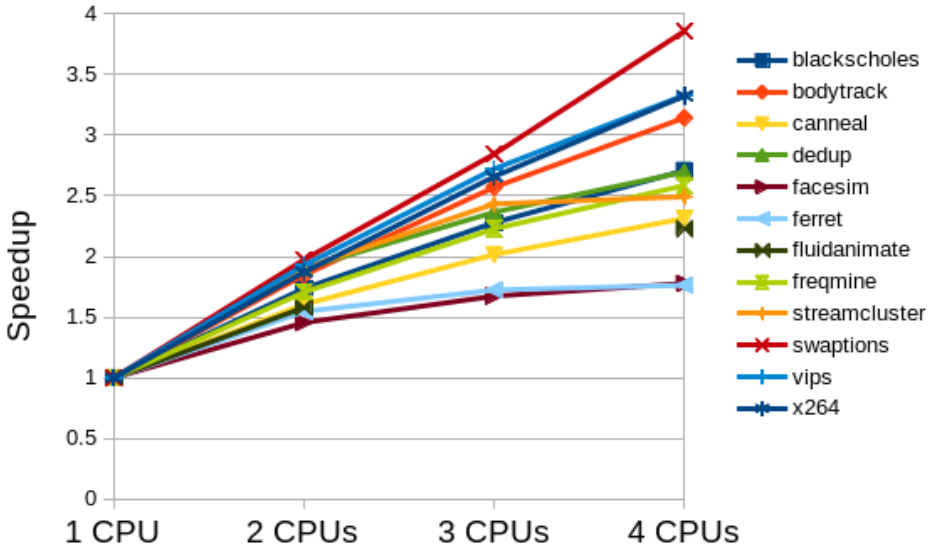


Figure 3. Cobham Gaisler device comparison (single-core)

Results – Benchmarking (2)

Multi-core scaling

- Multi-core speedup is application dependent and varies between benchmarks.
- L2 capacity and hit-under-miss support helps improve scaling and reduce impact of external memory speed.



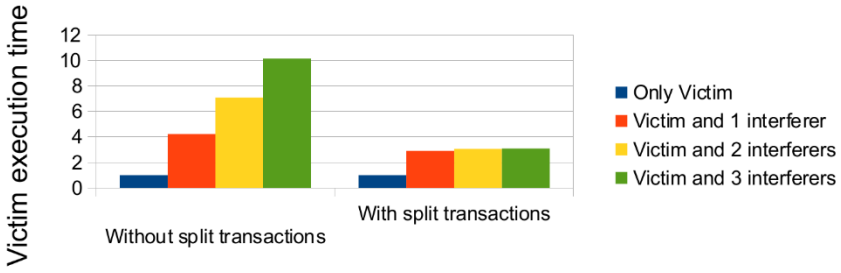
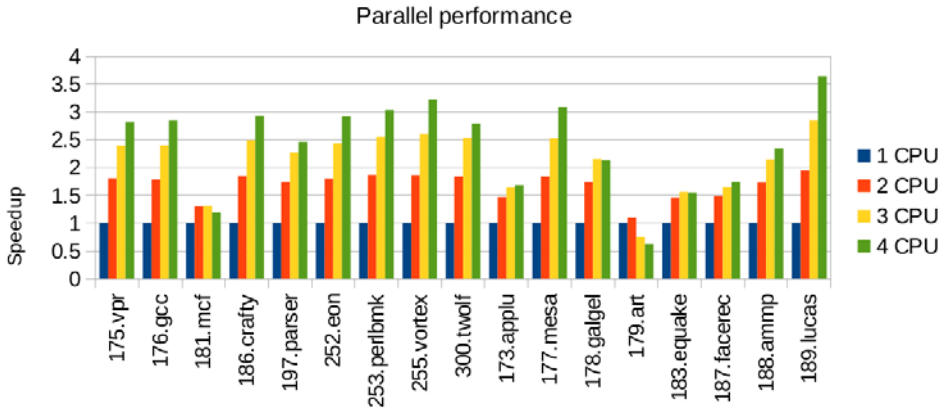


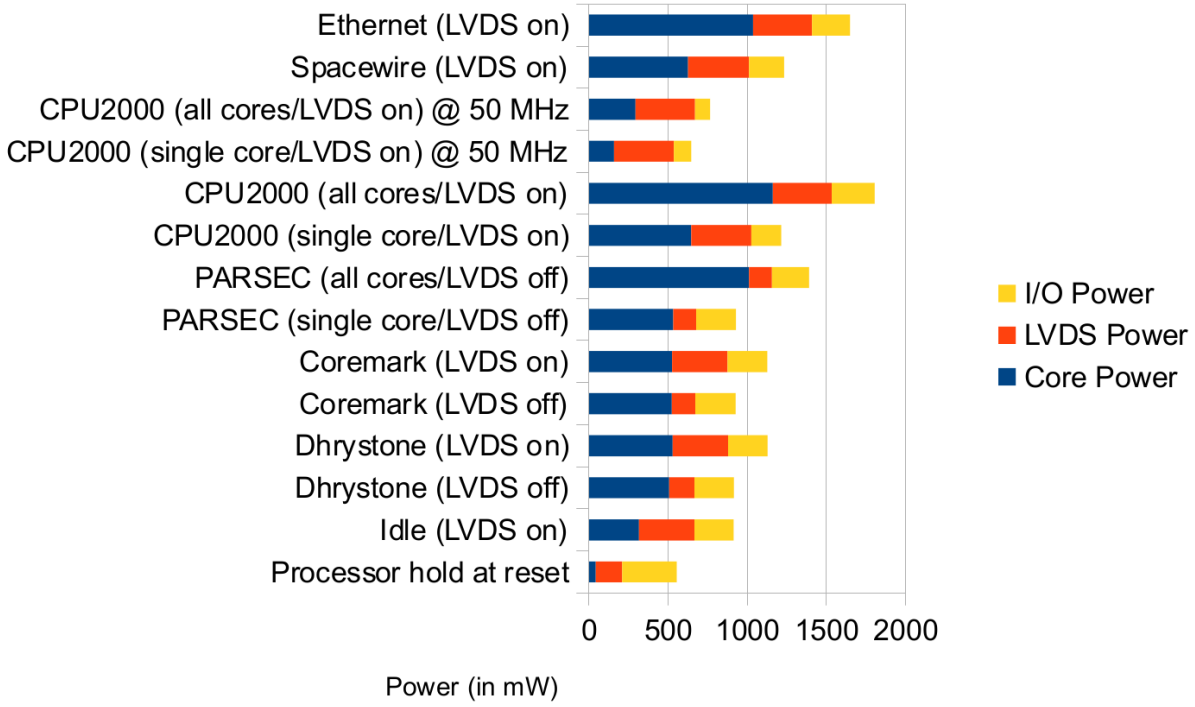
Figure 5. Impact of AMBA SPLIT transactions on bus interference



Results – Benchmarking (3)

Power consumption

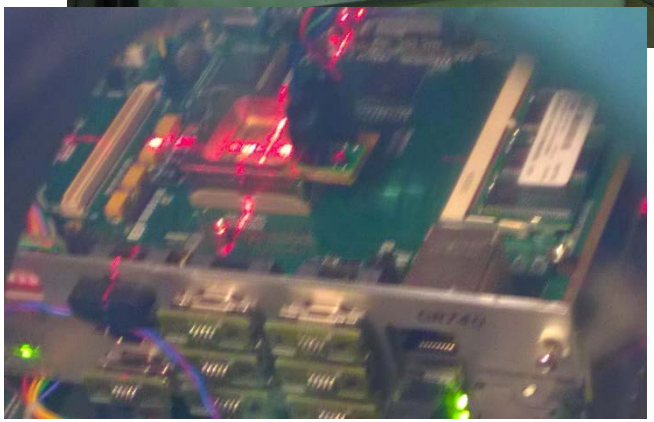
- Highest test case device power consumption measured in lab=1.8W – excellent power/performance!
- Thermal/power design value 4.4W at full load including margins for leakage at high temp and voltage variation



Radiation testing (1)

Overview

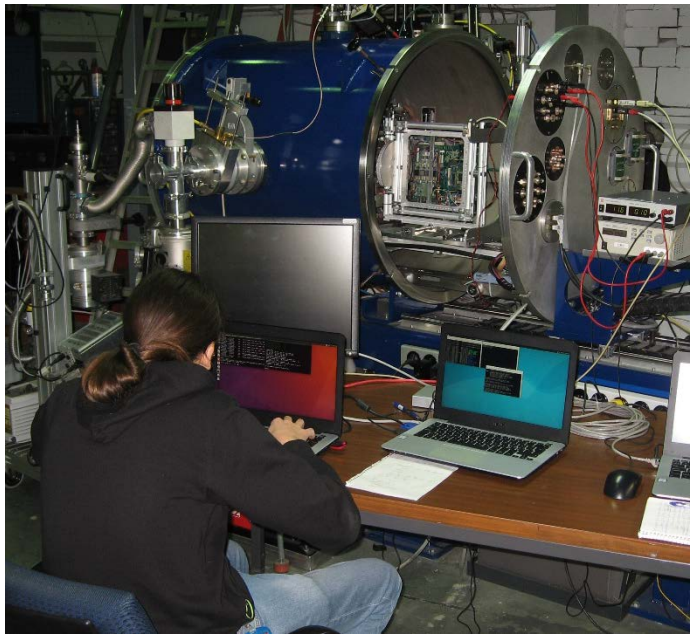
- Radiation campaigns performed at ESA radiation facilities UCL HIF/LIF (Belgium) and RADEF (Finland).
  - Static (basic cell error rate) and dynamic/application testing
  - Heavy ion and proton testing
- 4 sessions, 74 hours of beam time total.
- Radiation testing on this type of device is challenging
  - Device itself is logging the errors
  - A lot of post-processing and analysis required – many times more than the actual test time.

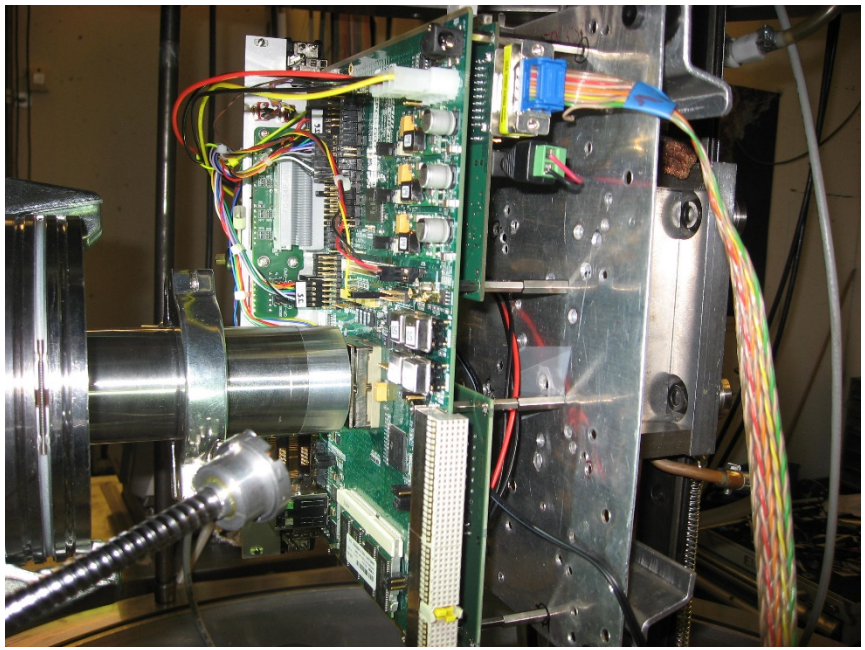


Radiation testing (2)

Results summary

- Radiation test results are overall positive
  - Error rates of building blocks (cells,RAM) matches expectation
  - TMR schemes implemented on RTL/layout level are working well
  - Target of 1E-4 errors/device/day (recoverable with reset) expected to be met with some margin in both GEO and LEO orbits





Radiation testing (3)

Level 2 cache issue

- Extensive radiation test campaign revealed L2 cache errata
  - Bit error in L2 tags not corrected properly in certain special cases
- The issue was isolated and diagnosed, root cause found
- Evaluated potential for metal mask fix with spare cells
  - Trial layout by ST showed such fix NOT feasible to implement
- Developed a partial SW workaround based on locked down cache
  - Gets MTBF down to order of 1 error/week (recoverable with reset)
  - Turning off L2 completely also possible workaround
- First silicon can still be flown
  - There are early adopter customers planning to fly first silicon using SW workaround, accepting higher error rate caused by errata.
- Extensive verification done to ensure issue has been corrected properly for respin.

Issues encountered

Outcome of testing

- A few other silicon errata discovered during the functional validation
- Minor ESD protection issue, limited to LVDS driver cells
  - Requires more careful handling of prototypes
- Minor logic errata
  - Can be handled with software or PCB workarounds
- All these issues will be corrected for the flight silicon

Next phase

- Phase 3 – Flight model development
  - New silicon addressing L2 EDAC errata and ESD sensitivity issue
  - Package and assembly adjustment to improve mechanical reliability of component (STM)
  - Qualification and burn-in test development (STM)
  - Establish supply chain for column attach
- GSTP activity approved in IPC May 2017
- Work is already progressing on all four points above
  - RTL is ready, back-end work on respin ready to begin in mid 2017
  - Preparations for qualification and columns ongoing
  - QML qualified flight silicon planned to be available by end of 2018

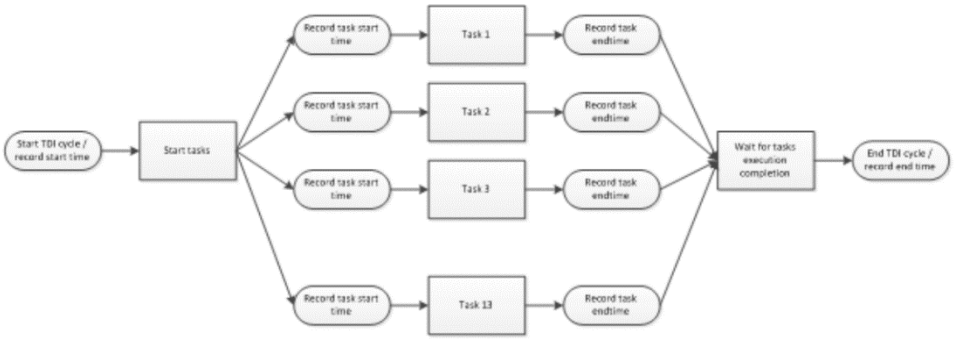
Related activities (1)

- The NGMP/GR740 work has been useful in other activities. A few examples (see also ESAs NGMP website):
  - "DDR interface for C65SPACE" (CG,ISD) – ESA contract to develop memory controller IP and PHY for DDR2/3 on ST 65nm space platform. Controller IP design uses lessons learned and experience from NGFP and GR740.
  - "Development environment for future Leon multi-core" (CG,OAR,ADS) - ESA project to make multi-core version of the RTEMS OS, uses GR740 as target.
  - "Heavy ion SEE testing of Microsemi RTG4 flash based FPGA" (Cobham RAD UK, CG)- Radiation test activity re-using NGMP design and GR740 radiation test software
  - "System impact of distributed multicore systems" (ADS, Univ. Pol. of Valencia) - Development of XtratuM hypervisor for LEON/SPARC, using NGMP as target.

Related activities (2)

Practical example

- Porting of GAIA VPU software
  - Study done together with Airbus DS to port space image processing application from US single board computer to NGMP.
  - Proof-of-concept for parallelizing single-core application
  - GR740 met performance needs with significant power saving compared to existing solution.



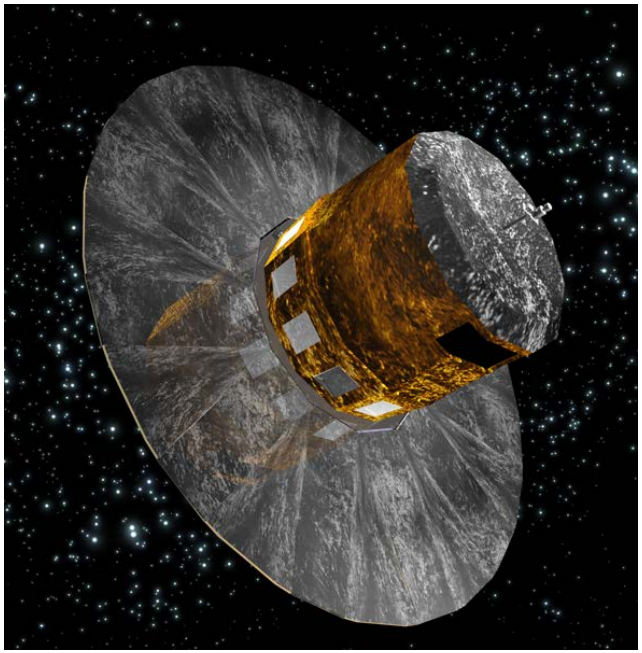


Image (C) ESA

Future evolution

- Future work (“GR745”), pending funding
  - Architectural improvements for higher compute performance
  - Extended support for time and space partitioning
  - More efficient virtualization support, hypervisor mode in HW
  - Move to DDR2/3/4 memory for performance and capacity
  - High-speed serial interfaces (SpFI / SRIO)
  - Flip chip packaging for improved pin count and signal integrity
- Depends on some technology level features
  - In particular, availability of DDR phy and IO buffers

Conclusions

- State of the art space microprocessor has been developed up to prototype level and meets or exceeds performance goals.
- European design and supply chain.
- Prototypes and development boards available for use by industry. We see healthy interest in the product.
- Two errata has been identified, one relating to radiation performance and one related to ESD protection. These will be corrected in the re-spin of the silicon. Otherwise, functional aspects of the design have been validated to be correct.
- Flight model development in progress (parts available planned for end of 2018)

End of presentation

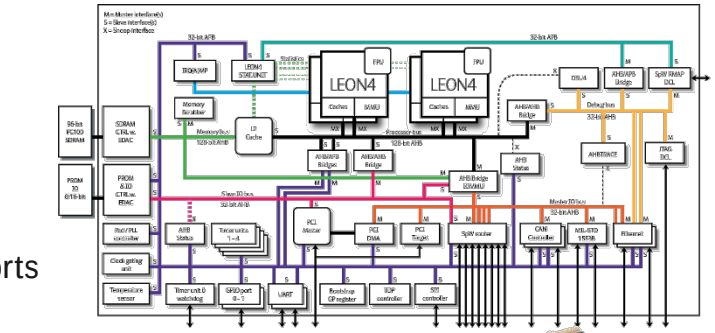
- Thanks for listening!

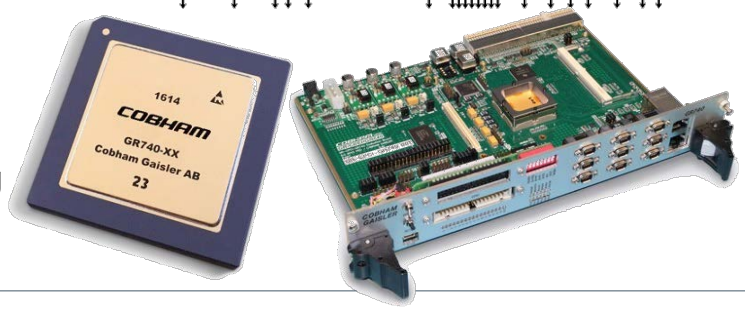
Contact: sales@gaisler.com

GR740 Website: http://www.gaisler.com/gr740

ESA NGMP website: http://microelectronics.esa.int/ngmp/

- Quad-core LEON4FT rad-tolerant SoC device
  - 4x LEON4FT with dedicated FPU and MMU
  - 128 KiB L1 caches connected to 128-bit bus
  - 2 MiB L2 cache, 256-bit cache line, 4-ways
  - 64-bit SDRAM memory I/F (+32 checkbits)
  - 8-port SpaceWire router with +4 internal ports
  - 32-bit 33 MHz PCI interface
  - 2x 10/100/1000 Mbit Ethernet
  - Debug links: Ethernet, JTAG, SpaceWire
  - MIL-STD-1553B, CAN 2.0B, 2 x UART
  - SPI master/slave, GPIO, Timers & Watchdog





COBHAM
Cobham Gaisler AB

life.augmented

SPARC