CURRENT AND NEXT GENERATION LEON SYSTEM-ON-CHIP ARCHITECTURES FOR SPACE

Jan Andersson[1], Daniel Hellström[1], Sandi Habinc[1], Roland Weigand[2], Luca Fossati[2]

[1]Aeroflex Gaisler, Kungsgatan 12, SE-411 91, Göteborg, Sweden
Tel: +36 31 7758650 Fax: +46 31 421407, E-mail: {jan,daniel,sandi}@gaisler.com

[2]European Space Agency, Keplerlaan 1 – PO Box 299, 2220AG Noordwjik ZH, The Netherlands
Tel: +31 71 565 32 98, E-mail: {roland.weigand,luca.fossati}@esa.int

EXTENDED ABSTRACT

Aeroflex Gaisler develops the LEON3FT and LEON4FT SPARC V8 fault-tolerant microprocessors. The processors are available both as IP cores part of an IP library that allows users to design their own custom system-on-chip (SoC) designs, and also as part of ready made designs and devices.

Traditionally a LEON SoC design has consisted of one single processor connected to a bus with a memory controller and various peripherals and communication controllers. In recent years a shift has been made where multi-core architectures have become available for use in the harsh space environment.

The presentation will give an overview of the LEON3FT and LEON4FT processors and then show how the architectures where LEON processors are implemented have evolved from single CPU systems, to multi-core devices via the GR712RC processor and currently to the quad-processor Next Generation Microprocessor (NGMP) architecture currently being developed in activities initiated by the European Space Agency (ESA).

This abstract mainly describes the GR712RC and NGMP architectures. The focus in the presentation will be on the NGMP architecture and describe the design decisions made and features implemented to improve performance, debugging-support and time-space-partitioning (TSP).

1 BACKGROUND

The LEON project was started by the European Space Agency in late 1997 to study and develop a high-performance processor to be used in European space projects. The objectives for the project were to provide an open, portable and non-proprietary processor design, capable to meet future requirements for performance, software compatibility and low system cost. Another objective was to be able to manufacture in a Single Event Upset (SEU) sensitive semiconductor process. To maintain correct operation in the presence of SEUs, extensive error detection and error handling functions were needed. The goals have been to detect and tolerate one error in any register without software intervention, and to suppress effects from Single Event Transient (SET) errors in combinational logic.

The LEON family includes the first LEON1 VHSIC Hardware Description Language (VHDL) design that was used in 2001 in the LEONExpress test chip developed in 0.35 µm technology to prove the fault tolerance concept. The second LEON2 VHDL design was used in 2004 in the processor device AT697 from Atmel (F) and various system-on-chip devices. These two LEON implementations were developed by ESA. Gaisler Research, now Aeroflex Gaisler, developed the third LEON3 design that is used in a number of avionics systems and also in the commercial sector. Aeroflex Gaisler recently announced the availability of the GR712RC rad-hard device with dual core LEON3FT processor and also the availability of the fourth generation LEON, the LEON4 processor.

Following the development of the TSC695 (ERC32) and AT697 processor components in 0.5 and 0.18 µm technology respectively, ESA has initiated the NGMP activity in 2009 targeting an European Deep Sub-Micron (DSM) technology in order to meet increasing requirements on performance and to ensure the supply of European space processors. Aeroflex Gaisler was selected to develop the NGMP system that is centred around the new LEON4FT processor.

2 GR712RC

The GR712RC System-on-Chip (SoC) is a dual core LEON3FT system suitable for advanced high reliability space avionics. Fault tolerance features from Aeroflex Gaisler's GRLIB IP library and an implementation using Ramon Chips RadSafe cell library enables superior radiation hardness.

The GR712RC device has been designed to provide high processing power by including two LEON3FT 32-bit SPARC V8 processors, each with its own high-performance IEEE754 compliant floating-point-unit and SPARC reference memory management unit.

This high processing power is combined with a large number of serial interfaces, ranging from high-speed links for data transfers to low-speed control buses for commanding and status acquisition.

The GR712RC device comprises the following functions:

- 2 x LEON3FT processor cores with MMU and GRFPU
  - Branch prediction and on-the-fly error correction resulting in 30% performance increase compared to regular LEON3FT
  - 4x4 KiB instruction cache and 4x4 KiB data cache
- On-chip Debug Unit with instruction and AHB trace buffers
- PROM/SRAM/SDRAM fault tolerant memory controller (using BCH or Reed-Solomon)
- 256 KiB on chip fault-tolerant RAM
- 6 x SpaceWire links (2 with RMAP support)
- 6 x UARTs
- 6 x General Purpose Timers (2 with time latch capability)
- Multi-processor Interrupt Controller with support for 31 interrupts
- 2 x 32 bits General Purpose I/O
- JTAG debug link
- 10/100 Ethernet MAC with RMII interface
- MIL-STD-1553B BC/RT/BM controller
- 2 x CAN 2.0 and one SatCAN controller
- CCSDS Telecommand decoder and Telemetry encoder
- SPI controller
- I^2C controller
- SLINK controller
- ASCS16 controller
- Clock gating unit
- I/O switch matrix

The variation in interfaces allows different systems to be implemented using the same device type, which simplifies parts qualification and procurement. It also brings cost reductions to software development since the core functionality can be reused from application to application, only changing the drivers for the interfaces. Due to the high amount of peripherals and a limited number of pins there is an I/O switch matrix that controls which peripheral is connected to each pin.

3 NEXT GENERATION MICROPROCESSOR

Figure 2 shows an overview of the NGMP architecture as implemented in functional prototype devices that will be available in Q4 2012.

The system consists of five Advanced High-performance Buses (AHB); one 128-bit Processor bus, one 128-bit Memory bus, two 32-bit I/O buses and one 32-bit Debug bus. The Processor bus hosts four LEON4FT cores connected to a shared Level-2 (L2) cache. The Memory bus is located between the L2 cache and the main external memory interfaces, DDR2 SDRAM and SDR SDRAM, and also connects a memory scrubber. As an alternative to a large on-chip memory, part of the L2 cache can be turned into on-chip memory by cache-way disabling.

The two separate I/O buses connect all the peripheral cores. All memory mapped interfaces of peripheral cores that can be directly accessed by the processors have been placed on one bus (Slave I/O bus), and all master/DMA interfaces have been placed on the other bus (Master I/O bus). The Master I/O bus connects to the Processor bus via an AHB bridge that provides access restriction and address translation (IOMMU) functionality. The two I/O buses include all peripheral units such as timers, interrupt controller, UARTs, general purpose I/O port, PCI master/target, Ethernet MAC, MIL-STD-1553B, Serial Peripheral Interface bus and SpaceWire router. All I/O

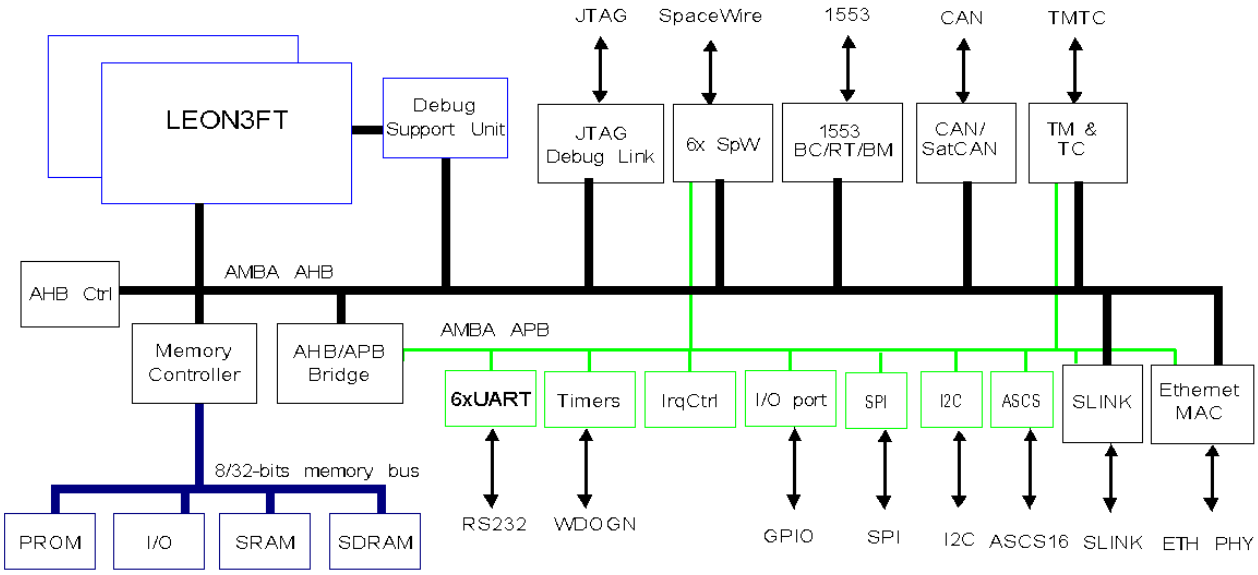

Figure 1: GR712RC Block Diagram

master units in the system contain dedicated DMA engines and are controlled by descriptors located in main memory that are set up by the processors. Reception of, for instance, Ethernet and SpaceWire packets will not increase CPU load. The cores will buffer incoming packets and write them to main memory without processor intervention.

The fifth bus, a dedicated 32-bit Debug bus, connects a debug support unit (DSU), PCI and AHB trace buffers and several debug communication links. The Debug bus allows for non-intrusive debugging through the DSU and direct access to the complete system, as the Debug bus is not placed behind an AHB bridge with access restriction functionality.

The list below summarizes the specification for the NGMP system:

- 128-bit Processor AHB bus
  - 4x LEON4FT
    - 16 + 16 KiB write-through cache with LRU or random replacement
    - SPARC Reference MMU
    - Physical snooping
    - 32-bit MUL/DIV
    - FPU shared between pairs of LEON4FT
  - 1x256 KiB Shared L2 write-back cache with memory access protection (fence registers), cache-way locking. LRU, psuedo-random or master-index replacement
  - 1x 128-bit to 32-bit unidirectional AHB to AHB bridge (from Debug bus to Processor bus)
  - 1x 128-bit to 32-bit unidirectional AHB to AHB bridge (from Processor bus to Slave I/O bus)
  - 1x 32-bit to 128-bit unidirectional AHB to AHB bridge with IOMMU (from Master I/O bus to Processor bus)
- 128-bit Memory AHB bus
  - 1x 64-bit data DDR2-800 memory interface with Reed-Solomon ECC (with 16 or 32 check bits)
  - 1x 64-bit data SDRAM PC133 memory interface with Reed-Solomon ECC (with 16 or 32 check bits)
  - 1x Memory scrubber
- 32-bit Master I/O AHB bus
  - SpaceWire router with eight external ports and four AMBA ports, with RMAP @ 200 Mbit/s
  - 2x 10/100/1000 Mbit Ethernet interface with MII/GMII PHY interface
  - 1x 32-bit PCI target interface @ 66 MHz
  - MIL-STD-1553B interface
- 32-bit Slave I/O AHB bus
  - 1x 32-bit PCI initiator interface @ 66 MHz with DMA controller mapped to the Master I/O bus
  - 1x 8/16-bit PROM/IO controller with BCH ECC
  - 2x 32-bit AHB to APB bridge connecting:
    - 5x General purpose timer unit
    - 1x 16-bit general purpose I/O port
    - 2x 8-bit UART interface
    - 1x Multiprocessor interrupt controller
    - 1x PCI arbiter with support for eight agents
    - 2x AHB status register
    - 1x Clock gating control unit
    - 1x LEON4 statistical unit (perf. counters)
    - 1x SPI master/slave controller
    - PLL and pad control units
- 32-bit Debug AHB Bus
  - 1x Debug support unit
  - 1x USB debug link
  - 1x JTAG debug link
  - 1x SpaceWire RMAP target

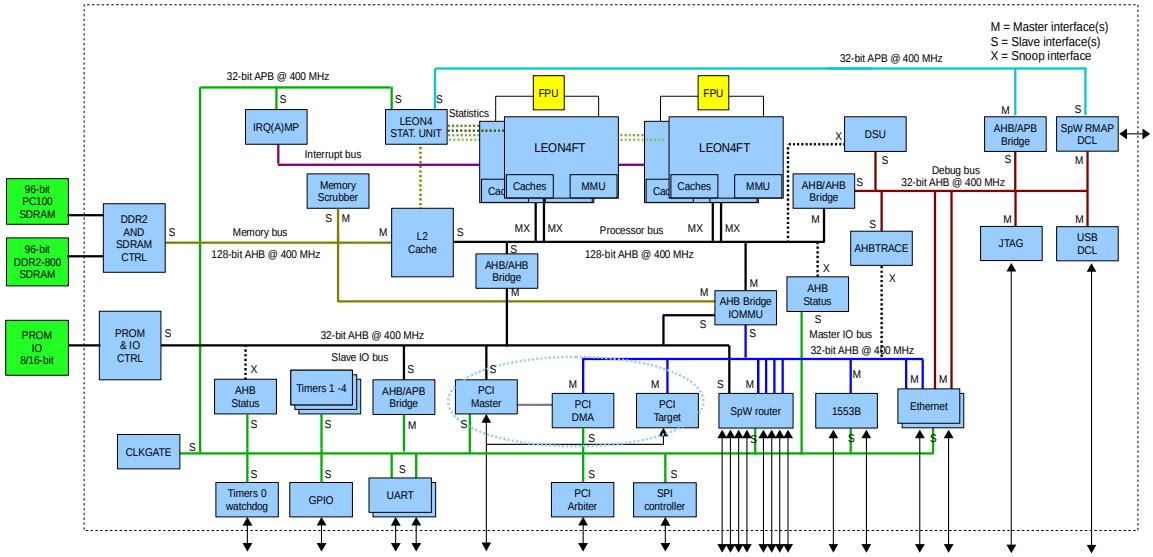

Figure 2: NGMP Functional Prototype Block Diagram

- 1x AHB trace buffer, tracing Master I/O bus
- 1x PCI trace buffer

4 CONCLUSION

Available system-on-chip architectures for space have evolved from simple micro-controllers to system-on-chip designs and more complex multi-core processor architectures. The new components for the space market are following the steps taken in the commercial world - implementing multiple processor cores (multi-core) in system-on-chip designs.

The GR712RC dual-core LEON3FT processor provides in addition to superior processing performance several functions suitable for small and large satellites, such as CCSDS/ECSS telemetry and telecommand, multiple high-speed serial links, etc. The component can be used both in platform and payload.

The NGMP will be a SPARC V8(E) based multi-core architecture that provides a significant performance increase compared to earlier generations of European space processors, with high-speed interfaces such as SpaceWire and Gigabit Ethernet on-chip. The platform will have improved support for profiling and debugging and will have a rich set of software immediately available due to backward compatibility with existing SPARC V8 software and LEON3 board support packages. NGMP includes also specific support for AMP configurations and Time-Space Partitioning. Five MMUs, one per CPU core and the IOMMU provide access protection, one dedicated interrupt controller (IRQAMP) allow interrupt steering to each CPU core, and duplicated sets of timers, one per core, allow running separate operating systems on each CPU core.

The dual-core GR712RC device is currently available from Aeroflex Gaisler. The NGMP is part of the ESA roadmap for standard microprocessor components. It is developed under ESA contract, and it will be commercialised under fair and equal conditions to all users in the ESA member states.

Both devices are also fully developed with manpower located in Europe, and only with European IP sources. They are therefore not affected by US export regulations.