NGMP → GR740

Status and Roadmap

Vision for Future

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History of ESA Microprocessor Developments

MA 31750 (Dynex Semiconductor)

- MIL-STD-1750A architecture
- GEC-Plessey 1.5 µm

SPARC V7 ERC32 chipset

- 3-chips: IU, FPU, MEC
- Temic 0.8 µm

SPARC V7 ERC32 single chip

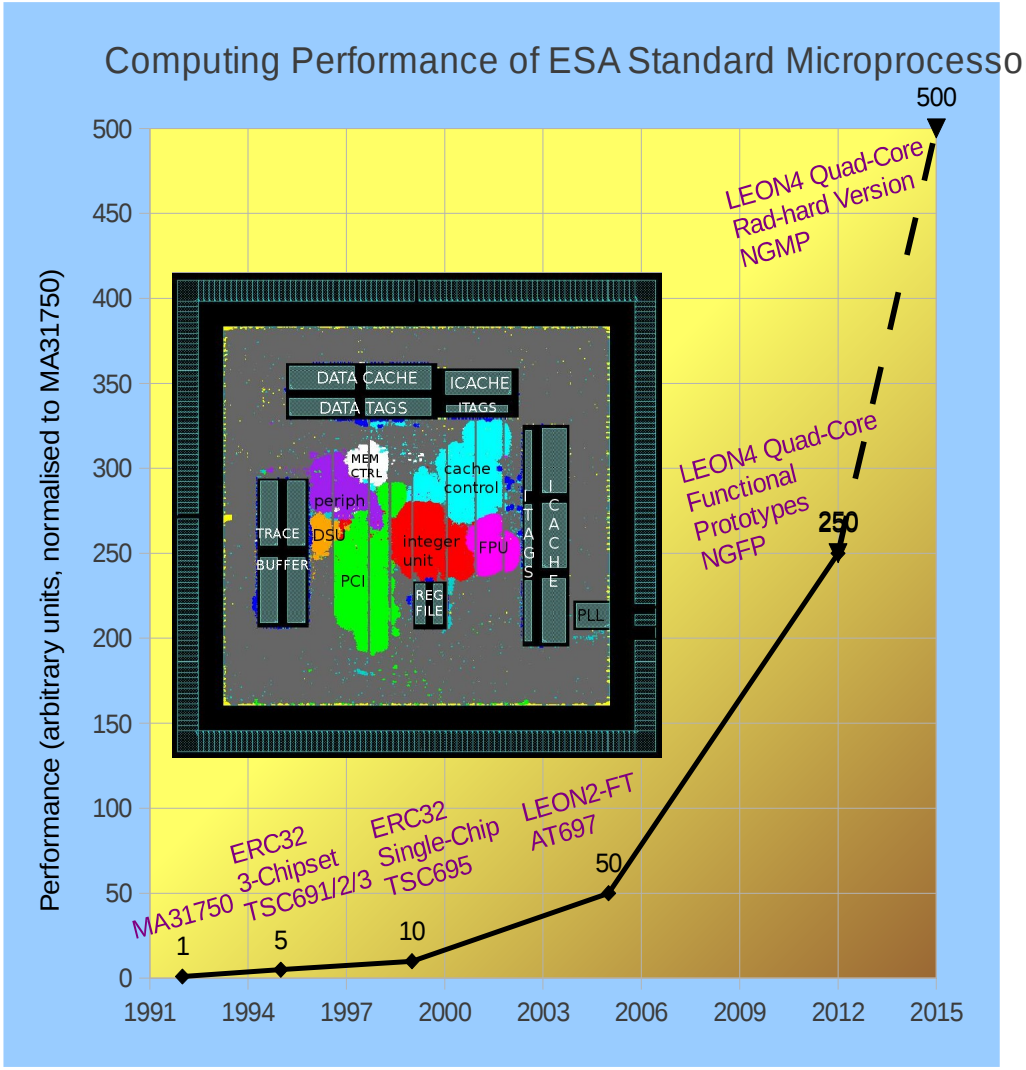
- Temic 0.5 µm

SPARC V8 LEON2/AT697

- Atmel 0.18 µm

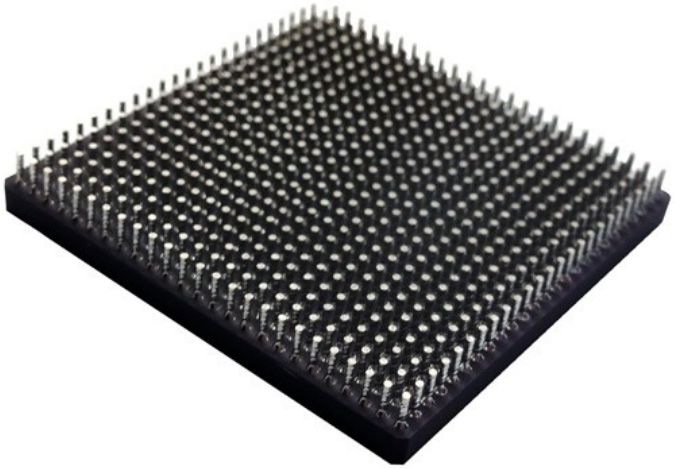
SPARC V8 LEON4/NGMP

- Goal: 10x AT697 performance



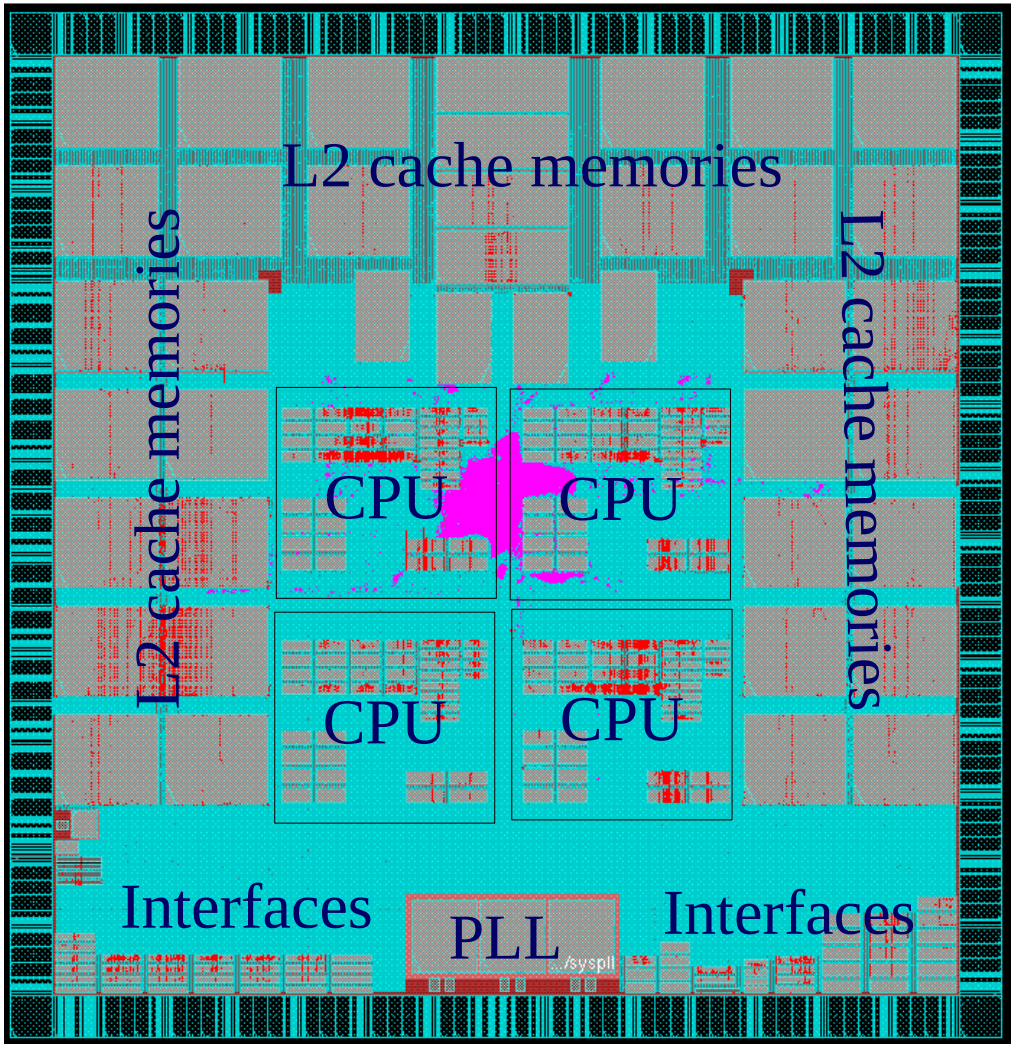
NGMP Development Roadmap

- Start 2009: VHDL / PDR done (2010), commercial prototypes (2013)
  - On-hold for 3 years waiting for access to technology
  - Development resumed in 2014, product code is now GR740
- ST C65SPACE technology design kit provided in April 2014
  - Technology mapping (memory and hard-IP integration) done
  - Layout in progress, directly by ST – no Atmel involvement
  - Architectural refinements (L2 cache) and bugfixes in progress
  - Baseline package: CLGA 625, cavity development in progress
- Tape-out planned in Q1/2015
- EM / board availability: Q4/2015
- Validation 2015 (funding approved)
- Qualification 2016 (funding permitted)
  - Goal: use existing (EM) silicon dies



GR740 Specification

- Adapted specification taking into account technology constraints and capabilities
- No DDR2 (requires PHY), only SDRAM
- No SERDES (requires flip-chip package)
- Increased L2 cache size 2 Mbyte
- Improved performance counters to ease execution time analysis
- L2 cache controller split support to reduce inter-core interference (TBC)
- Frequency goal 300 MHz (TBC)
  - 250 is currently more realistic
  - 4x250 = 10x100 = 10xAT697 = GINA
- Pin multiplexing:
  - PROM with UART, CAN, 1553 and SPW debug ports
  - Half of SDRAM port multiplexed with PCI and one of 2 Ethernet ports



Chip area ~ 8.4 x 8.7 = 73 mm²

NGMP Benchmarking

- Benchmarks run at the same frequency (50 MHz) for all devices
  → increase in max clock frequency to be considered
- SCOC3, AT7913 have similar performance as AT697

Benchmark	AT697	UT699	GR712RC	NGMP
164.gzip	1	0.94	1.1	1.31
176.gcc	1	0.79	0.97	1.3
256.bzip2	1	0.93	1.06	1.33
AOCS	1	1.2	1.52	1.79
Basicmath	1	1.3	1.46	1.62
Coremark, 1 thread	1	0.89	1.09	1.21
Coremark, 4 threads	1	0.89	2.05	4.59
Drystone	1	0.94	1.05	1.39
Drystone, 4 instances	1	0.94	1.61	4.81
Linpack	1	1.2	1.26	1.71
Whetstone	1	1.94	2	2.22
Whetstone, 4 instances	1	1.94	3.7	8.68

improved cycles per instruction (CPI)

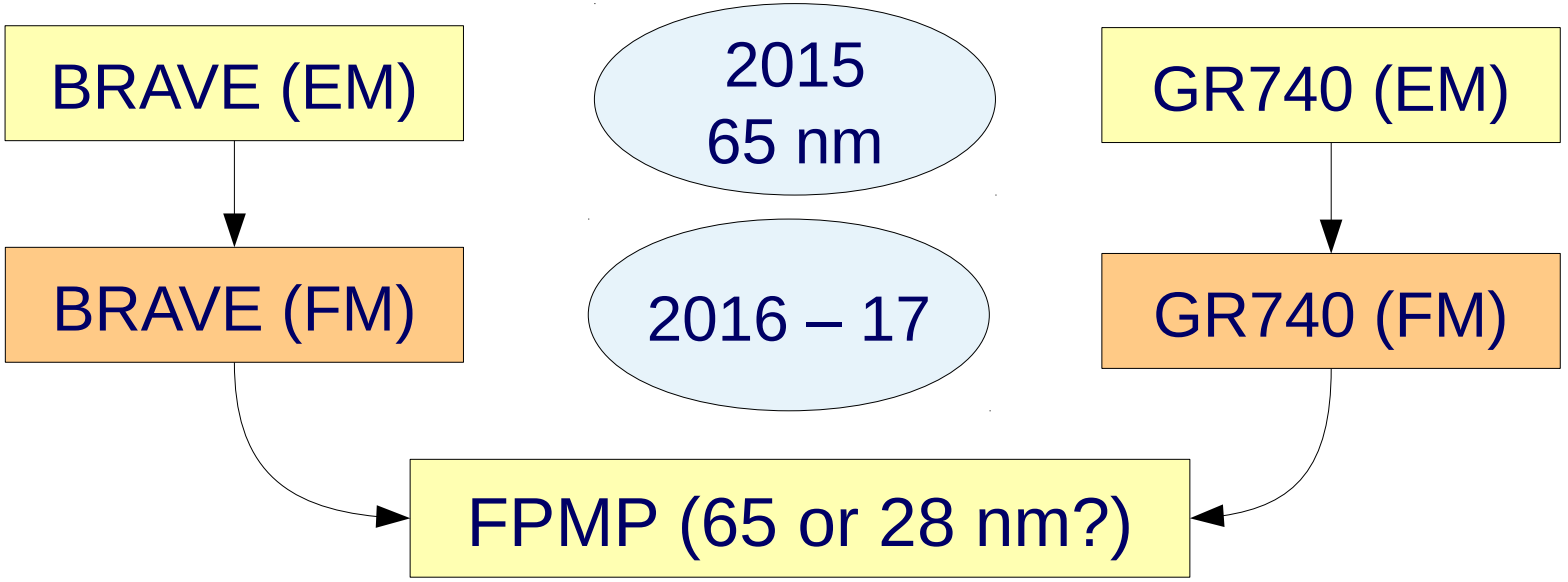
good scaling on multi-threaded benchmarks (4 cores) → almost x4

FPMP – Field Programmable MicroProcessor (a vision)

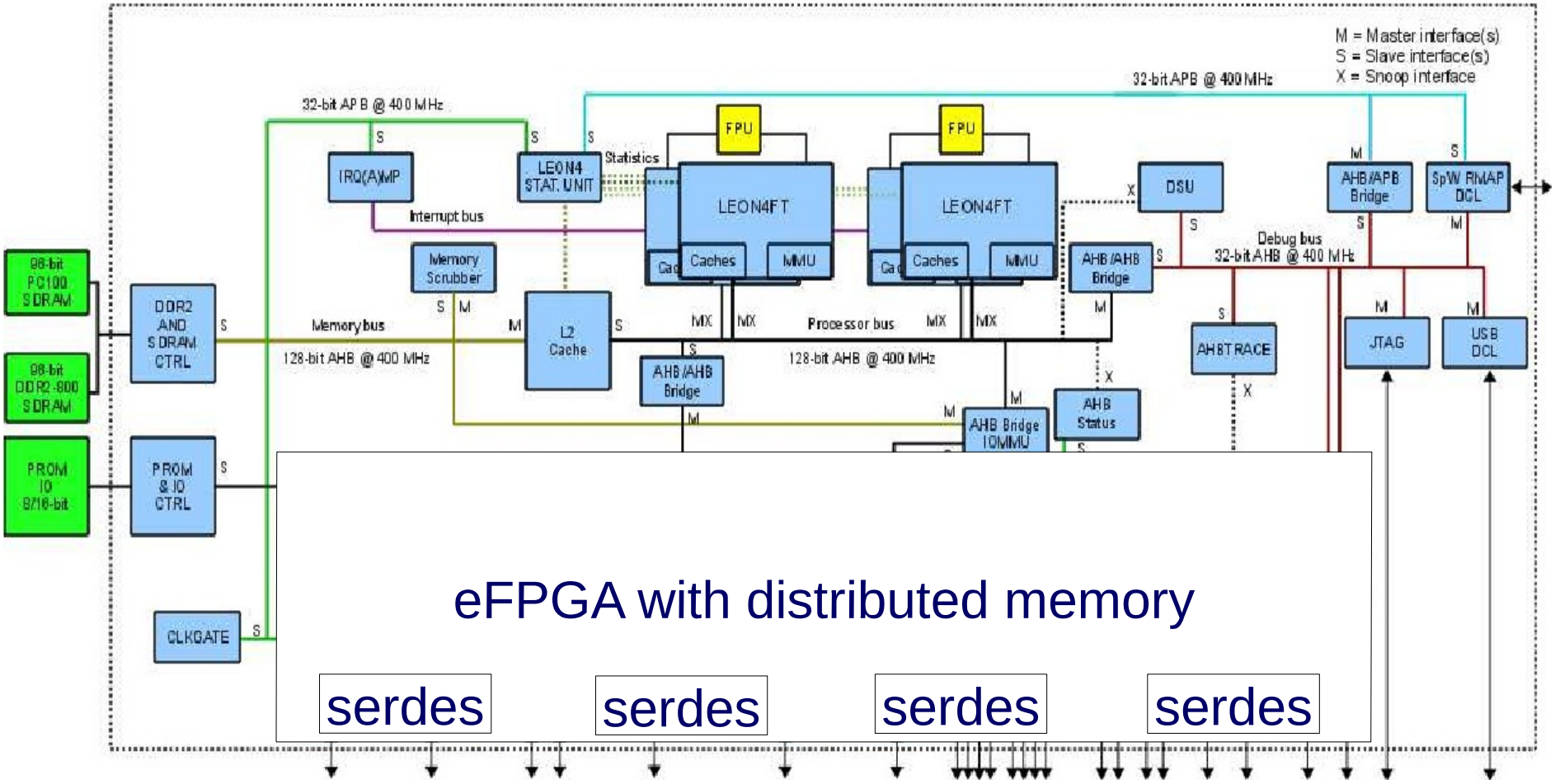
- FPGA and Microprocessor are 'high-volume' products for space
- Microprocessor and FPGA often complement each other
- Commercial FPGA offer SOC-FPGA with hard microprocessors

==> FPMP1 = space microprocessor with embedded FPGA?

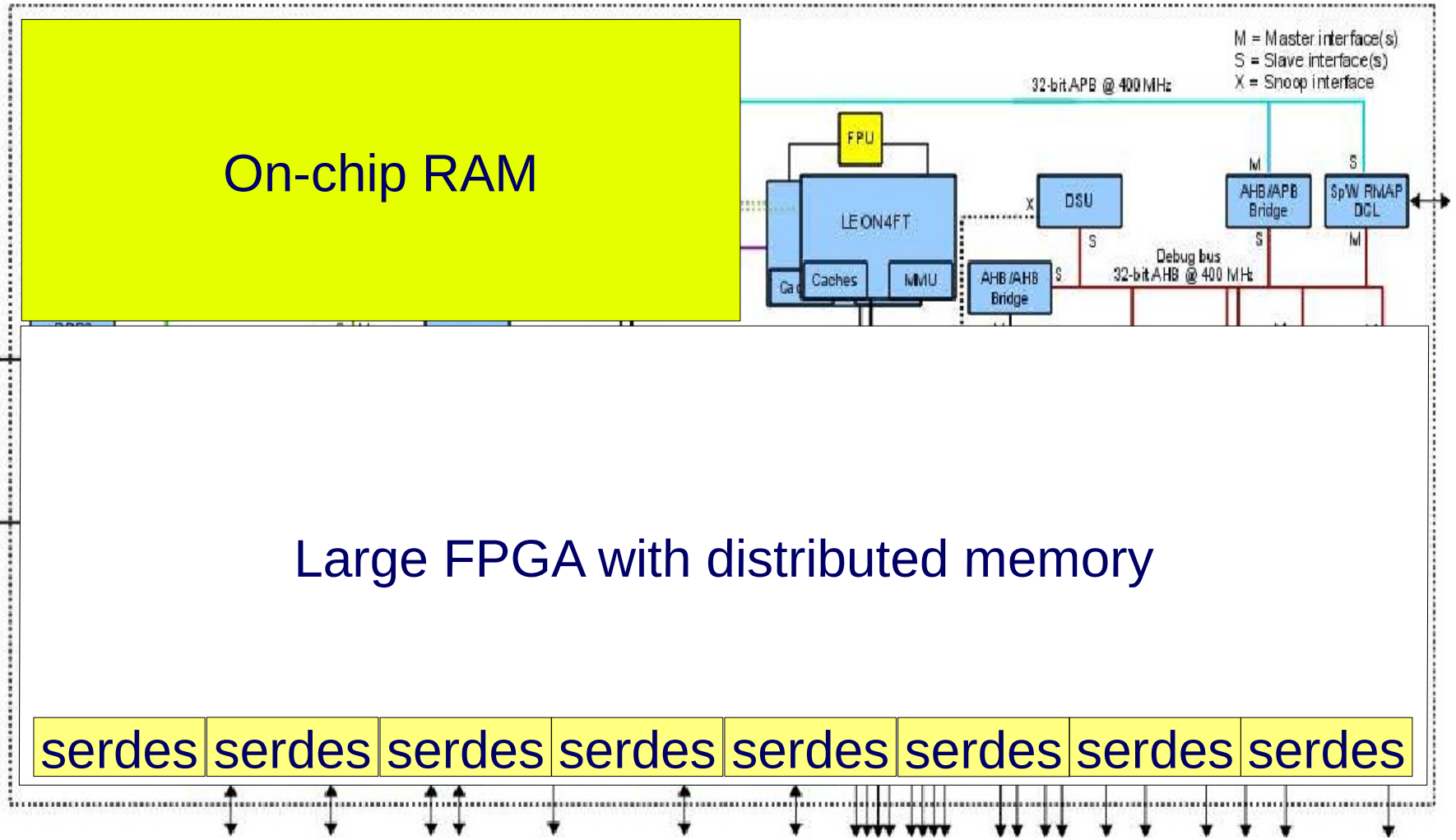
==> FPMP2 = space FPGA with embedded microprocessor?



FPMP1: high end CPU + eFPGA for IO and co-processing



FPMP2: large FPGA for DSP with “light” control CPU



no external memory

For more information and documentation

please refer to the following site:

http://microelectronics.esa.int/ngmp/ngmp.htm