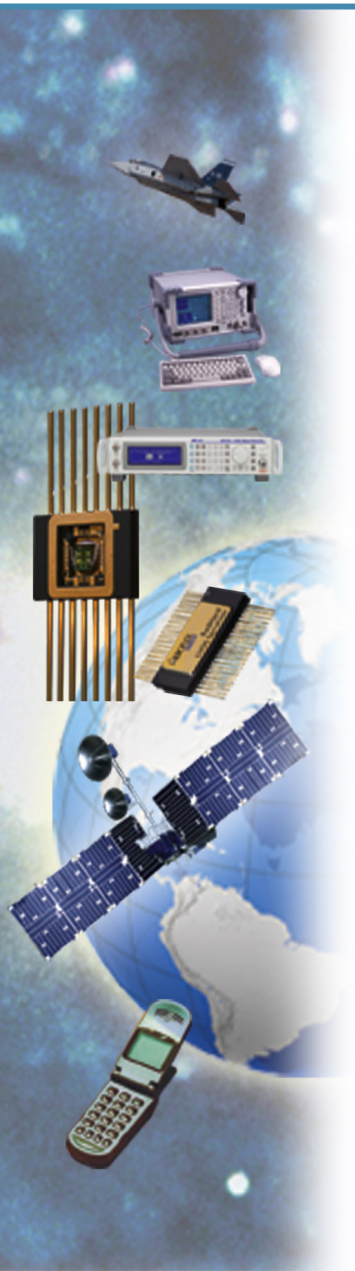


Next Generation Multipurpose Microprocessor

Activity Overview

DASIA 2010

June 1st, 2010

www.aeroflex.com/gaisler

Overview

- NGMP is an ESA activity developing a multi-core system with higher performance compared to earlier generations of European Space processors
- Part of the ESA roadmap for standard microprocessor components
- Aeroflex Gaisler's assignment consists of specification, the architectural (VHDL) design, and verification by simulation and on FPGA
- An FPGA prototype will be delivered by the end of 2010 and followed by synthesis on ASIC technology
- This presentation is an overview of the first part of NGMP development and covers:
  - Schedule
  - Overview of the hardware architecture
  - New features, target technology, open items
  - Software support (toolchains, OSs, drivers)
  - Additional development support (debugger, ISS)

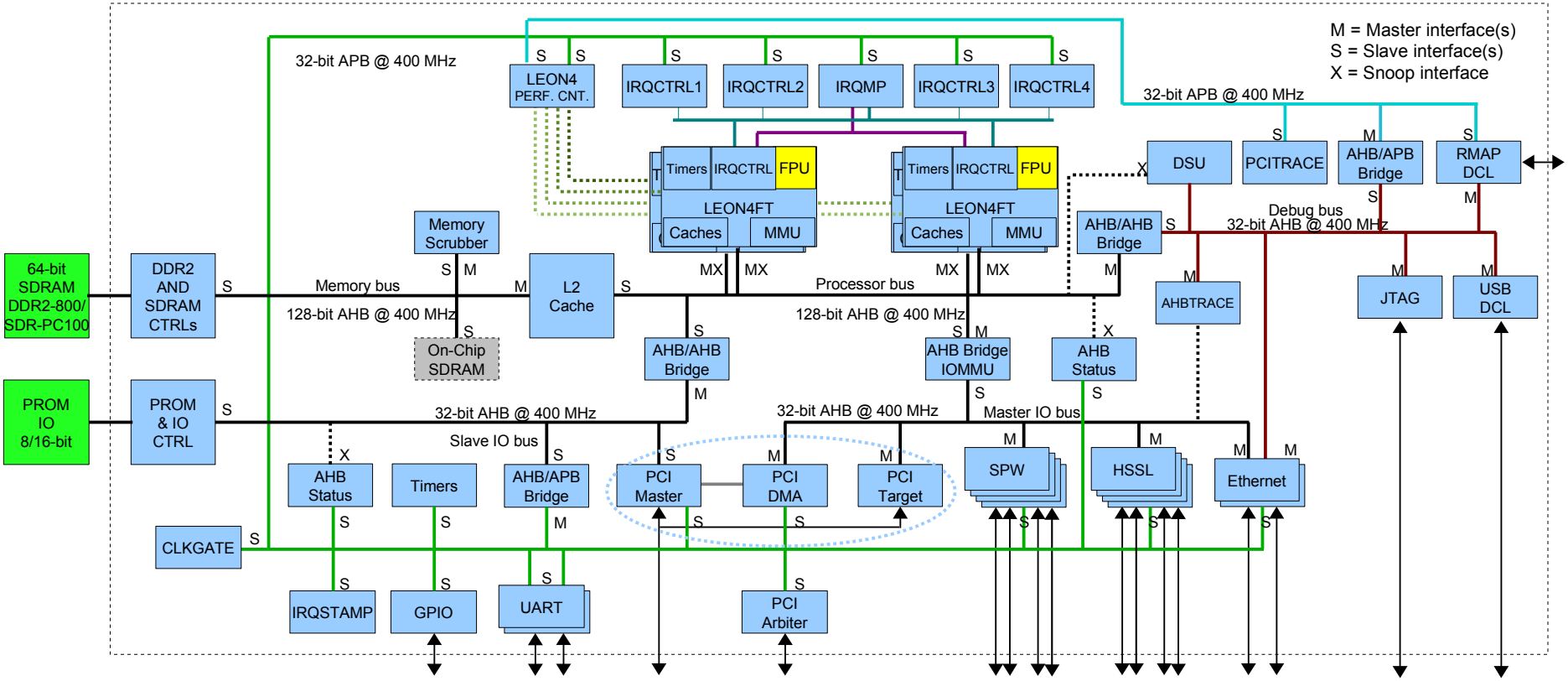
Development Schedule

- Aug 2009: Kick-off
- Feb 2010: Definition and specification
- June 2010: First versions of FPGA prototypes
- Dec 2010: Final RTL code, FPGA Demonstrator
- Aug 2011: Verified ASIC netlist
- Manufacturing of prototype parts not yet decided
- Development of flight model in a separate contract

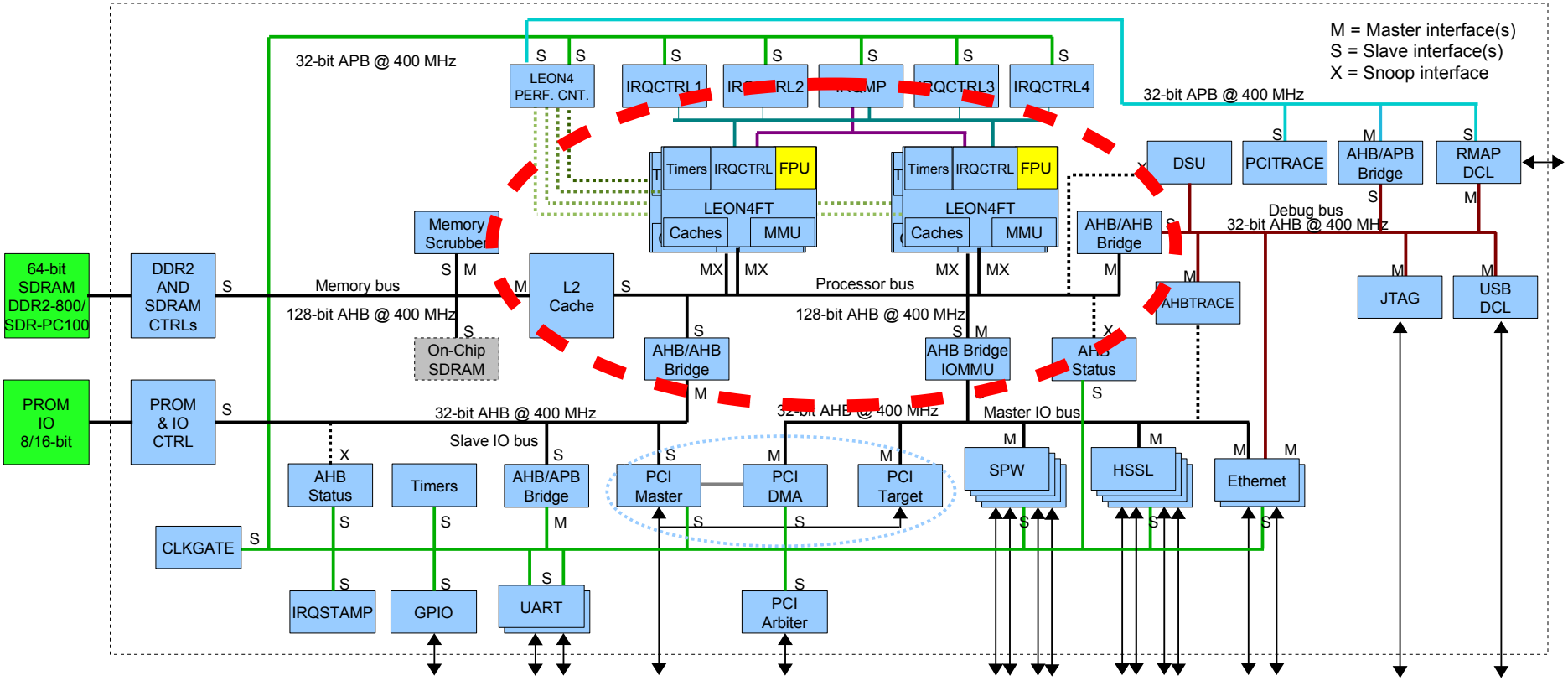
Architectural Overview

- Quad-core LEON4FT with GRFPU floating point units
- 128-bit L1 caches, 128-bit AHB bus
- 256 KiB L2 cache, 256-bit cache line, 4-way LRU
- 64-bit DDR2-800/SDR-PC100 SDRAM memory interface
- 32 MiB on-chip DRAM (if feasible)
- 4x GRSPW2 SpaceWire cores @ 200 Mbit/s
- 32-bit, 66 MHz PCI interface
- 2x 10/100/1000 Mbit Ethernet
- 4x HSSL (if available on target technology)
- Debug links: Ethernet, JTAG, USB, dedicated SpW RMAP target
- Target frequency: 400 MHz
- Maximum power consumption: 6W. Idle power 100 mW.

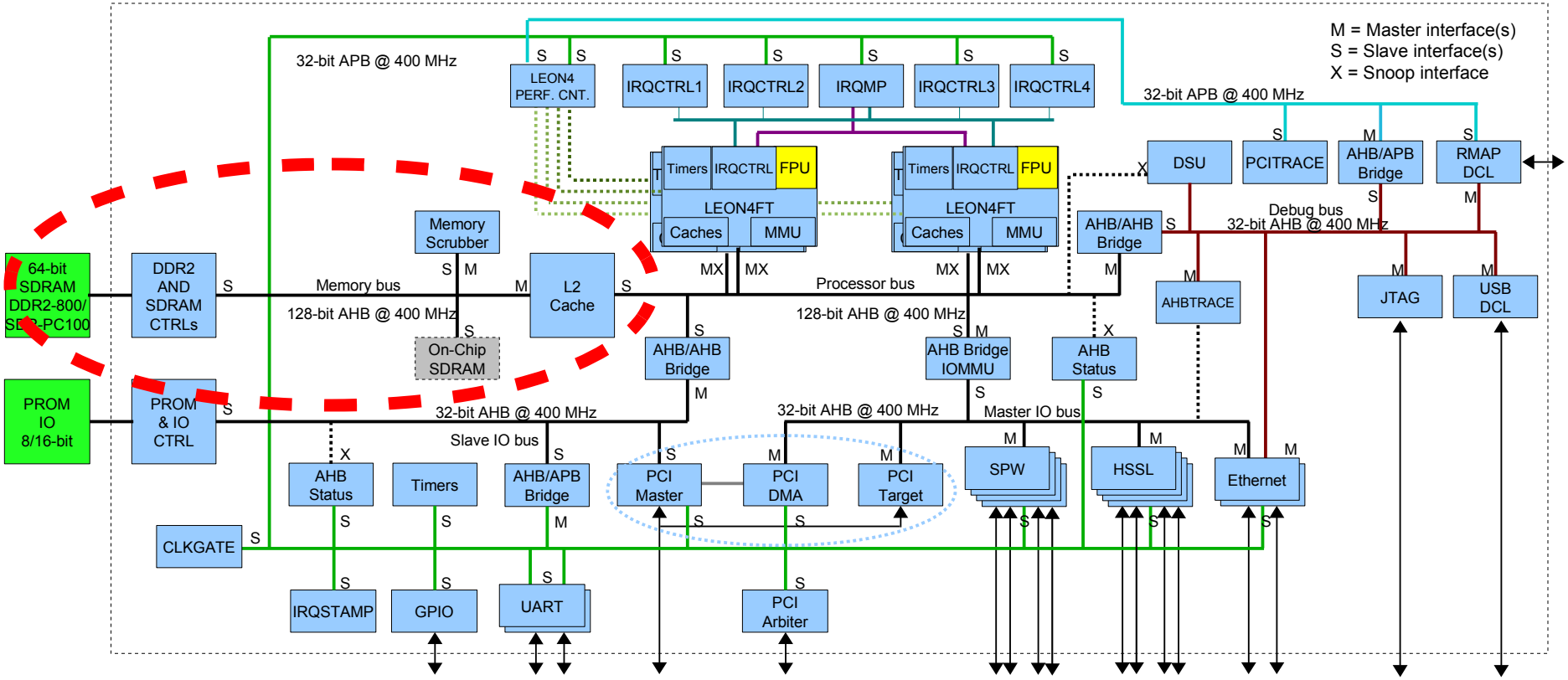
Architectural Overview



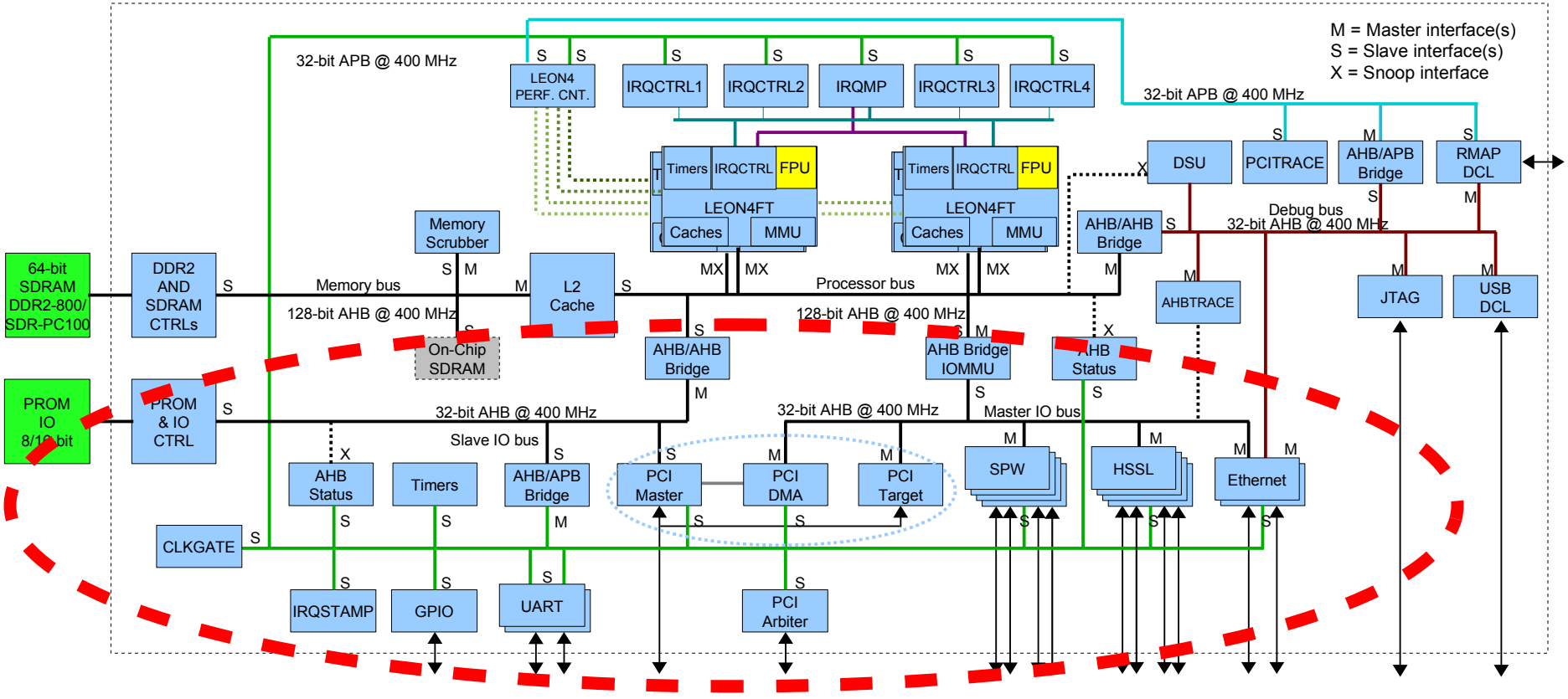
Architecture – Processor bus



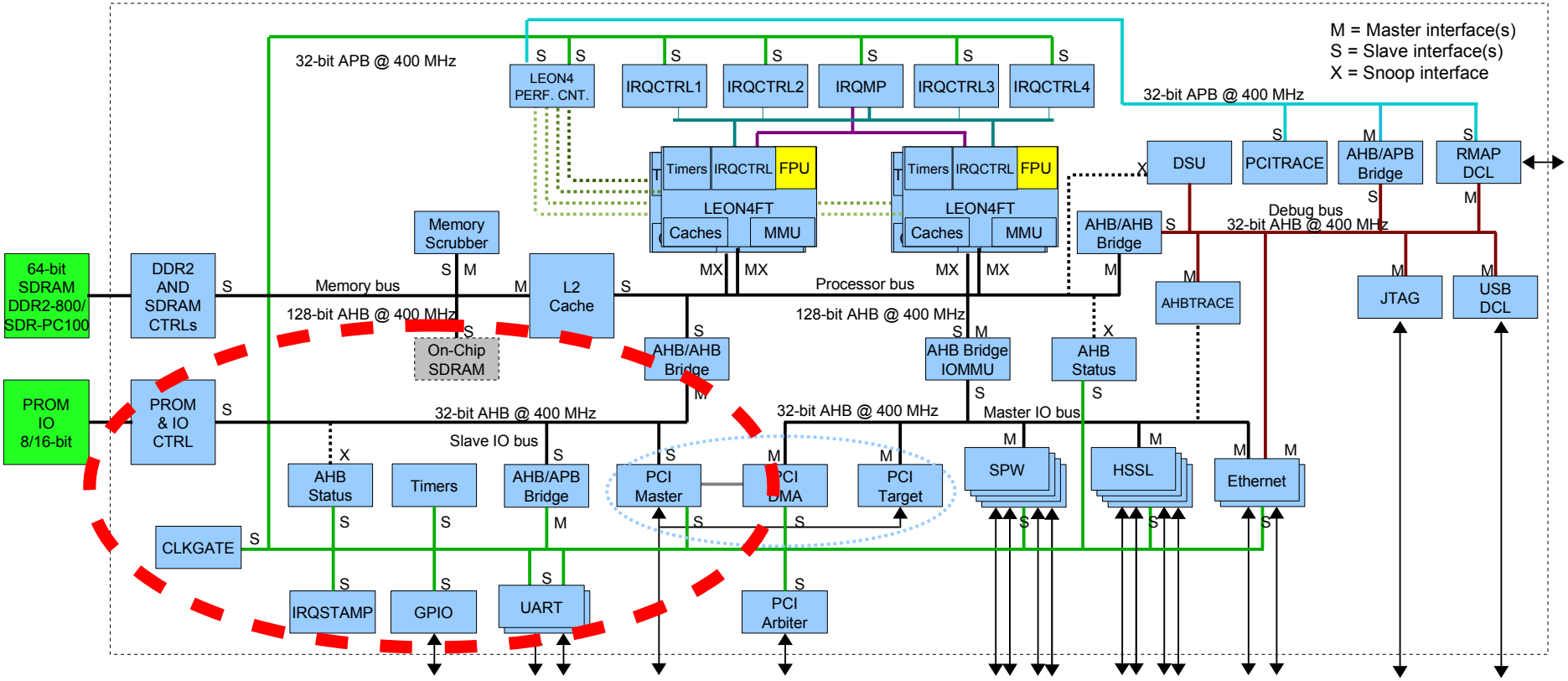
Architecture – Memory bus



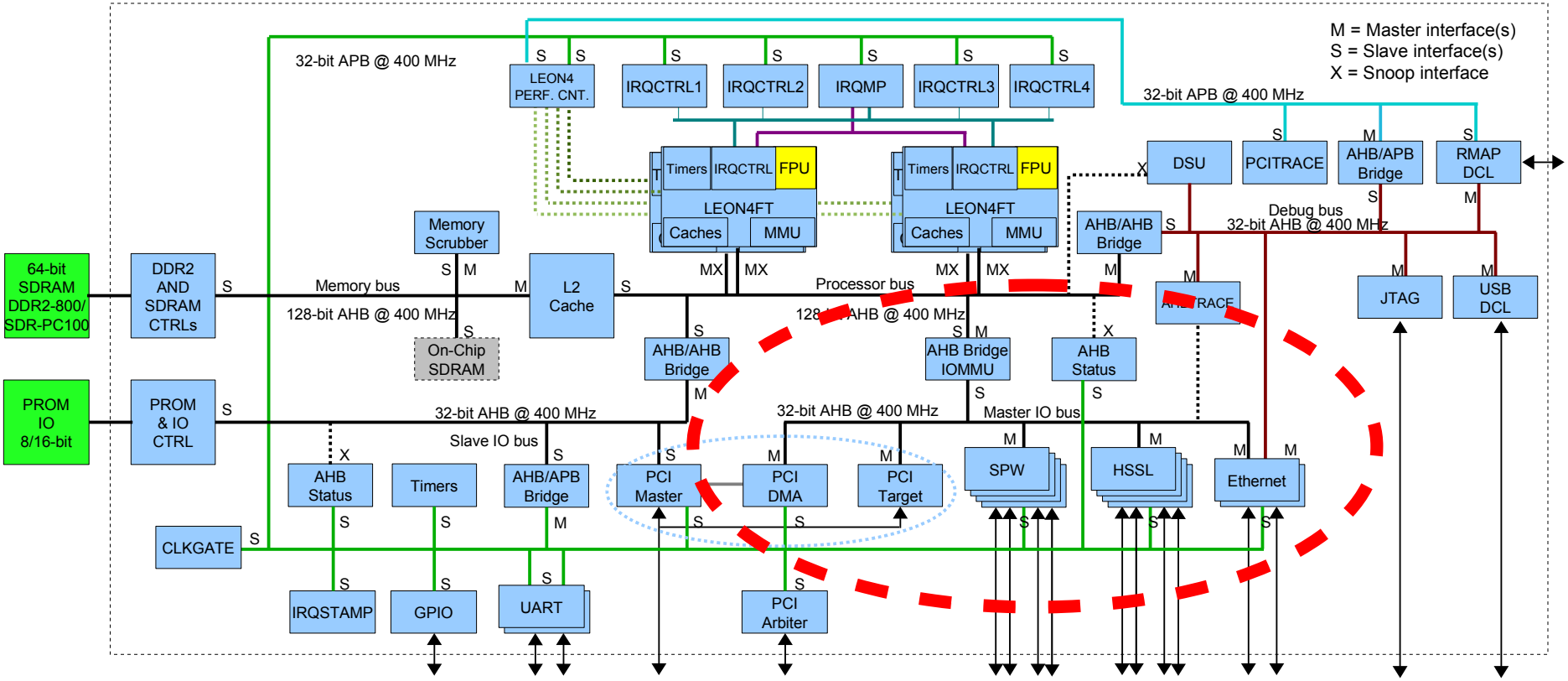
Architecture – I/O buses



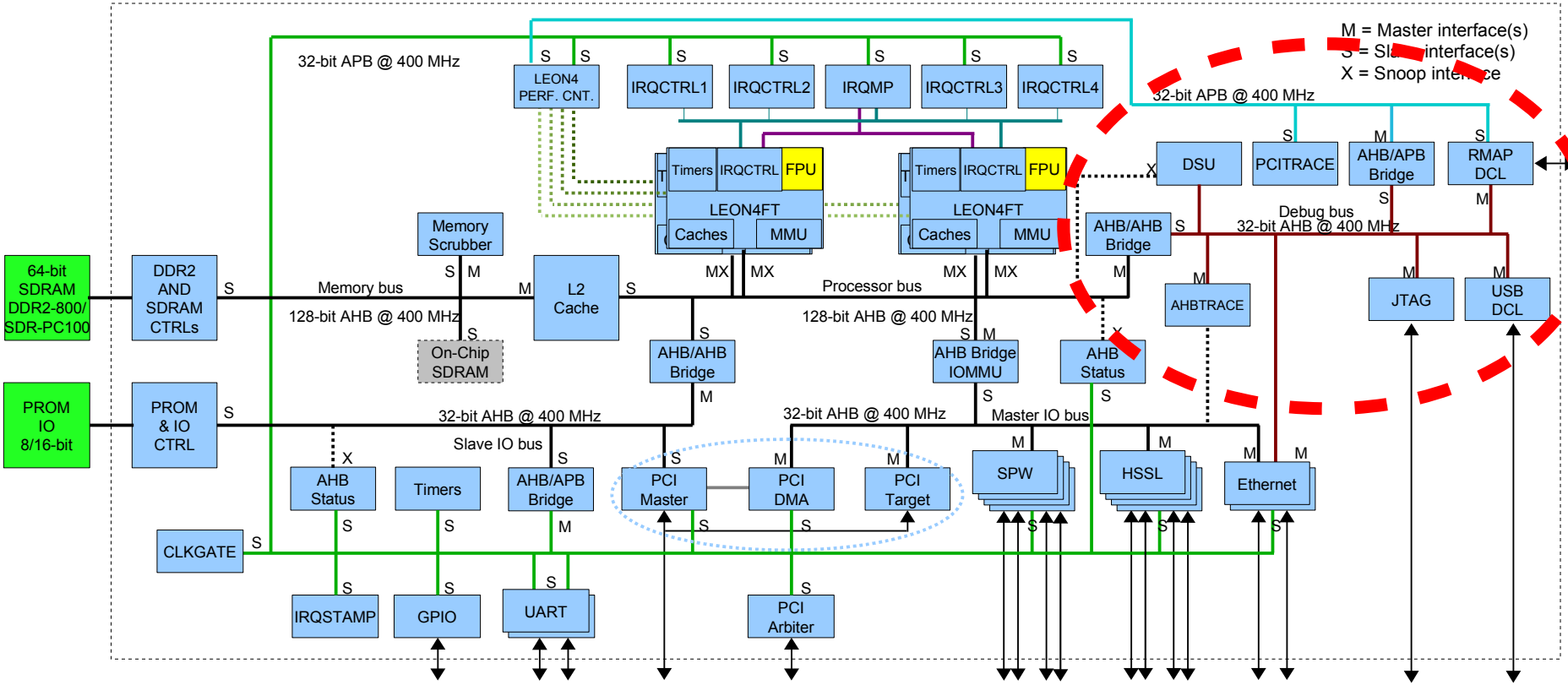
Architecture – Slave I/O bus



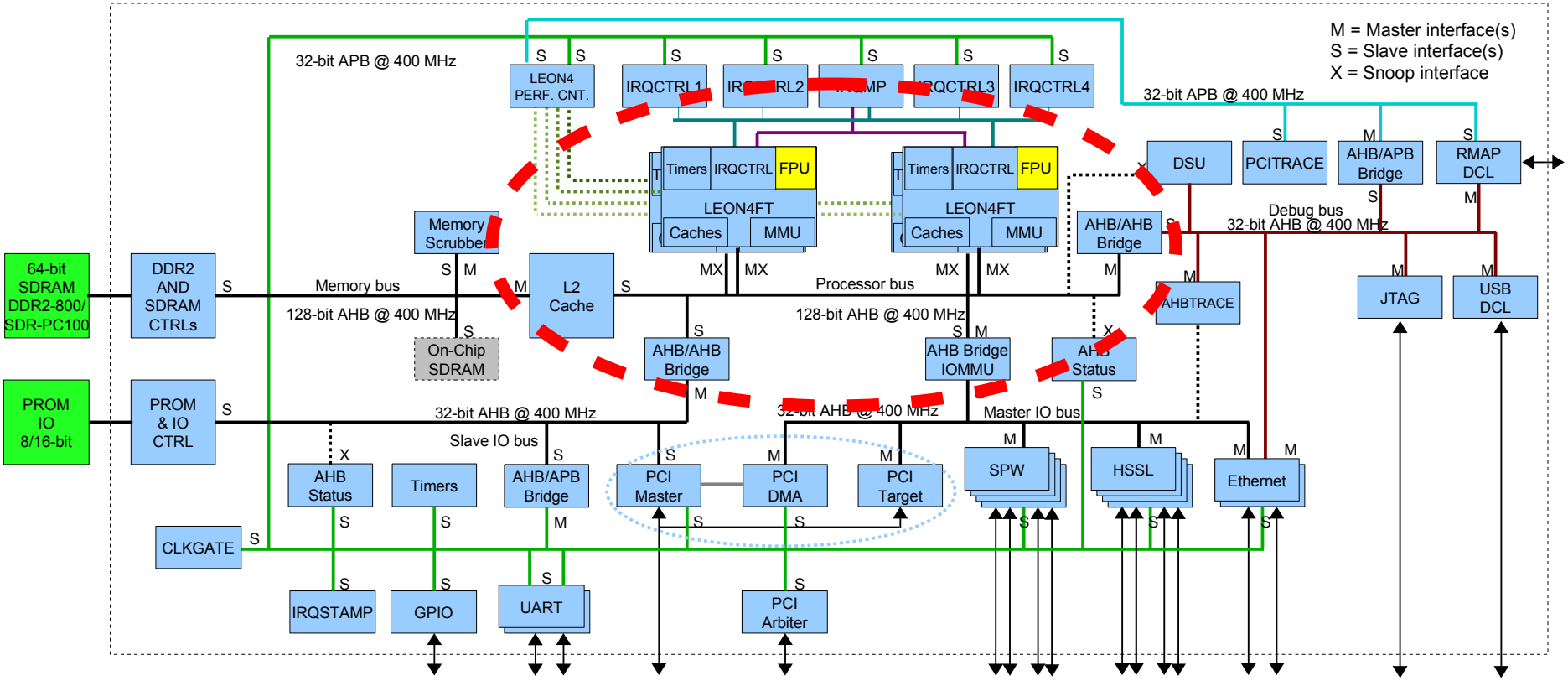
Architecture – Master I/O bus



Architectural Overview – Debug bus

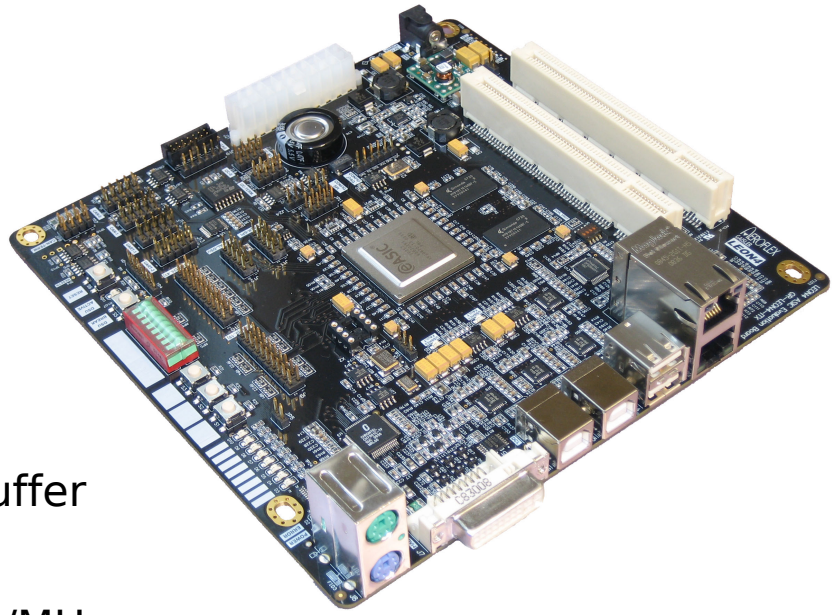


Architecture – Processor bus



Architecture - LEON4FT

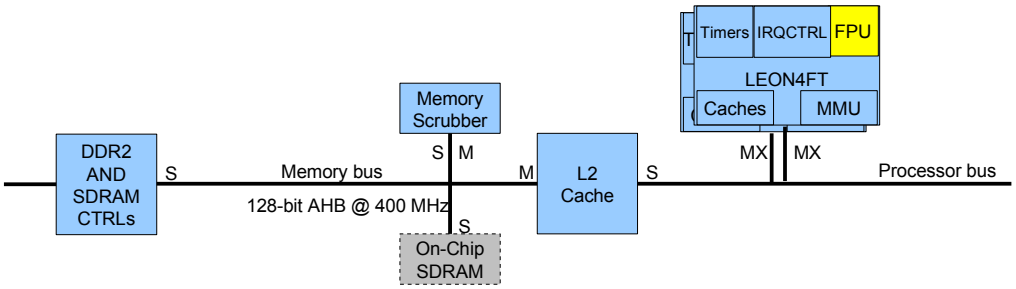
- IEEE-1754 SPARC V8 compliant 32-bit processor
- 7-stage pipeline, multi-processor support
- Separate multi-set L1 caches with LRU/LRR/RND, 4-bit parity
- 64-bit single-clock load/store operation
- 64-bit register file with BCH
- 64- or 128-bit AHB bus interface
- Write combining in store buffer
- Branch prediction
- CAS support
- Performance counters
- On-chip debug support unit with trace buffer
- Local timer and interrupt controller
- 1.7 DMIPS/MHz, 0.6 Wheatstone MFLOPS/MHz
- Estimated 0.35 SPECINT/MHz, 0.25 SPECFP/MHz
- 2.1 CoreMark/MHz (comparable to ARM11)



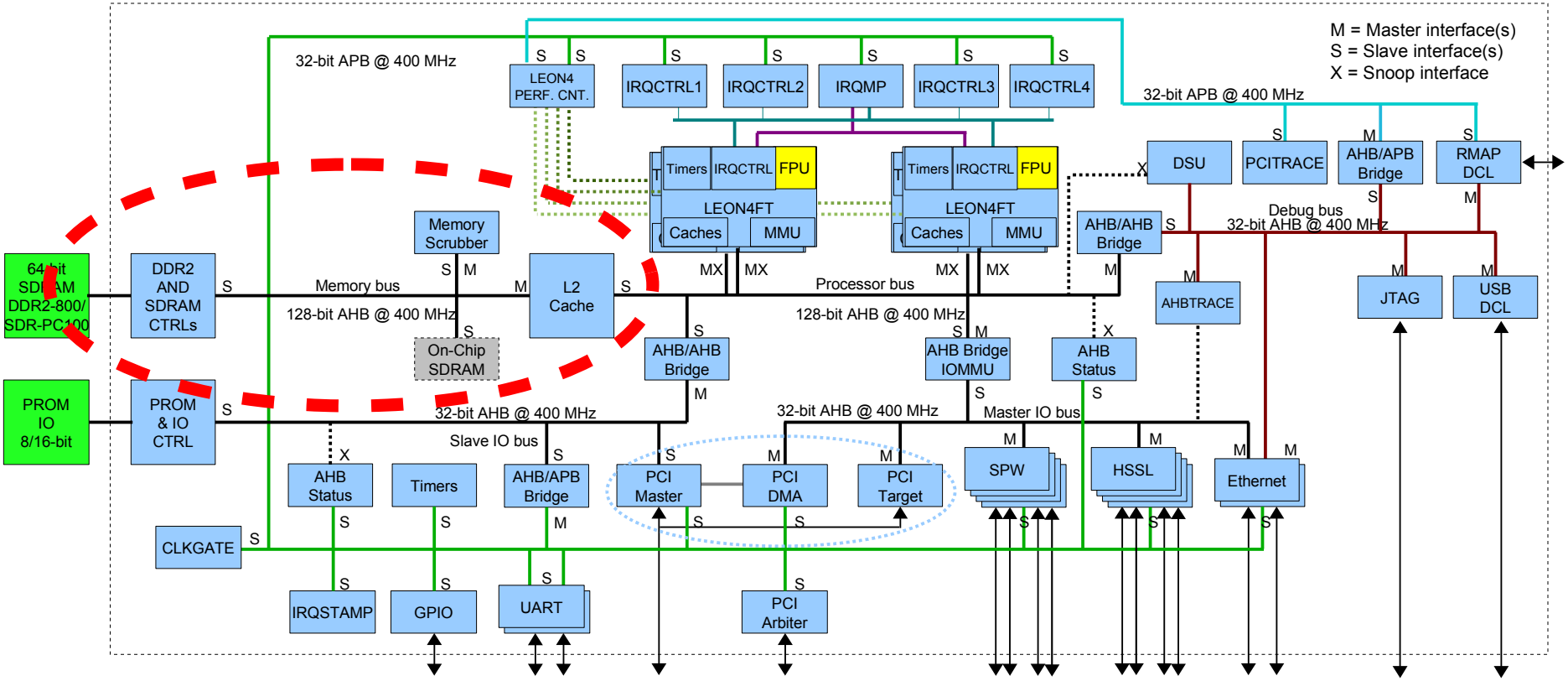
SPARC Compliant SCD V8

Architecture - L2 Cache

- 256 KiB baseline, 4-way, LRU
- 256-bit internal cache line with 64-bit BCH ECC
- Copy-back and write-through operation
- 0-waitstate pipelined write, 3/4-waitstates read hit
- Support for locking one more more ways
- Fence registers for backup software protection
- Essential for SMP performance scaling
- Reduces effects of slower memory (SDRAM) if DDR2 cannot be used

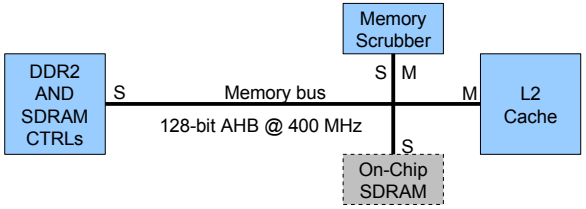


Architecture – Memory bus



Architecture - Memory scrubber

- Can access external DDR2/SDRAM and on-chip SDRAM
- Performs the following operations:
  - Initialization
  - Scrubbing
  - Memory re-generation
- Configurable by software
- Counts correctable errors with option to alert CPU
- User can define data pattern used for initialization

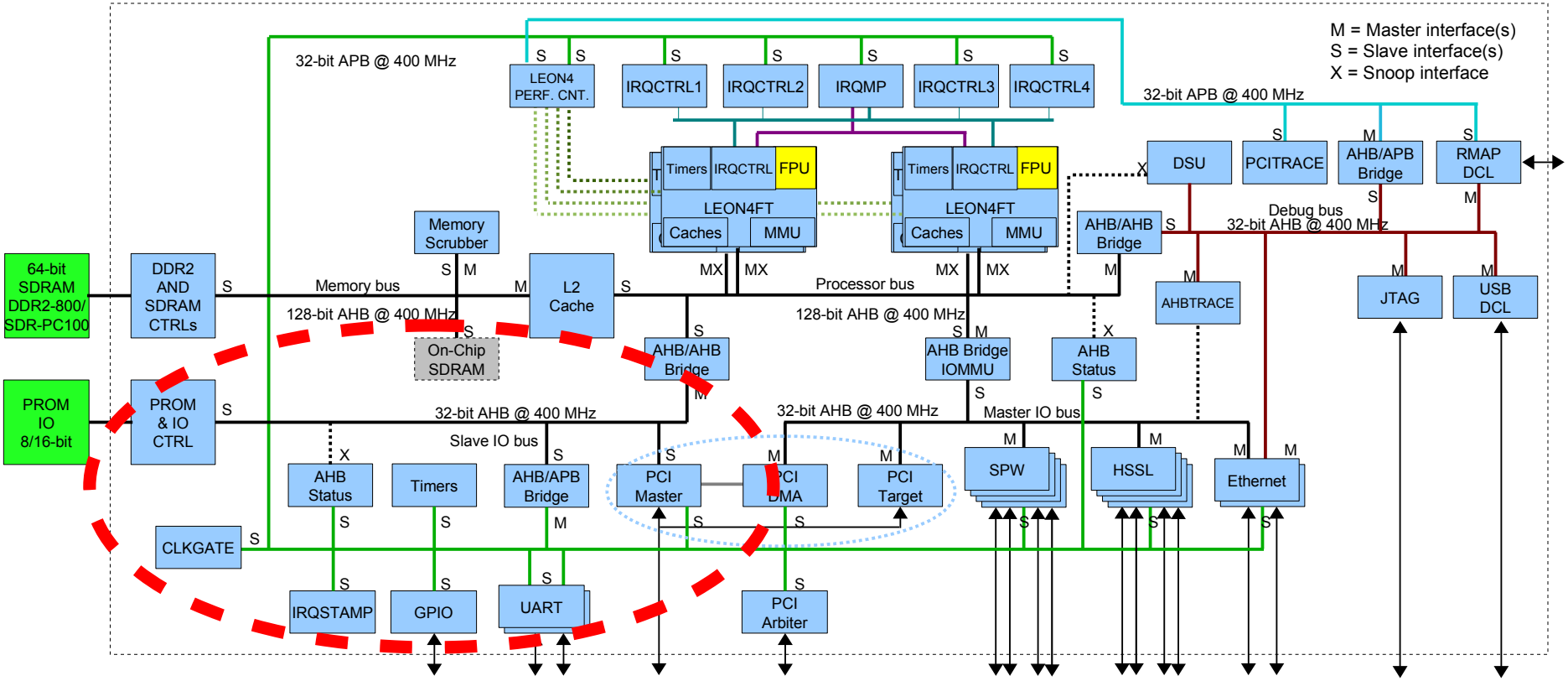


Architecture - Memory Controllers

- Primary memory interface: DDR2/SDRAM
  - DDR2-800/SDRAM PC100
  - 64-bit data
  - 16 and 32 bit Reed-Solomon ECC
  - Corrects two or four 4-bit errors
- On-chip SDRAM (if available on target tech.)
- Performance of external interfaces:

Interface	Cache line fetch (ns)	Sustainable bandwidth (MiB/s)	Min. sys. freq. (MHz)	Max. sys. freq. (MHz)
SDRAM PC100	100	320	-	400
DDR2-800	42.5	512	62.5	400

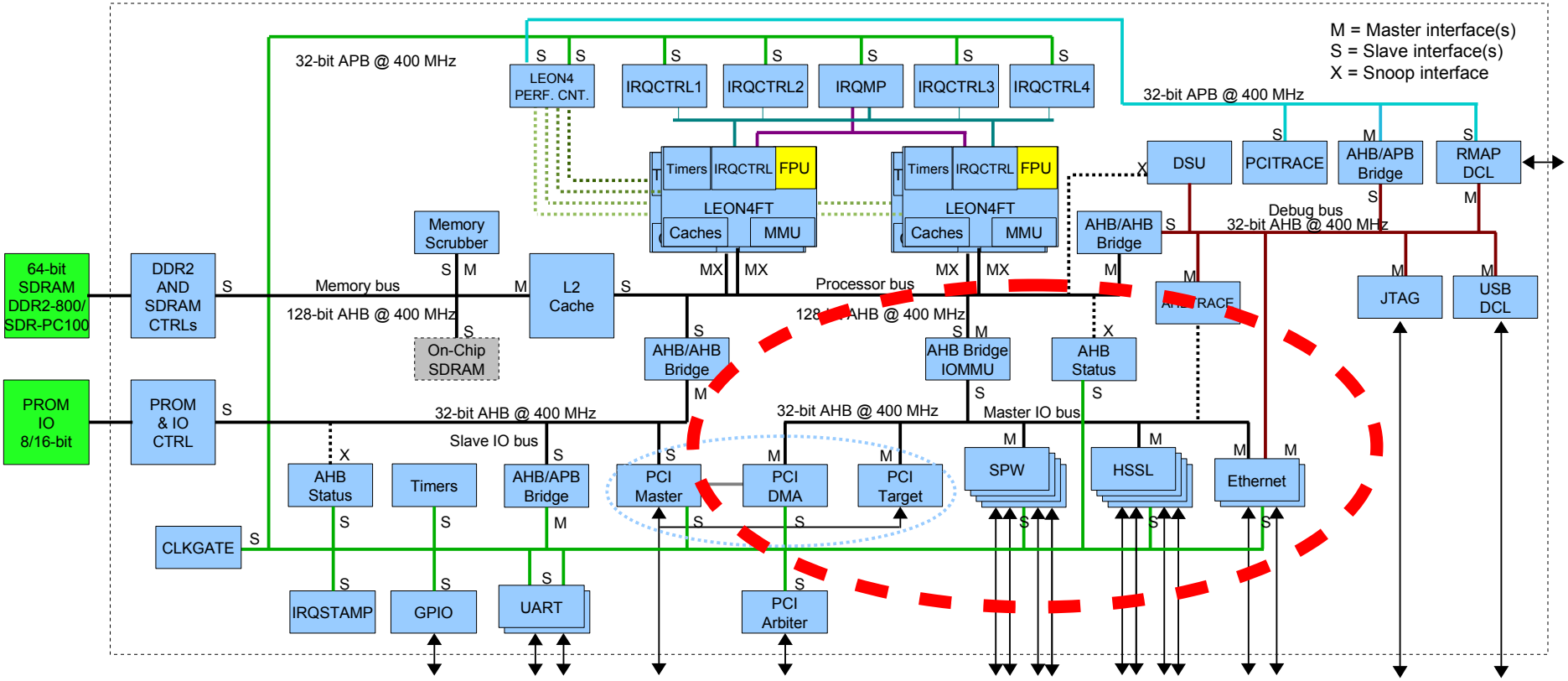
Architecture – Slave I/O bus



Architecture – Slave I/O bus cores

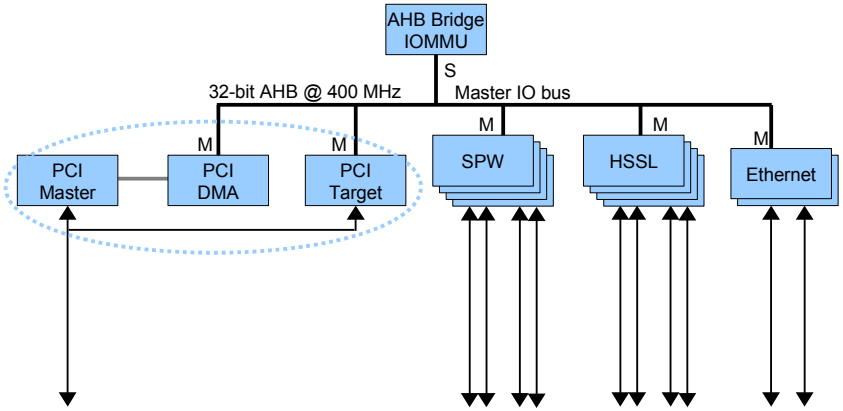
- Uni-directional AHB/AHB bridge
  - Reduced load on Processor bus
  - Performs read/write combining
- 8/16-bit PROM/IO controller with BCH ECC
- PCI master AHB slave interface
- AHB/APB bridges connecting all APB slave interfaces to be used in flight: Timers, UARTs, interrupt controllers, GPIO port, PCI arbiter, clock gating unit, SpaceWire controller, Ethernet MACs, interrupt time stamp unit, etcetera
- All core registers are placed on 4 KiB boundaries

Architecture – Master I/O bus



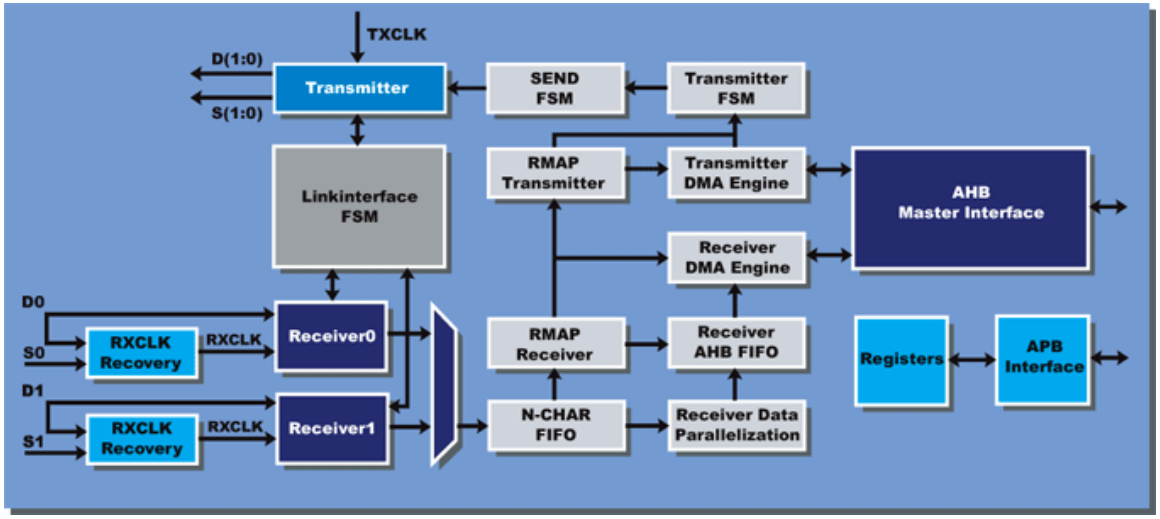
Uni-directional AHB bridge with IOMMU

- Connects all DMA capable I/O master through one interface onto the Processor bus
- Performs pre-fetching and read/write combining
- Provides address translation and access restriction
- Will not be required to use the same page tables as the processor
- Master can be placed in groups where each group can have its own set of page tables



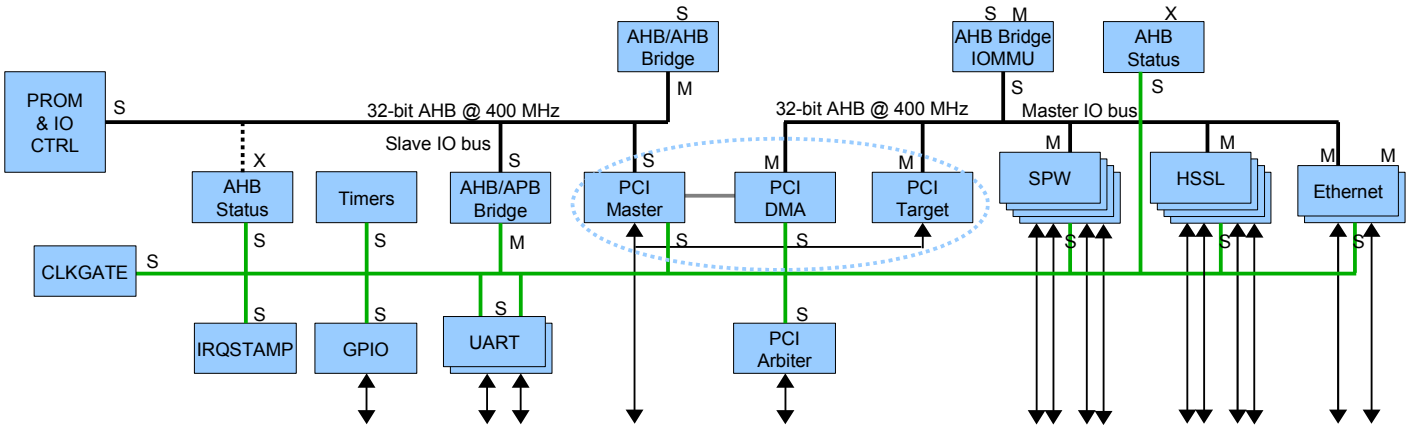
Architecture - Spacewire

- 4x Aeroflex Gaisler GRSPW2 cores
- Maximum link bit rate will be at least 200 Mb/s
- Hardware RMAP target in each core
- Two ports per core (redundant port)
- Each core has its own DMA engine



Architecture - PCI interface

- Provides PCI master/target interface
- 32-bit interface supporting 66 MHz operation
- Target DMA interface is placed on the Master I/O bus while the AHB slave interface is on the Slave I/O bus
- Target has two bars of sizes 256 MiB and 64 MiB
- Specification based on GRPCI core. AG is currently developing a new core which is planned to replace GRPCI.

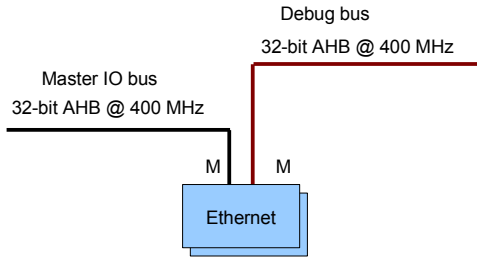


High-Speed Serial Link

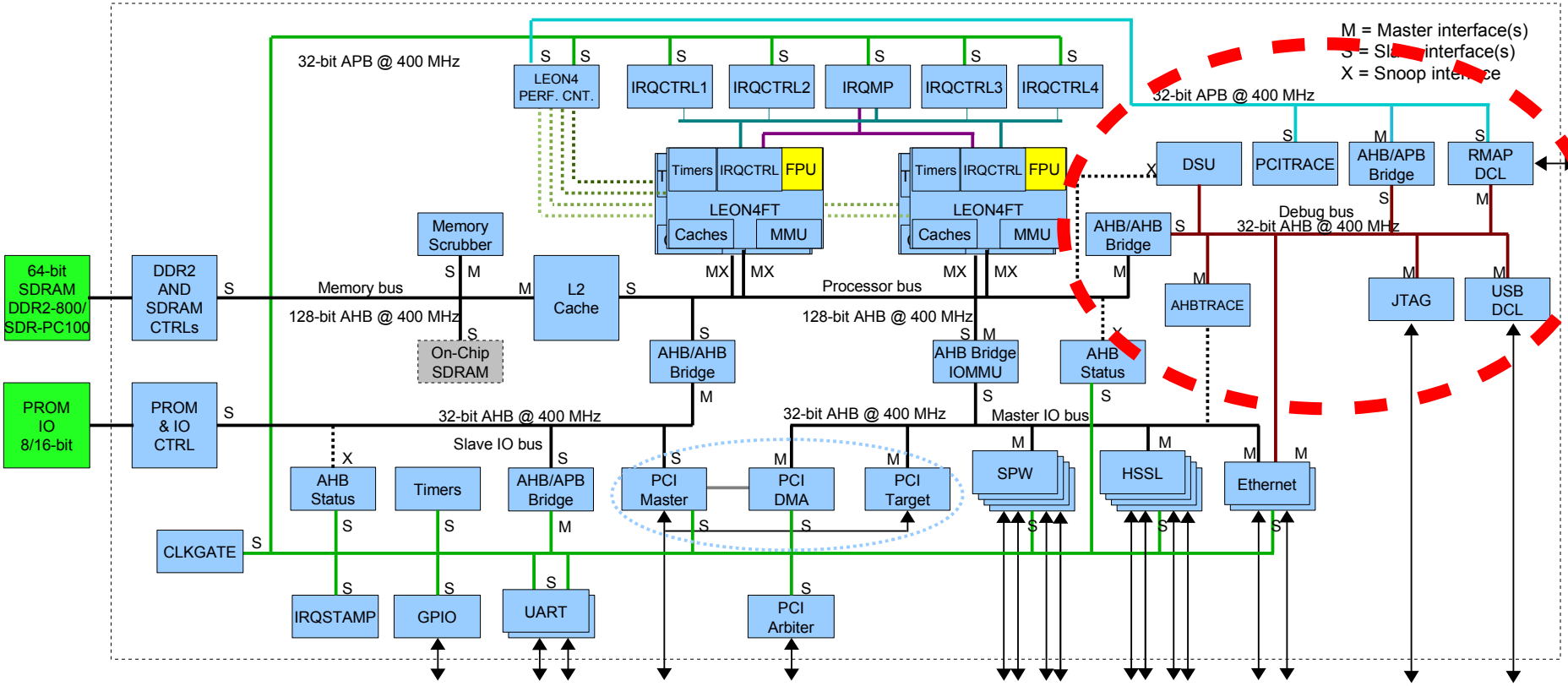
- Design has been specified to include 4 HSSL cores
- The High-speed Serial Link back-end is TBD
- Inclusion of HSSL depends on availability of macros on target technology
- Current status: Target technology will have SerDes macros capable of 6.25 Gbit/s operation
- AG is working with ESA to, at a minimum, be able to provide a simple descriptor based DMA cored based on GRETH_GBIT or GRSPW2

Gigabit Ethernet

- 2x Ethernet interfaces
- Supports 10/100/1000 Mbit in both full- and half-duplex
- DMA engine for both receiver and transmitter
- Internal buffer allows core to buffer a complete packet
- Supports MII and GMII interfaces to connect an external transceiver
- Supports scatter gather I/O and IPv4 checksum offloading
- Provides Ethernet Debug Communication Link
- 2 KiB EDCL buffer → 100 Mb/s
- Soft configurable EDCL IP/MAC addresses
- EDCL can also be connected to Debug bus

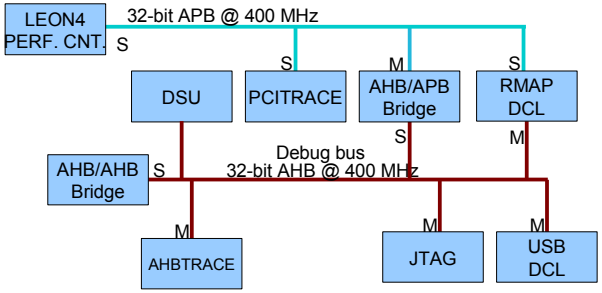


Architectural Overview – Debug bus



Architecture - Cores on Debug bus

- Debug Support Unit
  - Hardware breakpoints/watchpoints
  - Supports debugging multiple cores in parallel
  - Used to monitor processor status
  - Interface to instruction and (Processor bus) AHB trace
- PCI trace buffer
- AHB trace buffer monitoring Master I/O bus
- APB bridge allows direct access to LEON4 statistics unit
- Wide range of debug communication links



Debug Communication Links

- JTAG Debug Communication Link
  - Bandwidth: 500 kb/s
- RMAP target
  - Bandwidth: 20 Mb/s
  - Provides DSU access over SpW
- USB Debug Communication Link
  - Bandwidth: 20 Mb/s
- Ethernet Debug Links
  - Bandwidth: 100 Mb/s
  - Can optionally be connected to master I/O bus

Improved Debugging Support

The NGMP will have improved debugging support compared to the LEON2FT and many existing LEON3 implementations. The new features include:

- Several high-speed debug interfaces
- Non-intrusive debugging through dedicated Debug bus
- AHB trace buffer with filtering
- Instruction trace buffer with filtering
- Hardware data watchpoints
- Data area monitoring

Improved Profiling Support (1)

The NGMP has improved profiling support compared to the LEON2FT and LEON3. The new features allow to measure the following metrics:

- Processor statistics
  - Instruction/Data cache/TLB miss/hold
  - Data write buffer hold
  - Total/Integer/FP instruction count
  - Branch predication miss
  - Total execution time (excluding debug mode)
  - Special filters allow counting number of:
    - Integer branches
    - CALL instructions
    - Regular type 2 instructions
    - LOAD and STORE instructions
    - LOAD instructions
    - STORE and instructions

Improved Profiling Support (2)

In addition the processor statistics you can also measure:

- L2 cache hit/miss rate
- AHB utilization
  - AHB utilization per master
  - Total AHB utilization

- Interrupt time stamp unit allows users to measure interrupt handler latencies

Summary of New Features

- Features in NGMP not found in most present day LEON/LEON-MP architectures:
  - Quad core LEON4FT
  - L2 cache with locking
  - Large on-chip RAM (32 MiB, if available on target)
  - Wider AMBA buses
  - Better support for partitioning:
    - IOMMU
    - Per-processor timers and interrupt cntrlrs
  - Improved debug support (# links, filters, perf. cnt)
  - Improved support for AMP
  - Boot options (PROM, RMAP)
  - Interrupt time stamping
  - Hardware memory scrubber

Target technology

- Baseline is ST 65nm space technology
- Requirements
  - DDR2 PHY
  - I/O standards: LVTTL, SSTL, PCI
  - Memory:
    - 1-port RAM, 2-port RAM
    - High density 1-port RAM/SDRAM
- Backup options:
  - UMC 90 nm with DARE library
  - Tower 130 nm with Ramon library

Operating Systems

- Operating systems that will be ported in this activity:
  - RTEMS 4.8 and 4.10
  - WindRiver VxWorks 6.7 with SMP support
  - eCos 2.0
  - Linux 2.6
- Other OSs already ported to LEON include:
  - LynxOS (LynuxWorks)
  - ThreadX (Express Logic)
  - Nucleus (Mentor Graphics)

Toolchain

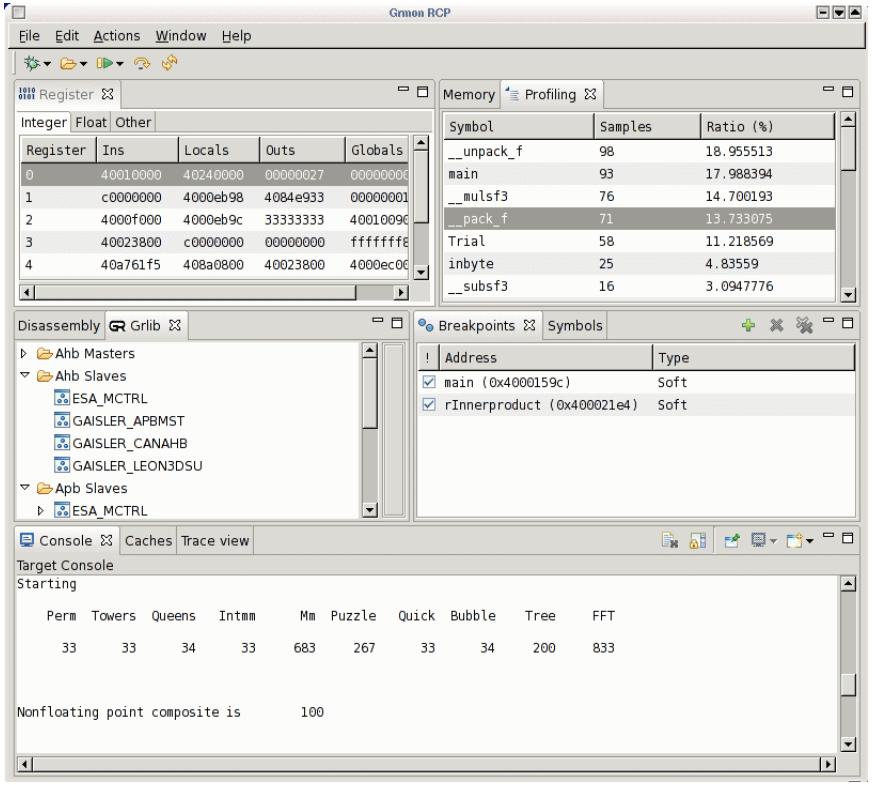
- The GNU C/C++ toolchain will be used
- Versions 4.1.2 and 4.4.2 have been successfully tested
- OpenMP requires GCC 4.4+ and a pthreads implementation
- RTEMS 4.8 uses GCC 4.2.4, RTEMS 4.10 uses GCC 4.4
- VxWorks 6.7 uses GCC 4.1.1
- MKPROM2 with support for booting SMP and AMP systems

Simulator

- NGMP simulator based on GRSIM
- C models of IP cores linked into a final simulator
  - LEON4
  - L2 cache and DDR memory interface
  - GRSPW, GRETH, GRPCI
- Reentrant and thread safe library
- Accuracy goal is above 90% over an extended simulation period

Debug tools

- NGMP will be fully supported by the GRMON debug monitor
- Complemented by standard RTOS trace tools



Thank you for listening

For updates and to download the NGMP specification, please see:

http://microelectronics.esa.int/ngmp/ngmp.htm

EXTRA SLIDES

Selection of Open Items

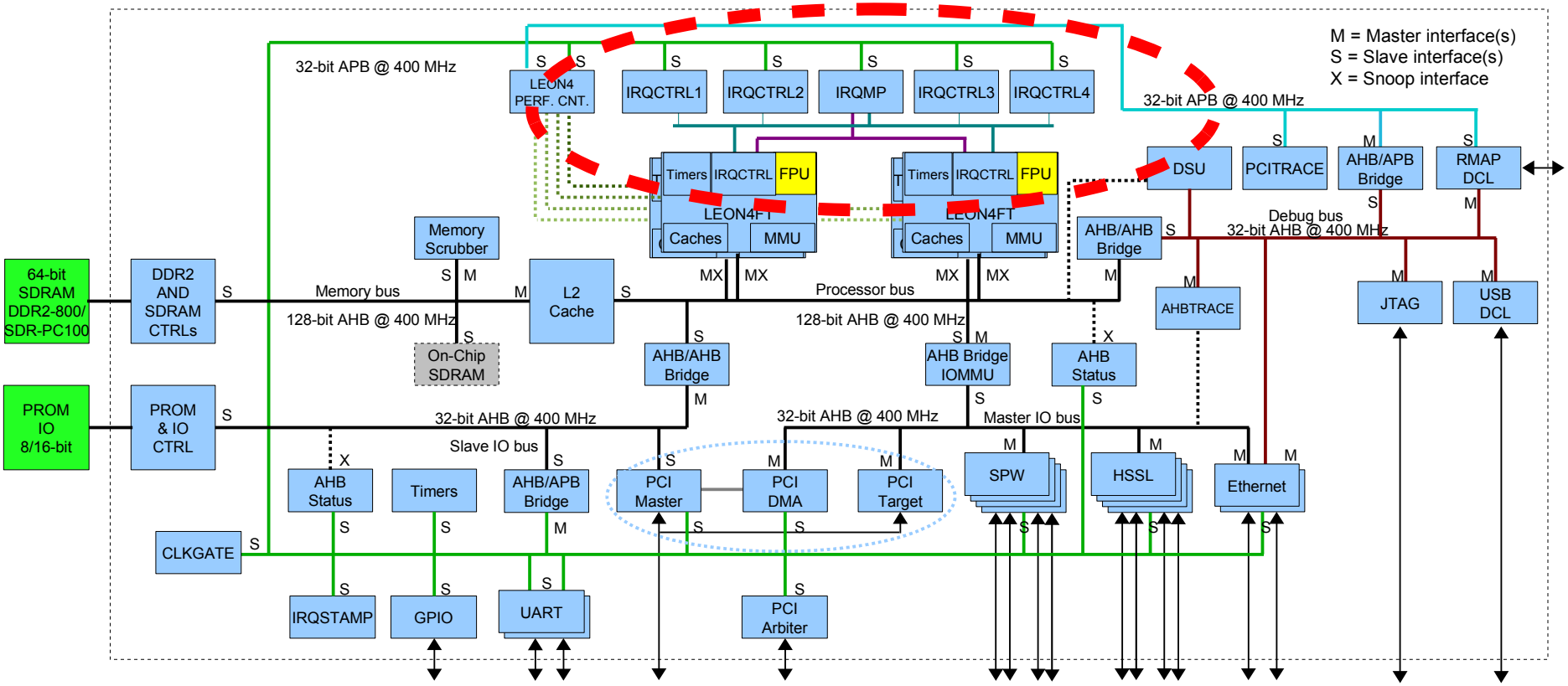
Choices that are still open include:

- On-chip DRAM (desirable but not likely to be included)
- 2 or 4 CPU cores
- Shared or individual FPUs (3 possible configurations)
- External memory type (DDR/DDR2)
- Configurable SDRAM width (32/64 data bits)
- L1/L2 cache size
- IOMMU implementation
- High-speed interfaces
- Different frequencies of processor bus and other buses
- Spare-column of external memory

Fault-Tolerance Summary

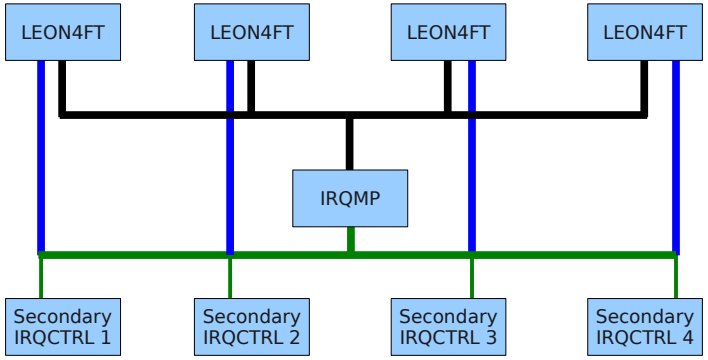
- Fault-tolerance in the NGMP system is aimed at detecting and correcting SEU errors in on-chip and off-chip RAM
- L1 cache and register files in LEON4FT are protected using parity and BCH
- L2 cache will use BCH
- External SDRAM will be protected using Reed-Solomon
- Boot PROM will use BCH
- RAM blocks in on-chip IP cores will be protected using BCH or TMR, smaller buffers can be synthesized as flip-flops
- Flip-flops will be protected with SEU-hardened library cells if available or TMR otherwise

Architecture – Interrupt infrastructure



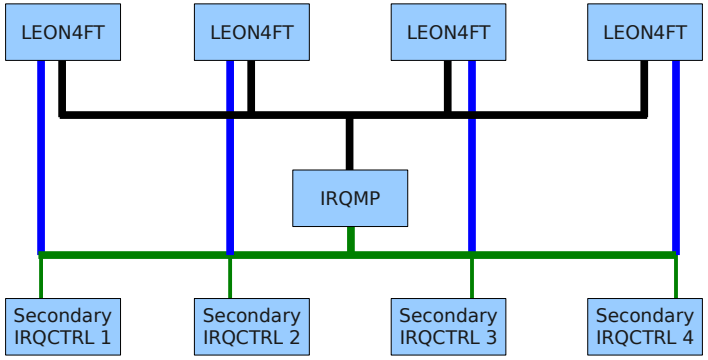
Interrupt infrastructure

- Specified to support AMP and SMP
- Internal processor interrupt controllers
- Shared multiprocessor interrupt controller (IRQMP)
- 4x secondary interrupt controllers
- General topology:



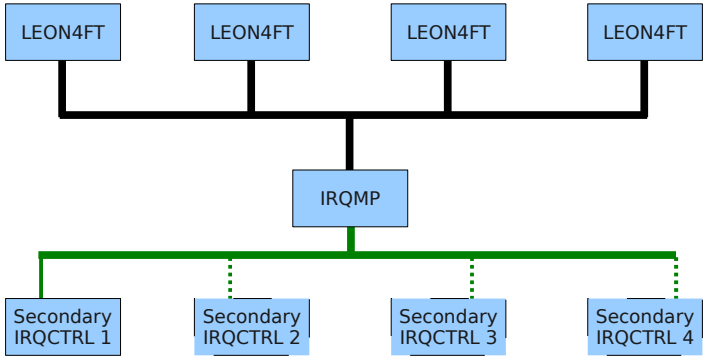
Interrupt infrastructure Cont..

- IRQMP is connected to each processor
- Each processor has an internal interrupt controller (not used when the processor core is listening to IRQMP)
- Each secondary interrupt controller is connected to IRQMP and to each internal interrupt controller.



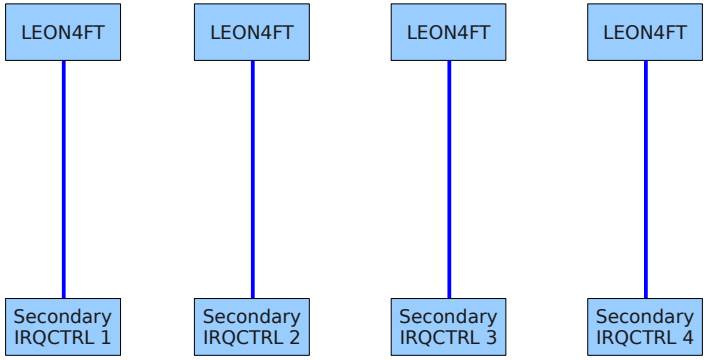
SMP Configuration

- All internal interrupt controllers are disabled
- Processor cores listen to IRQMP
- Mask register in IRQMP is used to listen to one or several of the secondary interrupt controllers



A(S)MP Configuration

- Processor cores use their internal interrupt controllers
- IRQMP is not used
- Each processor uses the internal interrupt controllers mask register to listen to one dedicated secondary interrupt controller



Interrupt infrastructure round-up

- Infrastructure also allows mixed configurations:
  - 1x SMP + (1x or 2x) AMP
- Synchronization via interrupts can be achieved via IRQMP or by writing the force register of a secondary interrupt controller
- Each configuration has the same view of the interrupt lines (local timers only available to the processor in which they are located)

Prototypes

- Investigations into ASIC prototypes is currently ongoing
- FPGA prototypes with reduced NGMP designs
  - Xilinx ML510
  - Synopsys HAPS-51
  - Aeroflex Gaisler GR-CPCI-XC4V with LX200 FPGA
  - Aeroflex Gaisler GR-PCI-XC5V