

Quad-Core LEON4

Next Generation Microprocessor

Evaluation Board

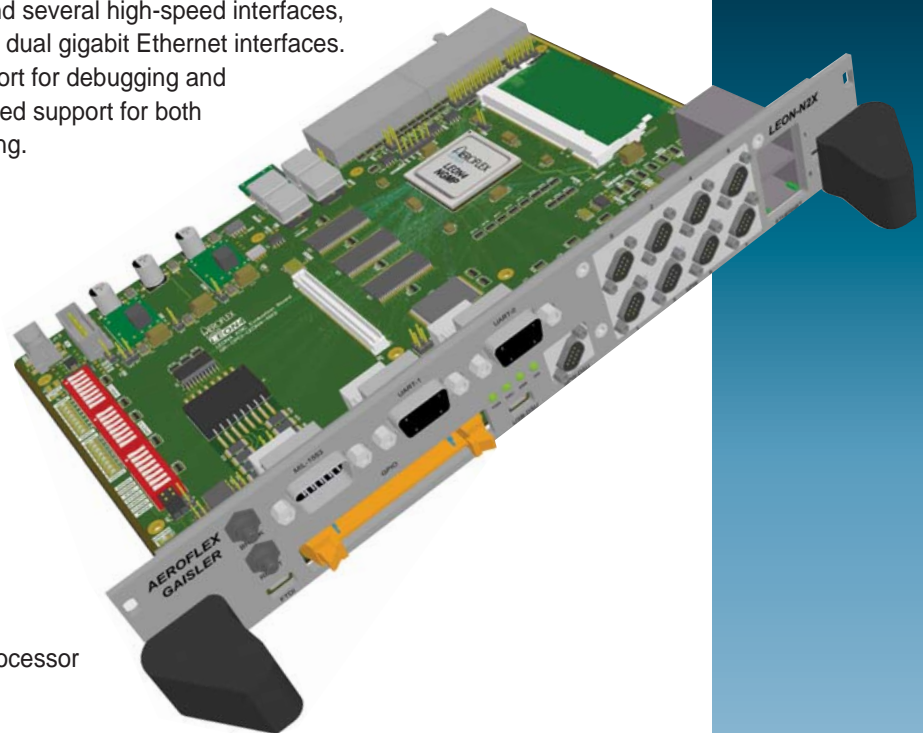
GR-CPCI-LEON4-N2X



Description

The GR-CPCI-LEON4-N2X evaluation board has been designed for evaluation of the Aeroflex Gaisler LEON4 Next Generation Microprocessor (NGMP) functional prototype device. The NGMP functional prototype is a system-on-chip with four 32-bit LEON4 SPARC V8 processor cores connected to a shared 256 KiB Level-2 cache and several high-speed interfaces, including an 8-port SpaceWire router and dual gigabit Ethernet interfaces. The architecture provides improved support for debugging and software partitioning together with extended support for both symmetric and asymmetric multiprocessing.

The board is a custom designed PCB in a 6U Compact PCI (CPCI) format, making the board suitable for stand-alone bench top development, or if required, to be mounted in a 6U CPCI Rack. The principle interfaces and functions are accessible on the front and back edges of the board, and secondary interfaces via headers on the board.



Features

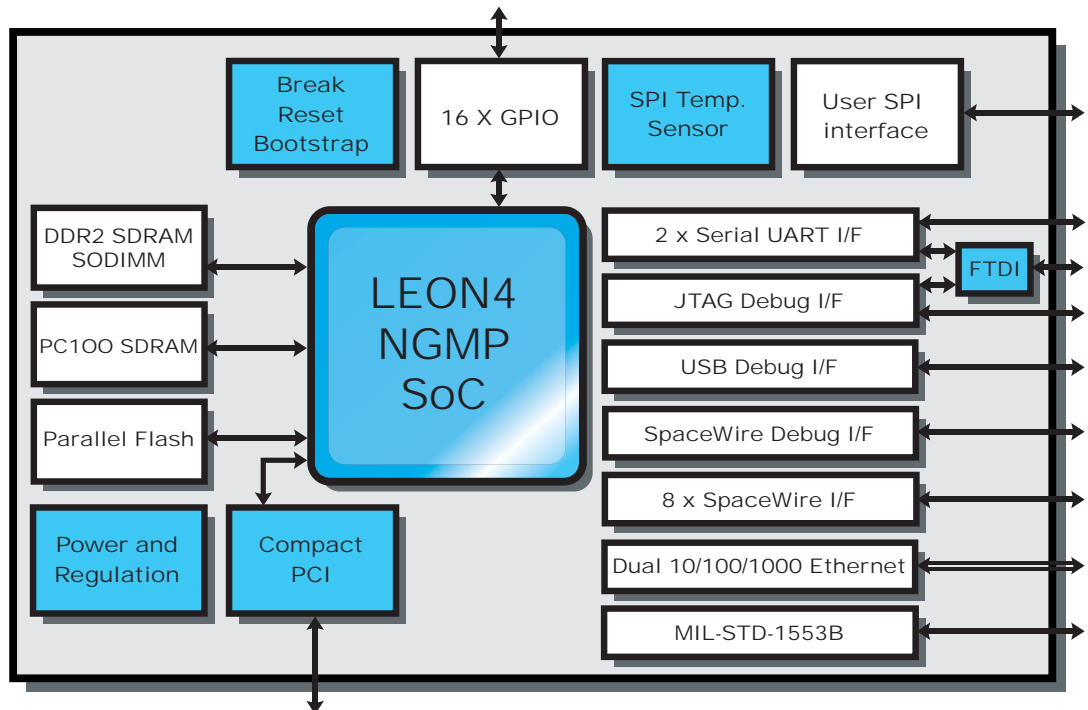
- Quad-Core 32-bit LEON4 SPARC V8 processor
- 6U Compact PCI format
- On board memory
 - DDR2 SDRAM SODIMM sockets, providing 96-bit wide interface with up to 2 GiB of data memory
 - PC100 SDRAM, 96-bit wide interface providing 128 MiB of data memory
 - NOR Flash PROM, 8 MiB, both 8- and 16-bit wide operation
- Debug communication links: SpaceWire, USB 2.0, Ethernet, JTAG
- Interfaces at front edge of board:
 - Dual 10/100/1000 Mbit Ethernet interface
 - Dual-redundant MIL-STD-1553B interface
 - 8-port SpaceWire interface
 - SpaceWire Debug Communication Link interface
 - 16 bit General Purpose I/O (ribbon cable style connector)
 - USB-to-Serial interface providing access to UARTs and JTAG debug interface
- Interfaces at back edge of board:
 - Compact PCI interface (32 bit, 33/66MHz), configurable for Host or Peripheral slot
 - Input power connectors for stand-alone use
- Interfaces on board:
 - DIP switches for GPIO and bootstrap signal configuration
 - LED indicators
 - SPI interface
 - Two Serial UART interface (RS232)
 - JTAG debug interface

LEON4 applications and support

The LEON4 processor is a fault-tolerant synthesizable VHDL model of a 32-bit processor compliant to the SPARC V8 architecture developed by Aeroflex Gaisler. For more information on the LEON4 core, the VHDL model, synthesis, configuration, hardware and software development tools, IP core developments and Real-Time Operating Systems, please refer to the Aeroflex Gaisler website (www.aeroflex.com/gaisler).

Specifications

- Aeroflex Gaisler LEON4 NGMP in FC896 package
- Processor core frequency: 150 MHz
- Compact PCI 6U form factor (233.5mm x 160mm)
- Memory
 - DDR2-800 SDRAM, 1 bank 96 bits wide, DDR2-SODIMM sockets
 - PC100 SDRAM, 1 bank 96 bits wide, 6x256 Mbit, discrete chips
 - Parallel Boot Flash (64 Mbit, both 8- and 16-bit wide operation)
- Dual RJ45 10/100/1000 Mbit GMII/MII Ethernet interface (KSZ9021GN with RJ45 jack)
- 8 SpaceWire interfaces (MDM9S)
- SpaceWire Debug Communication Link (MDM9S)
- USB 2.0 Debug Communication Link (ISP1504A with USB Mini-AB) interface
- 16 bit General Purpose I/O (34 pin 0.1" ribbon cable style connector)
- Dual-redundant MIL-STD-1553B Interface (DE9)
- FTDI Serial to USB interface (FT2232H with USB Mini-AB)
- DIP switches for GPIO signal configuration
- DIP switch for Memory interface configuration
- SPI interface user connections on 0.1" header
- SPI Temperature Sensor
- Two Serial UART interface (RS232) with DE9 female connectors
- JTAG Debug Communication Link
- Test connector for boundary scan
- 4-pin Molex style and 2.1 mm jack power connectors
- Push buttons for RESET and BREAK
- LED indicators for POWER, ERRORN, DSU active and GPIO
- Assorted jumpers and test points for configuration and test of the board
- Power, reset, clock and auxiliary circuits
- MMCX connectors for external clock sources
- AMP connector for memory mapped I/O



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