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Who we are: INAF

- Italian National Institute for Astrophysics http://www.inaf.it
- Areas of interest of the group
  - Computing system architectures
  - Fault-tolerant systems
  - Development of FPGA-based systems
- Activities
  - Research & Development
  - Education

FLIPPER GAME

Goal

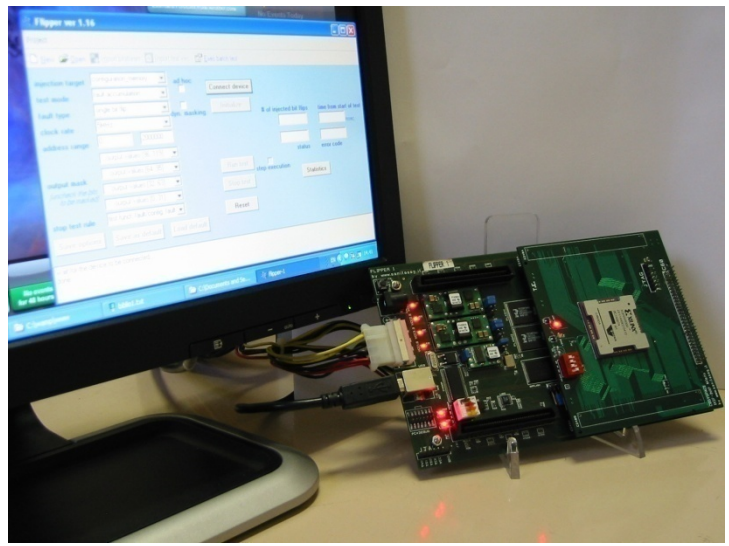
- Introduction of FLIPPER as a tool for evaluating SEU sensitivity of designs implemented in SRAM-FPGAs
- Examples of FLIPPER usage

Outline

- Main feature overview
- Recent results about validation
- Brief description of the FLIPPER-STAR-RoRA integrated flow

FLIPPER

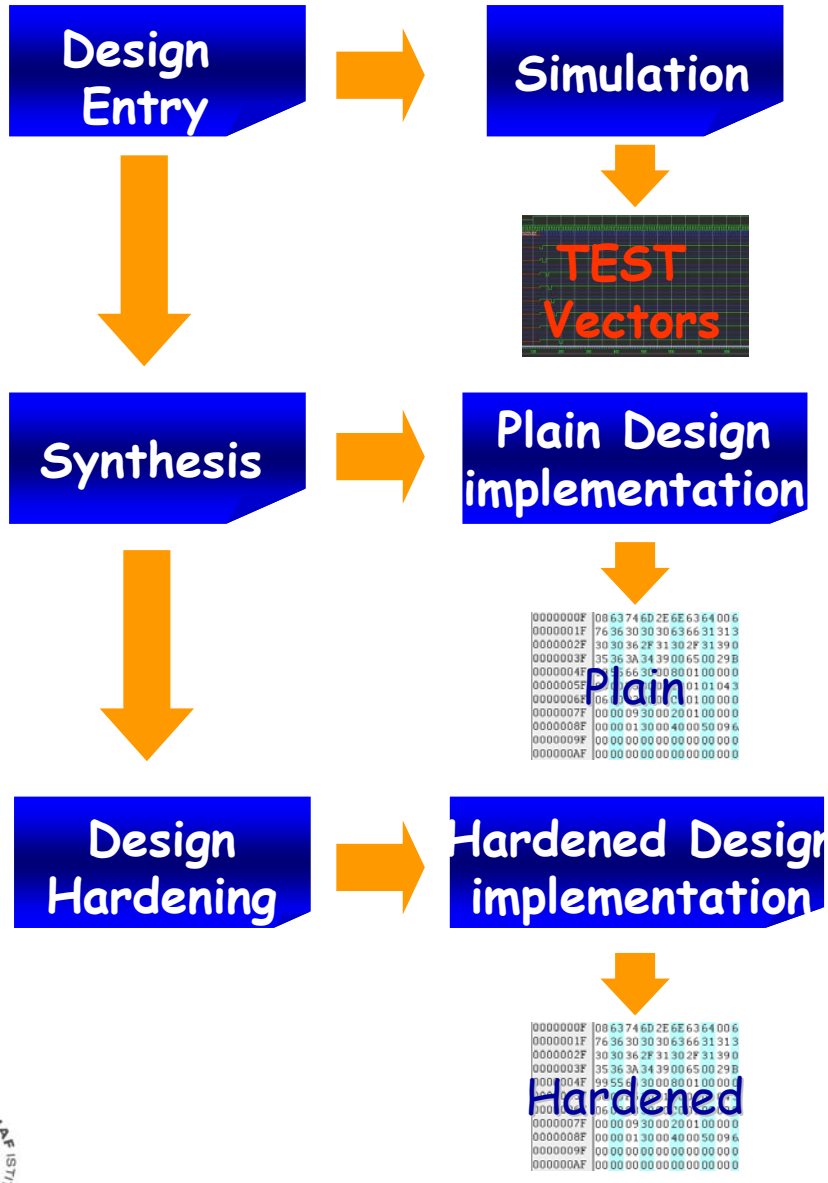
- FLIPPER project started in 2004
- FLIPPER injects bit-flips within the FPGA configuration memory by means of partial re-configuration
- The system consists of a hardware platform and a software application running on a PC
- DUT device is an XQR2V6000 hosted on a piggy-back board
- Test vectors and reference values for the functional test of implemented designs are imported by the software application from an external HDL simulator

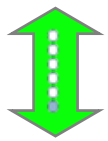


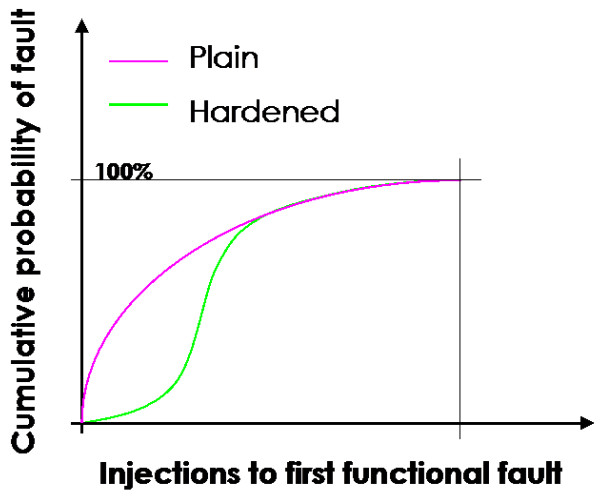
What's FLIPPER for

- Quantitative characterization of design robustness
- Workload dependant analysis of sensitive bits
- Comparison of design hardening techniques
- Tuning of design redundancy and protection
- Optimization of radiation ground testing

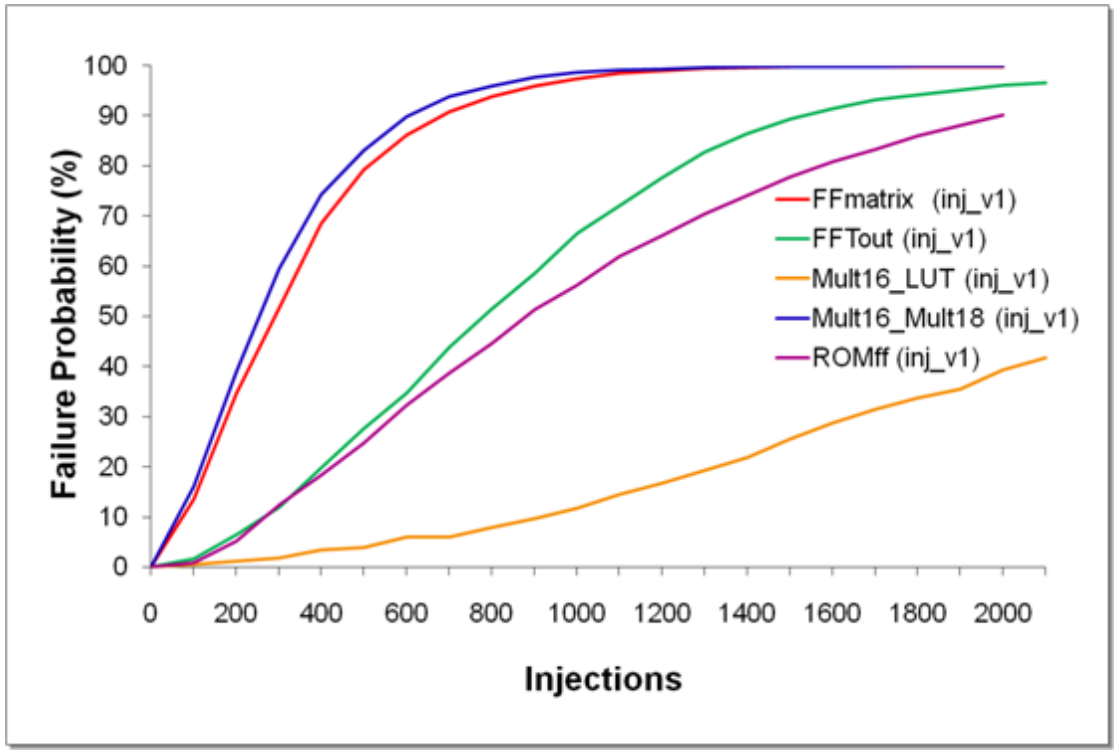
An Example


Design Entry
Simulation
TEST Vectors
Synthesis
Plain Design implementation
Plain
Design Hardening
Hardened Design implementation
Hardened




Plain
Hardened
100%
Cumulative probability of fault
Injections to first functional fault

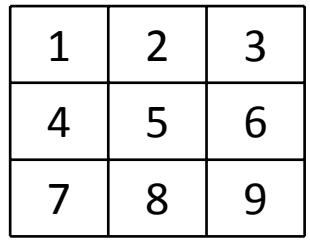
Example: per Module Results

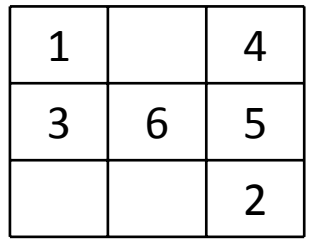


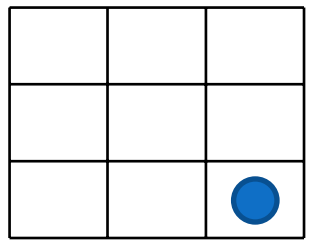
- Max 100k injections per RUN
- 28000 test vector @10 MHz
- Per module analysis
  - MOST sensitive "module" -> Mult16_Mult18
  - LESS sensitive "module" -> Mult16_LUT

What FLIPPER can do

- Identifies design sensitive bits with respect to the applied set of test vectors
  - Systematic
- Mimics the irradiation experiment (bit-flip accumulation)
  - Random
- Evaluates the impact of critical bits for a given workload
  - Specific

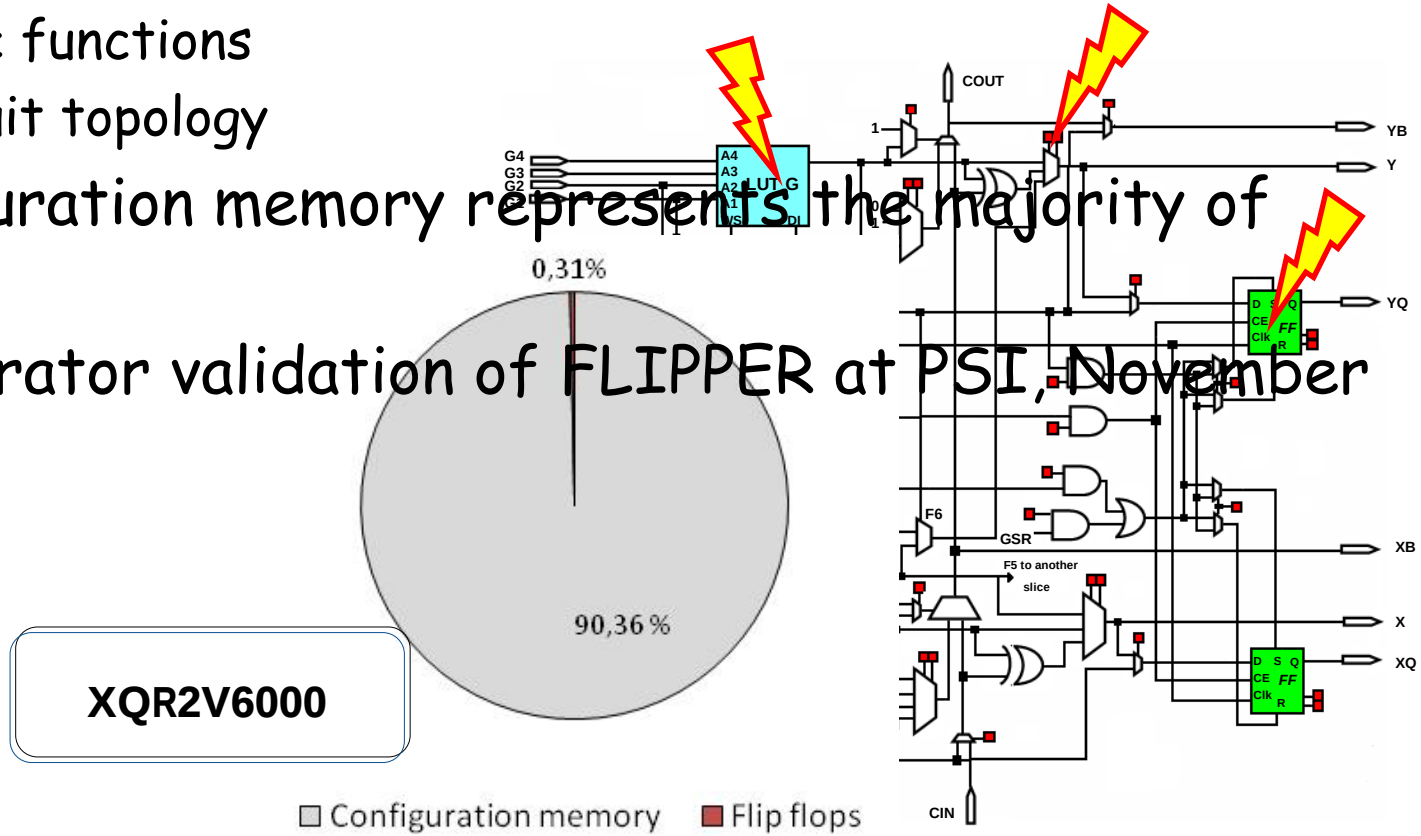






Fault Model

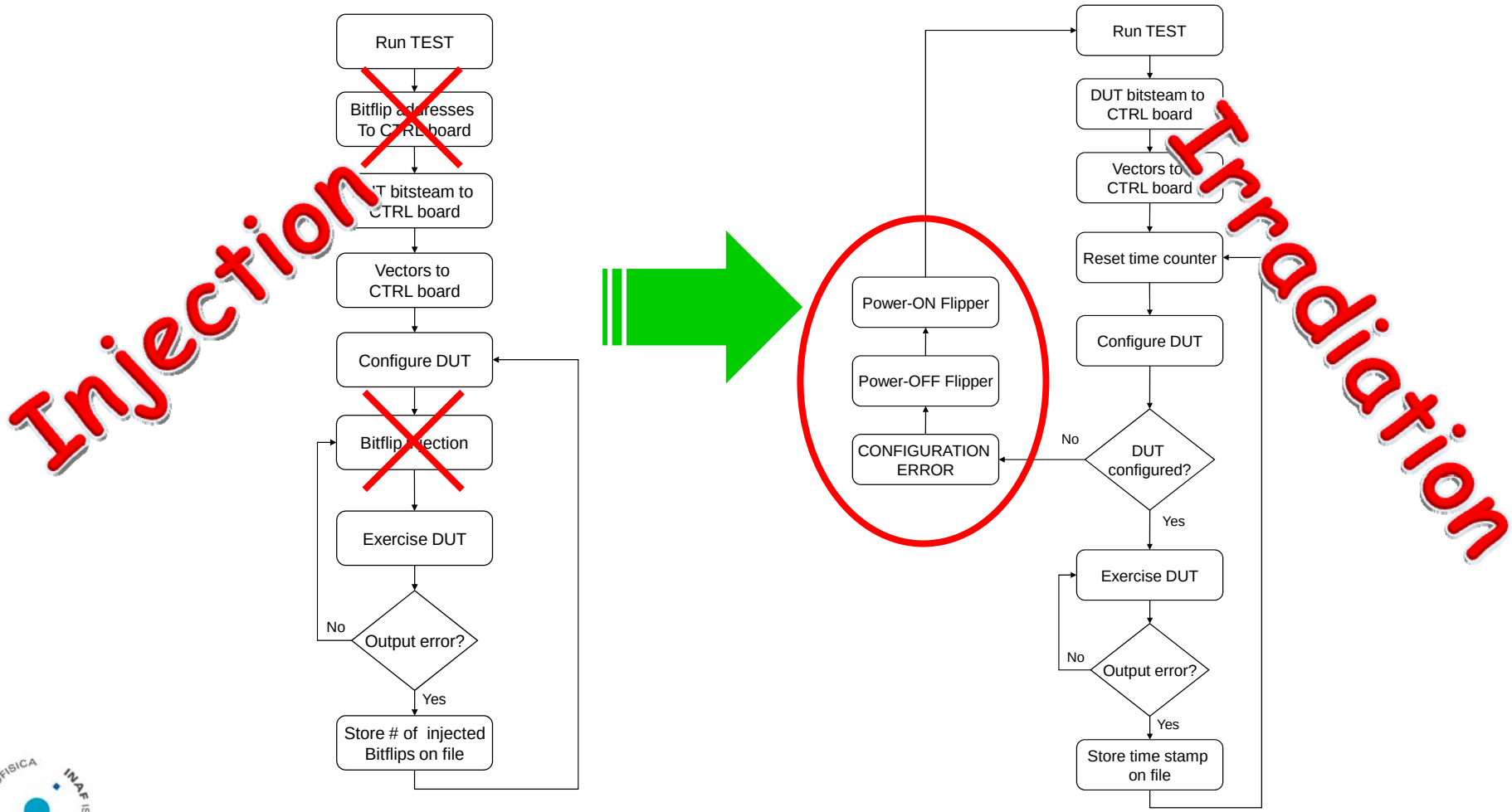
- Bit-flip of configuration memory cells
- Bit-flips in configuration memory may affect
  - Logic functions
  - Circuit topology
- Configuration memory represents the majority of device
- Accelerator validation of FLIPPER at PSI, November 2008



FLIPPER Validation

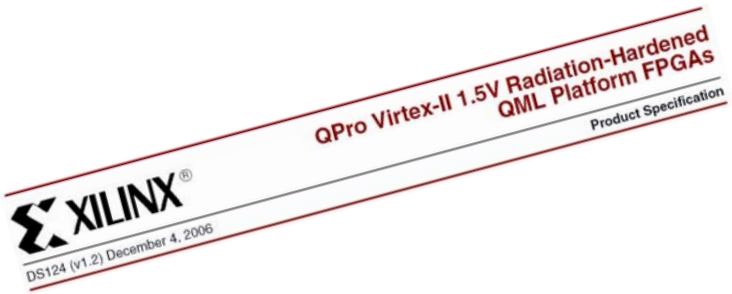
- Beam time@PSI provided by ESA
- A priori fault injection analyses for prediction purposes
- In beam procedures easily derived from the fault injection ones
- Benchmark design with two protection variants (V1, V2)
  - V1 is derived from the unprotected design by straightly applying XTMR
  - In V2 a dummy feedback path, controlled by a multiplexer, is inserted for each flip-flop (the XTMR is forced to instantiate a voter for every flip-flop in the design)

Procedures


Injection
Run TEST
Bitflip addresses To CTRL board
DUT bitsteam to CTRL board
Vectors to CTRL board
Configure DUT
Bitflip injection
Exercise DUT
Output error?
No
Yes
Store # of injected Bitflips on file
Irradiation
Run TEST
DUT bitsteam to CTRL board
Vectors to CTRL board
Reset time counter
Configure DUT
DUT configured?
No
Yes
Exercise DUT
Output error?
No
Yes
Store time stamp on file
CONFIGURATION ERROR
Power-OFF Flipper
Power-ON Flipper

Irradiation Experiment

DUT Device: XQR2V6000



- 180 MeV proton beam (nominal)
- average flux : ~ $6.28 \cdot 10^{7}$ cm^{-2} s^{-1}
  - 1 CBU at most during test vector application
  - CBU_{rate}: ~ 82 s^{-1}
- stimuli: ~ 28,000 vectors@10 MHz
- total exposure time: ~ 8 hours
- Fluence: ~ $2.19 \cdot 10^{12}$ p/cm^{-2}
- TID: < 140 krad
- ~ 600 samples for V2, ~ 400 samples for V1

Radiation Specifications(1)

Table 3: **Minimum Radiation Tolerances**

Symbol	Description	Min	Max	Units
TID	Total Ionizing Dose Method 1019.5, Dose Rate ~50.0 rad(Si)/sec	200	-	krad(Si)
SEL	Single Event Latch-up Immunity Heavy Ion Linear Energy Transfer (LET)	160	-	(MeV-cm²/mg)
SEFI	Single Event Functional Interrupt GEO 36,000km Typical Day		1.5E-6	Upsets/Device/Day

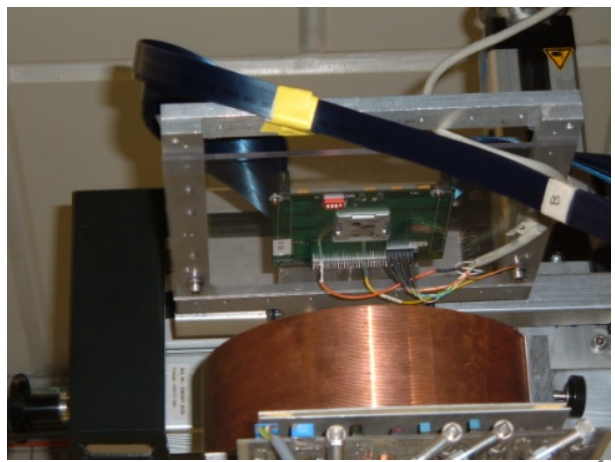
XQR2V6000 : device specification

Device static proton cross section (per bit)

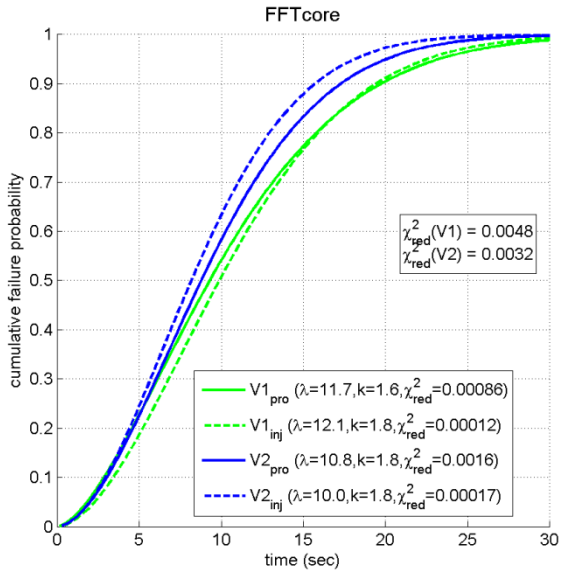
$3 \cdot 10^{-14}$ cm^2 @198 MeV

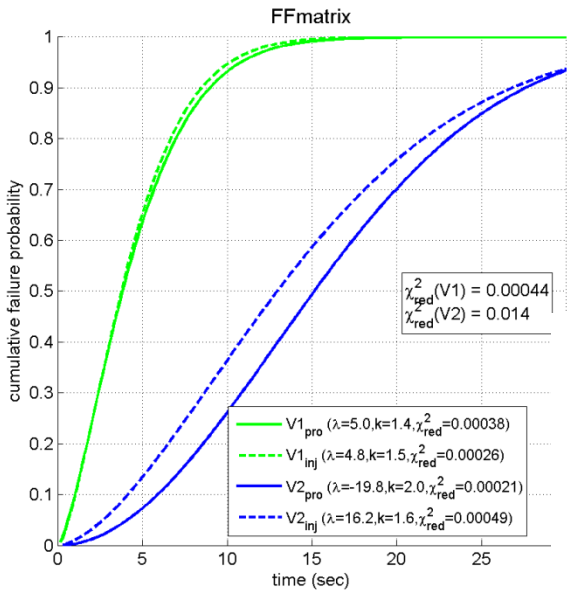
# of configuration cells

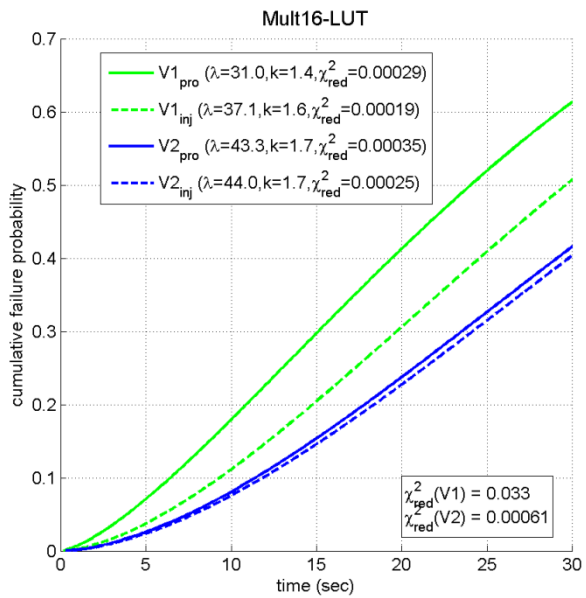
19.742.976



Results







——— Proton data

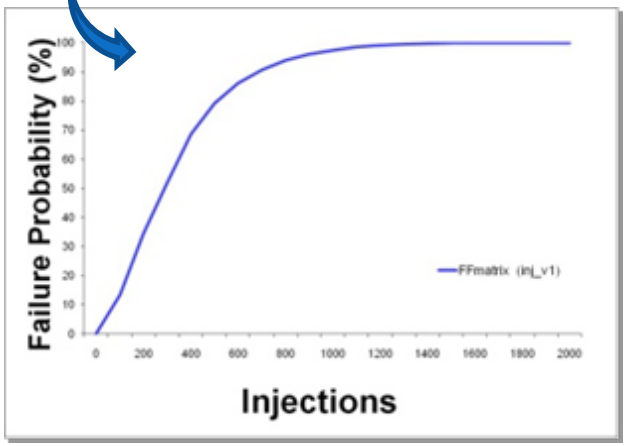
- - - - Injection data

V1 variant

V2 variant

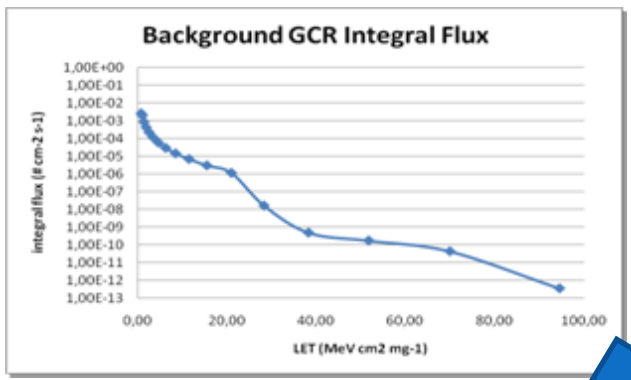
Design failure prediction

Design Level

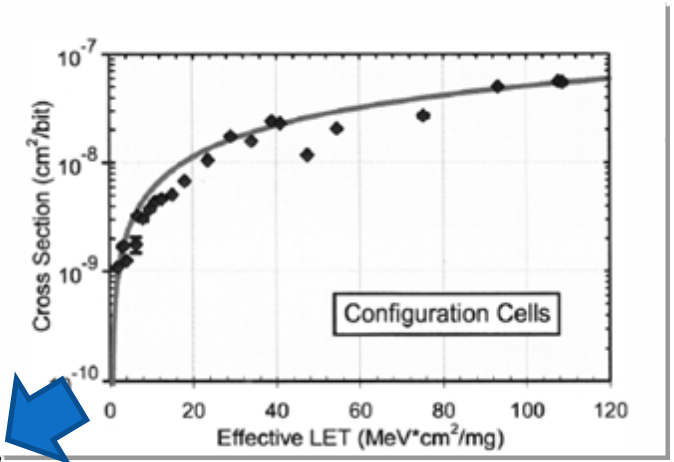


$$t \propto \frac{1}{CBU_{rate}} \cdot n_{inj}$$

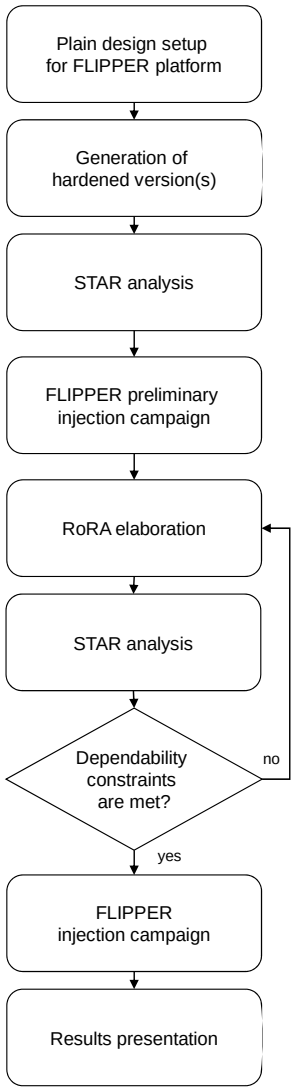
Device Level



CBU_{rate}



FLIPPER-STAR-RoRA Integrated Flow



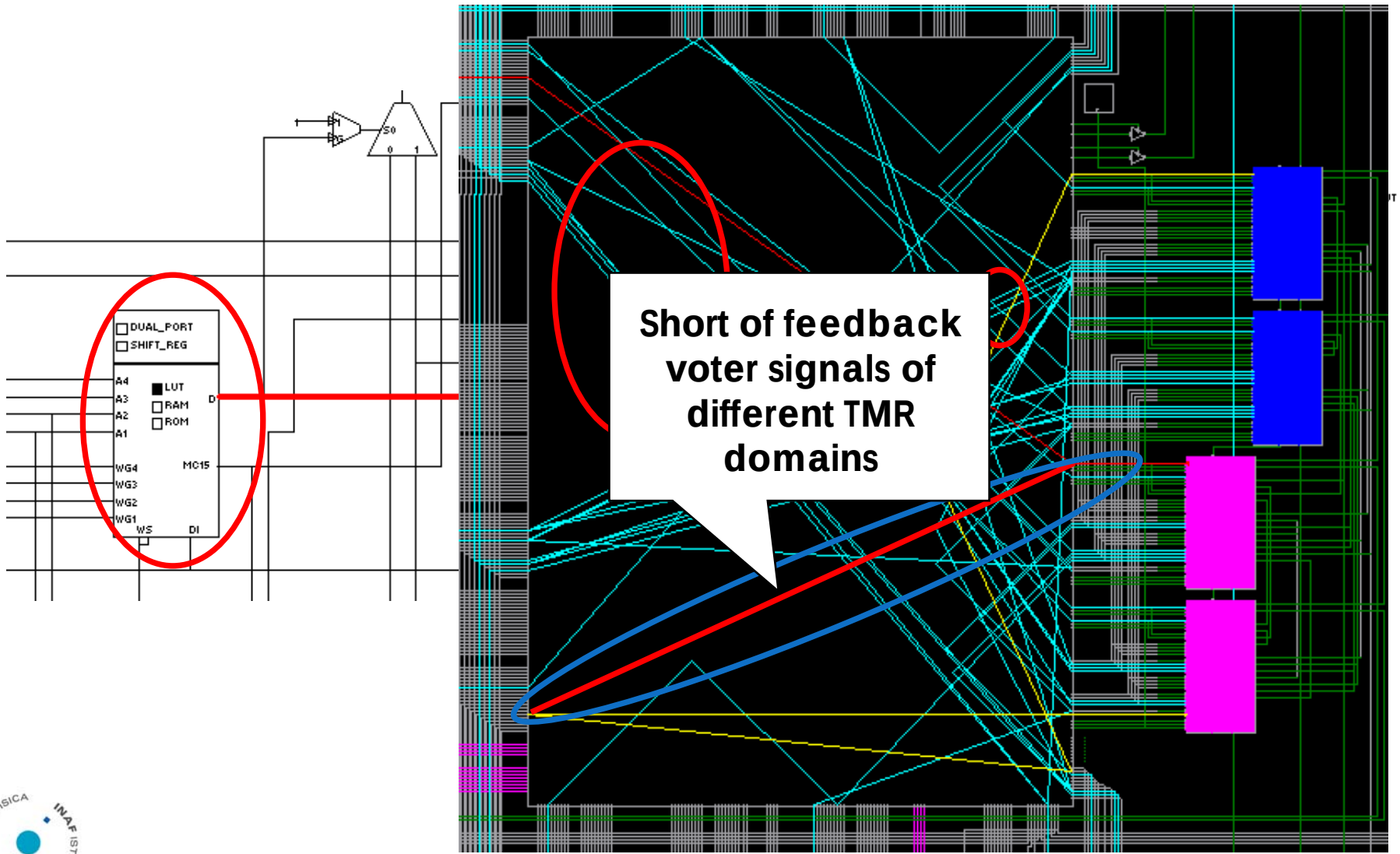
- Plain design setup for FLIPPER platform
- Generation of hardened version(s), for example by XTMR
- Static analysis of common mode failures by means of STAR
- FLIPPER preliminary injection
- Criticalities fix by RoRA:
  - Smart placement to remove CLB-related common mode failures
  - Smart routing to remove PIP-related common mode failures.
- FLIPPER injection campaign
- Injection result presentation

FLIPPER-STAR: An Example

- STAR identifies a list of critical bits
- FLIPPER ad-hoc injection: evaluates the impact of critical bits for a given workload
  - selected bits in the configuration memory are injected
  - the altered bit is restored before the successive injection is performed
- Design
  - Simple 8 bit counter protected by XTMR

X-TMR Circuit	CLB [#]	IOBs [#]	Slices [#]	LUTs [#]	FFs [#]
COUNT8	33	90	130	144	120

Results - COUNT8



Future Works

- Virtex 4 DUT
- New hardware platform
  - Ethernet link
  - DDR2 onboard memory
- Software upgrade

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