Mitigation of SCU and MCU effects in SRAM-based FPGAs: placement and routing solutions

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Goal

To provide solutions for increasing the fault-tolerance capabilities with algorithms able to reduce sensitive configuration memory bits of SRAM-based FPGAs.

Summary

- Introduction
- Cell Upsets in FPGA's configuration memory
- (X)-TMR hardening techniques limitations
- Hardening circuits against SCU/SEU
  - RoRA and V-Place tool
- Hardening circuits against MCU/MBU
  - Layout-based placement
  - V-Place v.2 tool
- Roadmap
- Conclusions

Introduction

- SRAM-based FPGAs are drastically sensinsitive to radiation particles
- Rad-Hard devices are available
  - Increases the designing cost
  - SEL immune but not immune to bit-flip effects
- TMR techniques must be applied to protect errors due to single configuration memory bit-flip
- Prevent accumulation (scrubbing techniques)
- Our solutions remove errors that corrupt TMR increasing the fault tolerance capability of circuits mapped on SRAM-based FPGAs.

Cell Upsets in FPGA's configuration memory

- Single Cell Upsets (SCUs) modify the configuration of routing or logic resources
  - Logic

    LUT, Configuration, MUXes… status modification
  - Routing

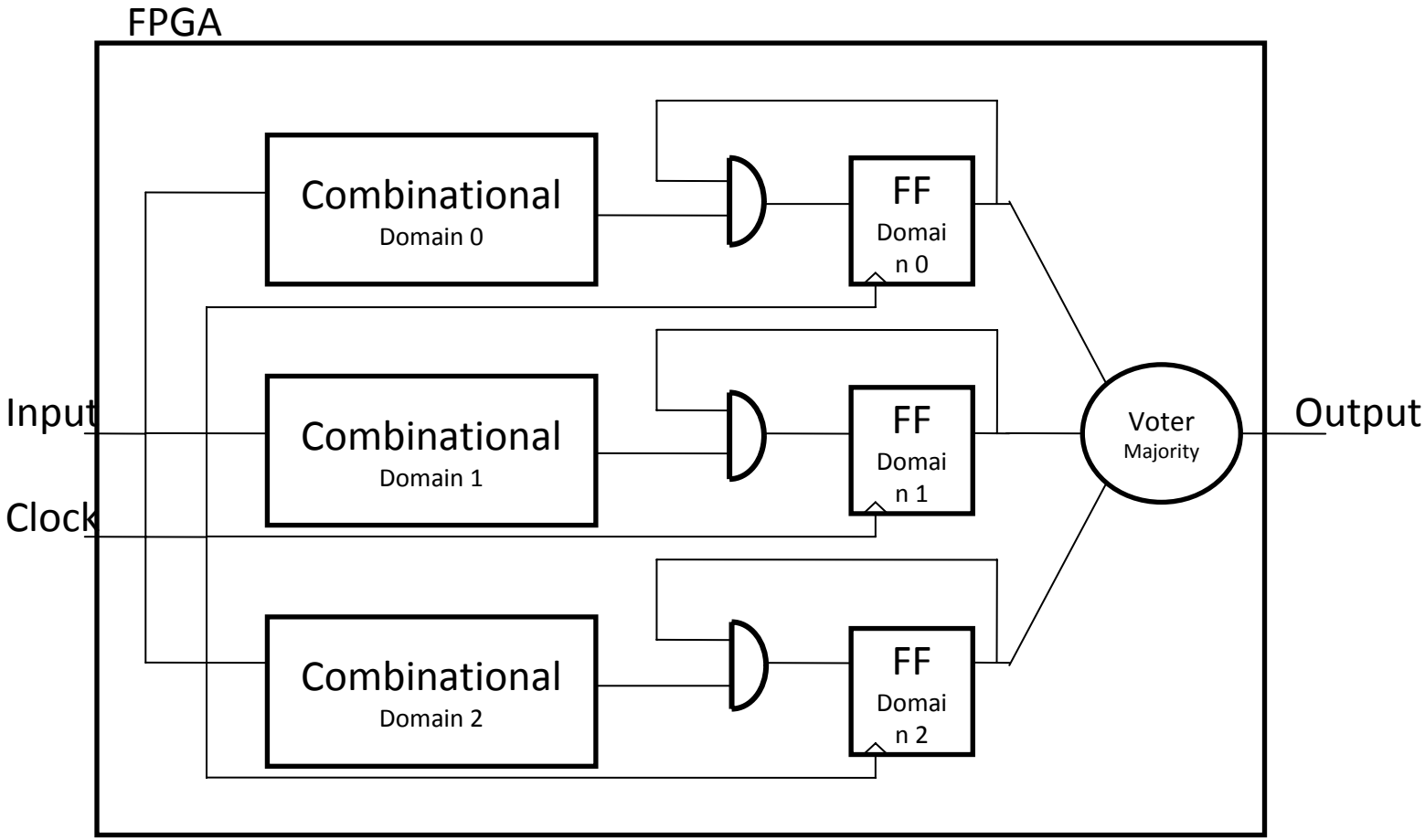
    PIPs are opened/shortened together
- Multiple Cell Upsets (MCUs) modify the configuration of routing and logic resources
  - The scenario changes on the basis of:

    Orientation: single column, row or diagonal

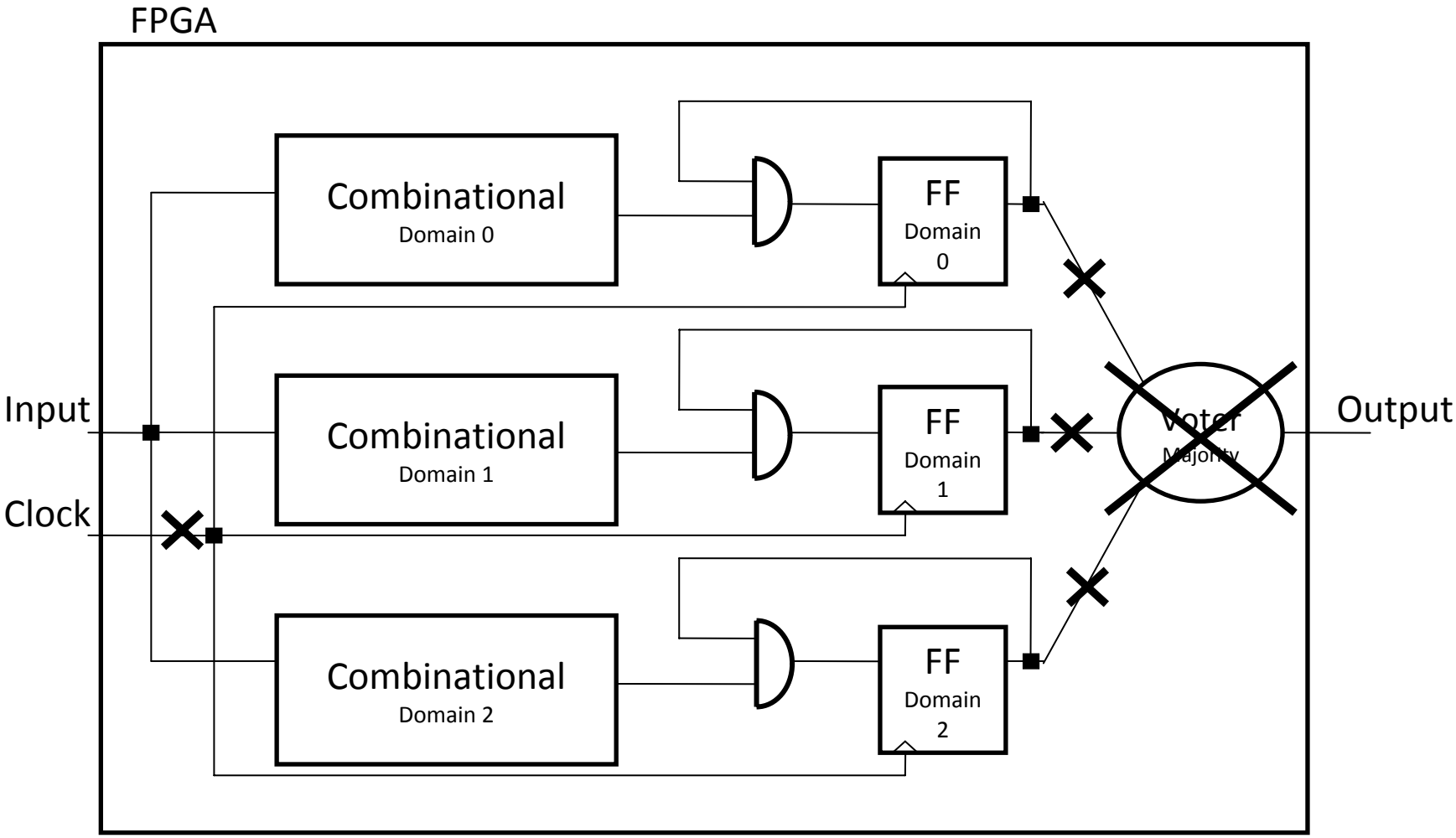
    Case: 2 or more cells, 00->11, 01->10, …

    Effects: Short, Open, Routing, Logic or Routing/Logic

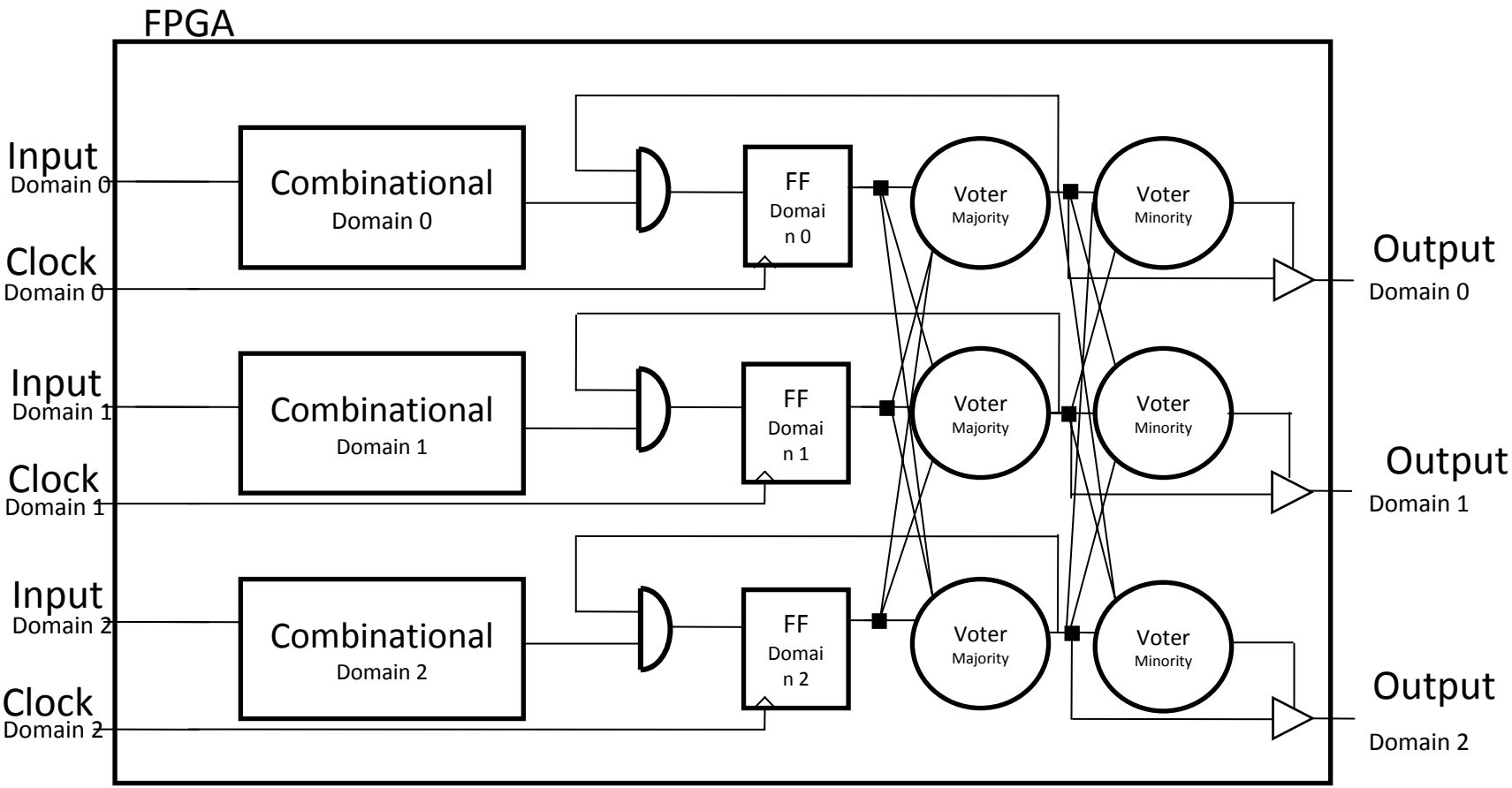
Standard TMR



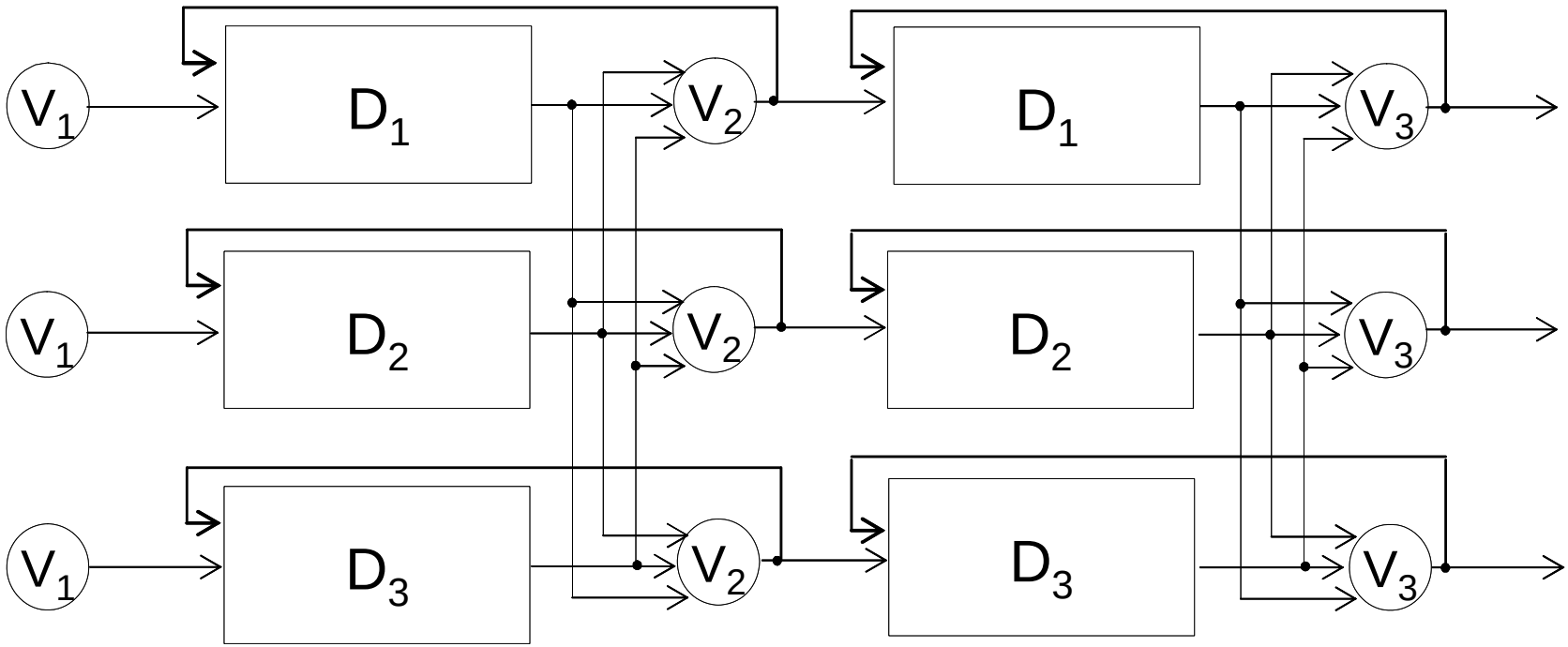
Standard TMR



X-TMR


FPGA
Input
Domain 0
Clock
Domain 0
Input
Domain 1
Clock
Domain 1
Input
Domain 2
Clock
Domain 2
Combinational
Domain 0
Combinational
Domain 1
Combinational
Domain 2
FF
Domai
n 0
FF
Domai
n 1
FF
Domai
n 2
Voter
Majority
Voter
Majority
Voter
Majority
Voter
Minority
Voter
Minority
Voter
Minority
Output
Domain 0
Output
Domain 1
Output
Domain 2

X-TMR and Voter Partitions



Voter Partition 1

Voter Partition 2

X-TMR hardening techniques limitations

1. Redundancy based hardening techniques are applied at the pre-synthesis or synthesis level

   FPGA's layout information are not considered

SCUs/MCUs affecting different logic domains within the same voter partition corrupt the TMR protection

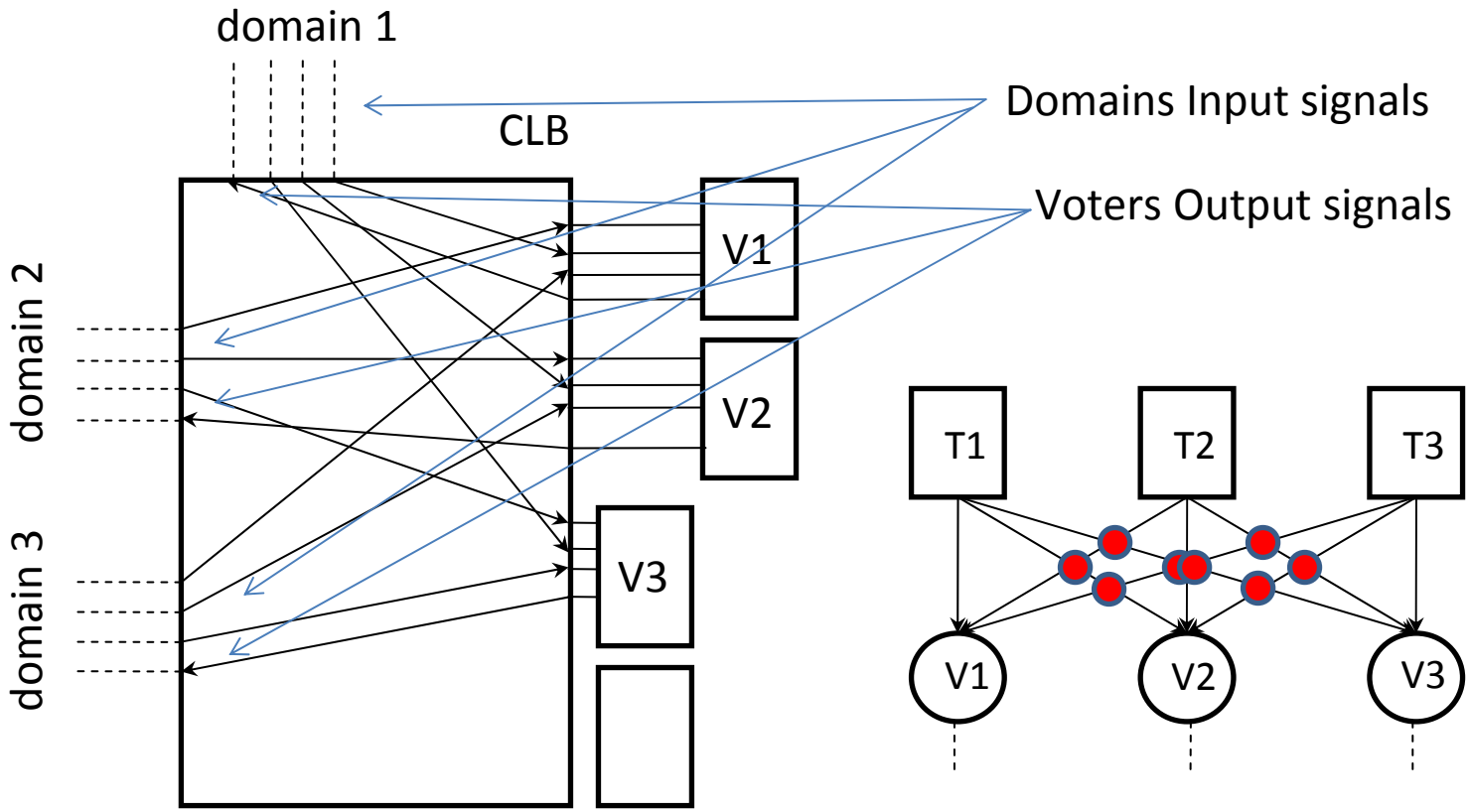
2. Voter partitions decrease intrinsically the TMR robustness

   Voter structure creates at least 9 crossing points between nets of different TMR domains

Commercial mapping and place/route tools implement voter's structure using nearby LUTs

Voter interconnections converge into a single switch-matrix.

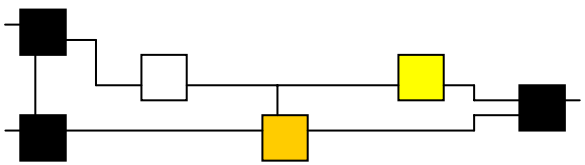
X-TMR hardening techniques limitations



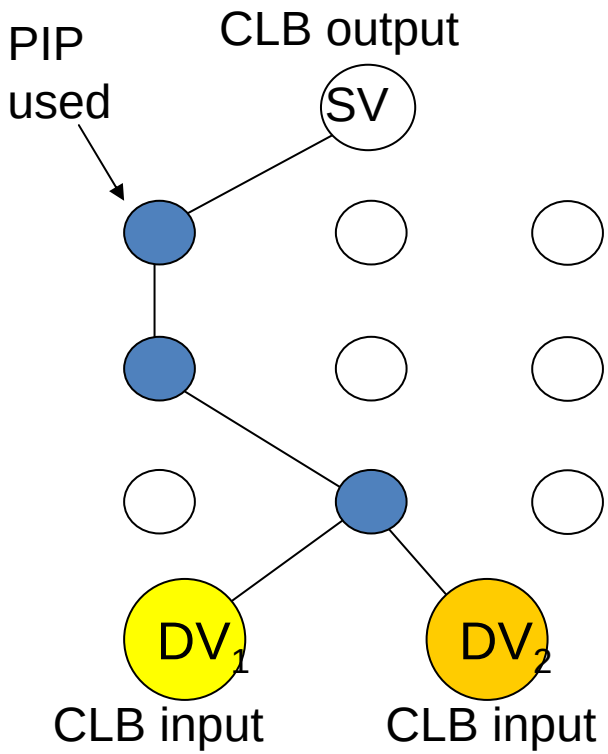
Hardening circuits against SCU

- Reliability-oriented Routing Algorithm - RoRA

```
/*Placement*/
generate_partitions (S1, S2, S3, S4)
generate_circuit_replicas (F1, F2, F3)
generate_majority_voter (Voter)
for each logic block LB ∈ Fi
 place LB on  Si  where i = {1, 2, 3}
place majority Voter on S4
/*Routing*/
FVS = ∅
for each source vertex SV ∈ Fi
{
      for each destination vertex DV ∈ SV
    create_routing_tree (SV, DV)
   update (FVS)
}
```



Circuit replica placed in Si



- **Create the connections between the Control Logic Blocks**

Hardening circuits against SCU

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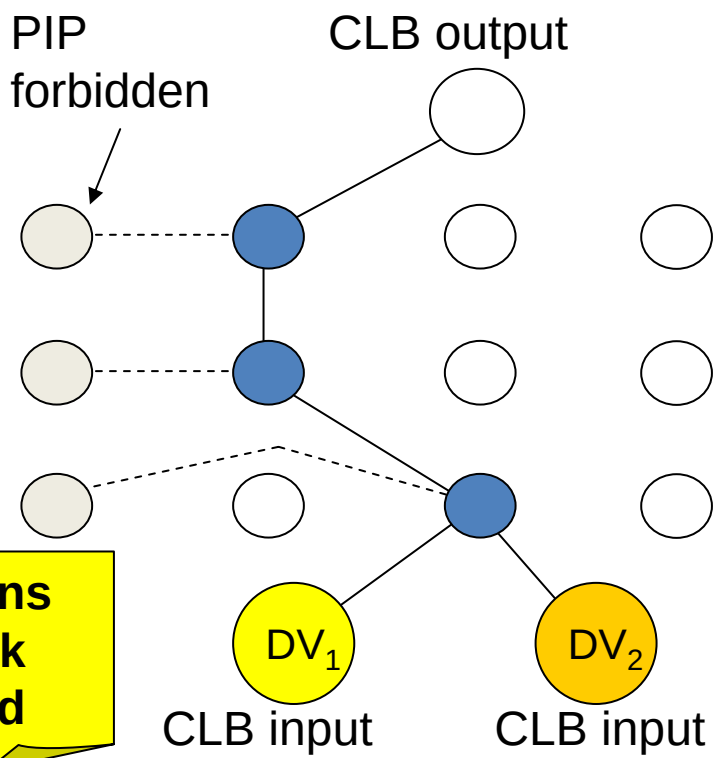


- **While routing is performed, solutions that could allow a single fault to link different circuit replicas are avoided**

Hardening circuits against SCU

- Reliability-oriented Routing Algorithm – RoRA

1. reads the a X-TMR or TMR description
2. suitably performs place and route (according to predefined rules that guarantee robustness against fault effects)

– Placement constraints
  – compatible with the Virtex-II and Virtex-IV
  – oriented to the internal voter structure
– Routing algorithm solves singular criticalities

Hardening circuits against SCU

- Some results about RoRA

Circuit	Device	Critical SEUs	
		X-TMR Circuit	RoRA Circuit
B01	XC2V40	6	0
B02	XC2V40	3	0
B03	XC2V40	16	0
B04	XC2V40	418	0
B05	XC2V80	432	0
B06	XC2V40	7	0
B07	XC2V40	186	0
B08	XC2V40	14	0
B09	XC2V40	13	0
B10	XC2V40	49	3
B11	XC2V40	2	0
B12	XC2V250	57	6
B13	XC2V40	1	0
B14	XC2V1500	54	0

Hardening circuits against SCU

- Versatile Placement algorithm – V-Place
  - To solve the problem of performance degradation while implementing fault tolerant circuits

FPGA and TMR considerations...

- Voter schemes congest routing interconnection
- Severe impact on real-design delay
  - 1.5 and 2.5 times the original not TMRed circuit

- Available solutions forces user's constraints
  - Data path analysis during place and route
  - Phase-shifting persist and timing problem can result

  - Data-path delay introduced by the voting scheme
  - Fully period constant for each voter path not applicable
  - Impossible to cover all the possible feedback signal cross-domains.

Hardening circuits against SCU

The V-Place algorithm is able to:

- Find a valid placement for each logic block
- Use the minimal number of routing segments

It implements two heuristics:

- Min-cut optimization techniques
- Quadratic placement.

Hardening circuits against SCU

- Some results about V-Place

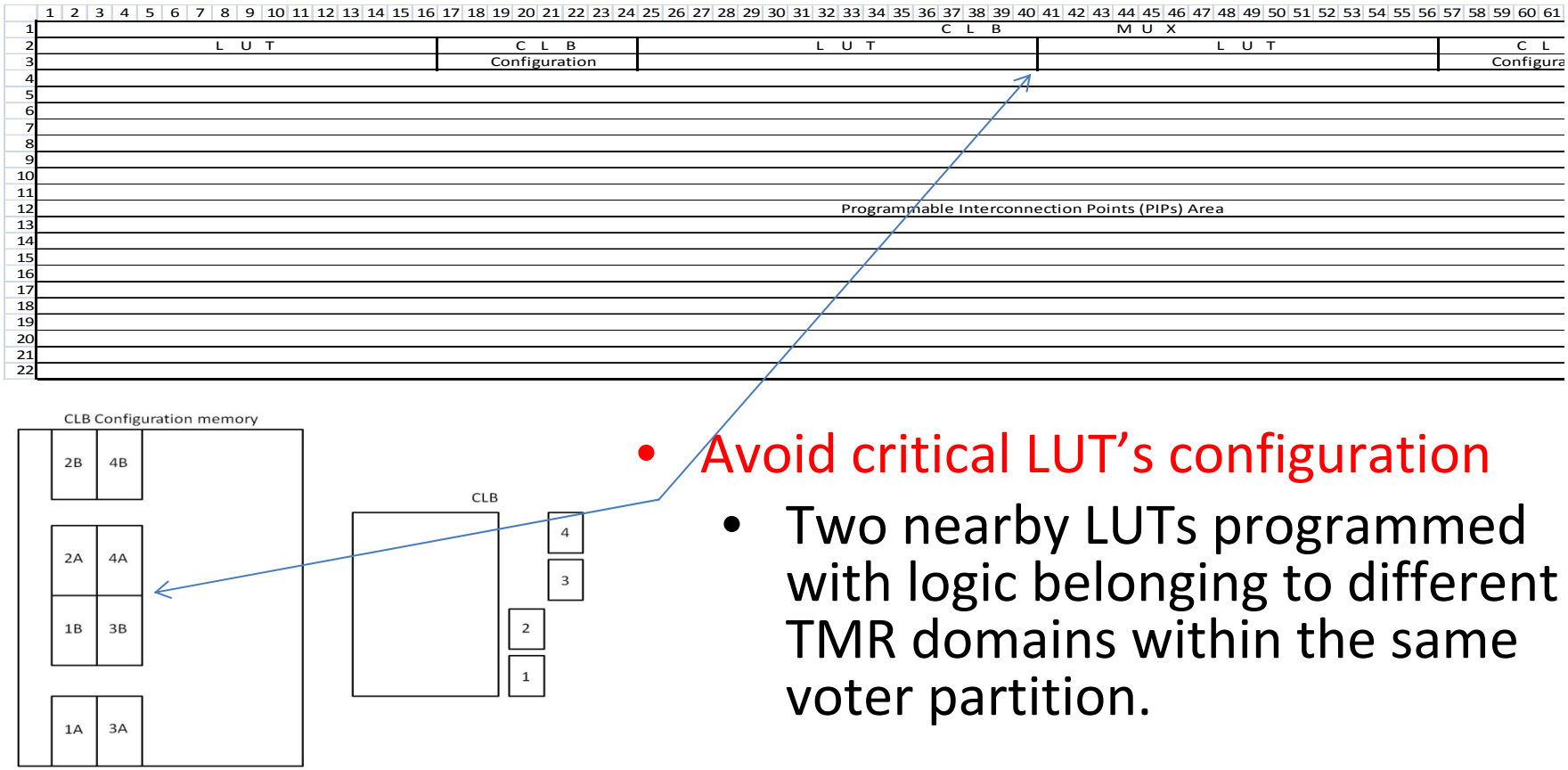
Circuit	Critical Path Delay [ns]		
	Original	TMR	V-Place
B01	1.24	1.71	1.26
B02	0.85	1.35	0.91
B03	2.01	3.26	2.08
B04	2.13	2.22	1.99
B05	2.50	3.24	2.62
B06	0.96	1.98	1.04
B07	2.10	2.15	2.10
B08	1.14	1.52	1.24
B09	1.90	1.94	1.91
B10	1.71	2.11	1.83
B11	2.24	4.67	2.54
B12	2.11	4.56	2.46
B13	0.83	1.76	0.91
B14	2.18	5.03	2.20

Hardening circuits against MCU

- Placement Hardening Algorithm for Multiple Cell Upsets
- Analytical-model based on a graph
- Physical layout information
- Three metrics
  - LUTs
  - Voters
  - CLB clusters

Hardening circuits against MCU

- LUT metric

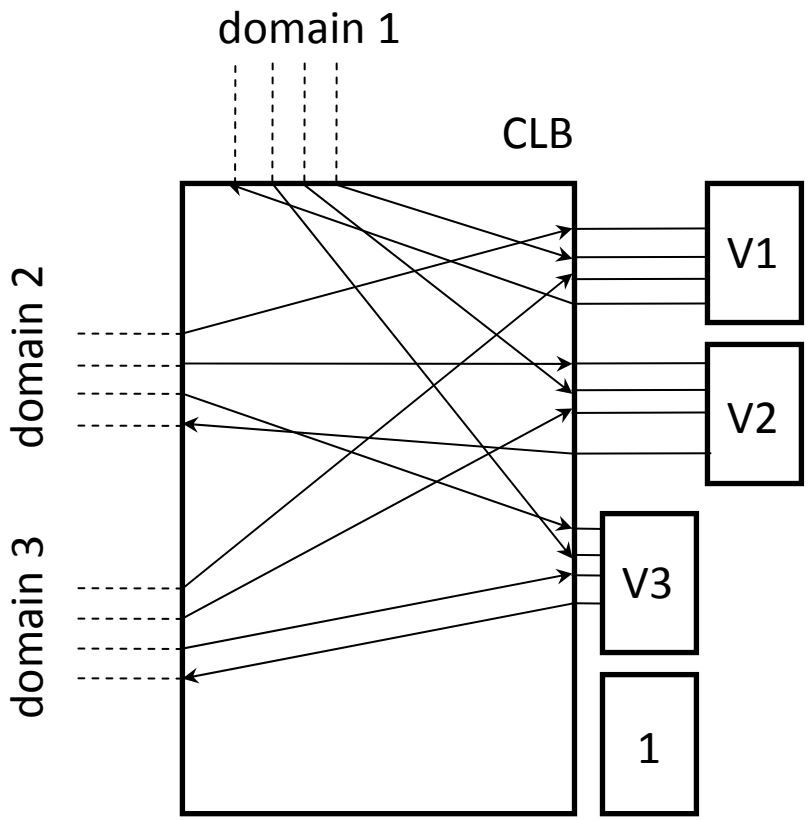


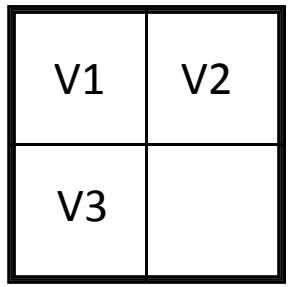
- Avoid critical LUT's configuration
  - Two nearby LUTs programmed with logic belonging to different TMR domains within the same voter partition.

Hardening circuits against MCU

- Voter metric

To delocate the voter positions in different CLBs



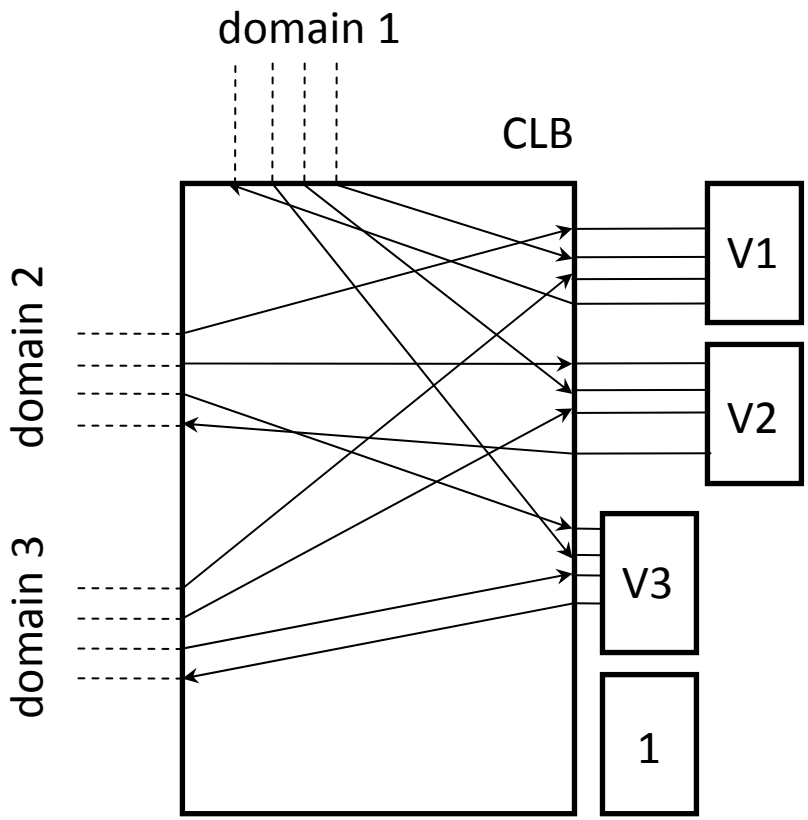


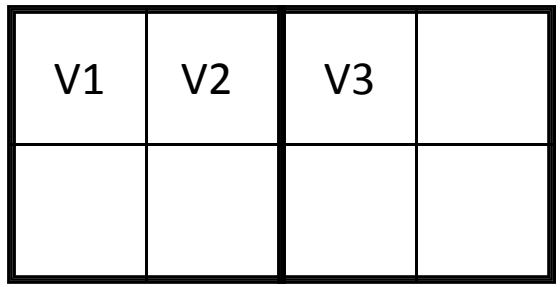
Routing density (9+3) / 1 = 12

Hardening circuits against MCU

- Voter metric

To delocate the voter positions in different CLBs



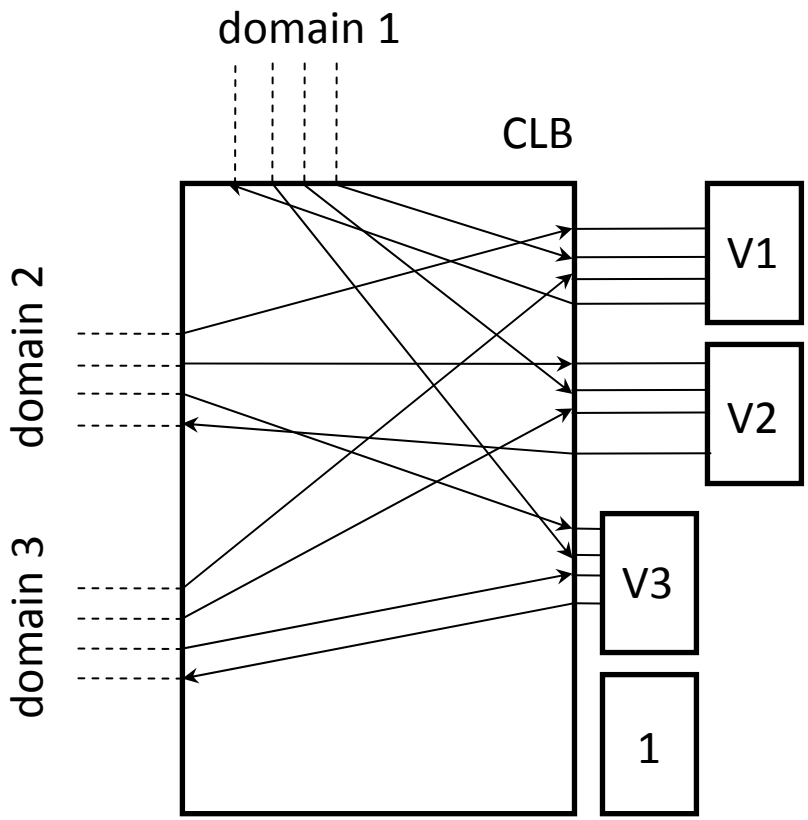


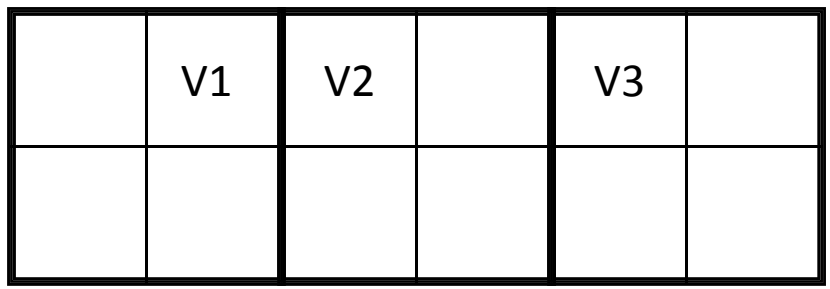
Routing density (9+3) / 2 = 6

Hardening circuits against MCU

- Voter metric

To delocate the voter positions in different CLBs



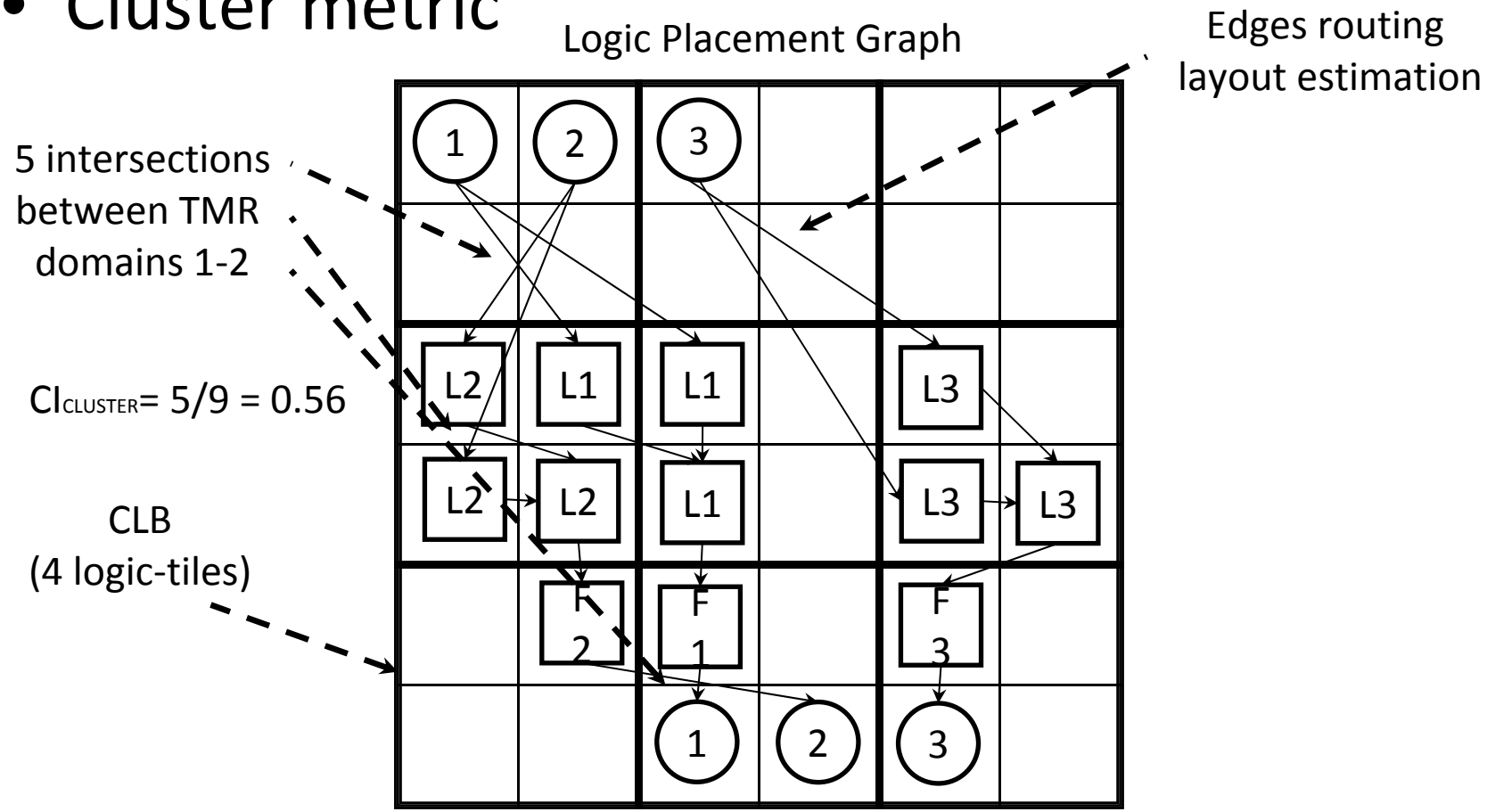


Routing density (9+3) / 3 = 4

The voter routing density is reduced

Hardening circuits against MCU

- Cluster metric



Hardening circuits against MCU

- Some results

Circuit	# Critical MCUs – 2-cells	
	TMR circuit	V-Place v.3 circuit
b01	18	0
b02	13	0
b03	69	1
b04	1,139	10
b05	1,359	12
b06	23	1
b07	635	8
b08	39	2
b09	45	1
b10	164	5
CORDIC	684	9

Roadmap


2004
STAR v0/RoRA v0
Xilinx Spartan II
2006
STAR v1/RoRA v1
Xilinx Virtex II
Full XTMR support
2007
STAR v2/RoRA v2
Faster analysis engine
2008
STAR v3/RoRA v3/VPLACE v1
SCU Virtex 4
Susanna v1
AT40K
2009
STAR v3.1/RoRA v3.1/VPLACE v2
Xilinx MCU
Susanna v2
ATF280E
2010
STAR v3.2/RoRA v3.2/VPLACE v3
Xilinx MCU Virtex 4
Susanna v2.1
Improved report
Atmel, France
Boeing Satellite Systems, USA
EADS IW, France
European Space Agency, NL

Conclusions

- Place and Route solutions are developed for hardening circuits against SCUs / MCUs
- Support available for Xilinx Virtex I-II/4 devices

For further information…

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