ATMEL ATF280E
Rad Hard SRAM Based FPGA

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Overview

- Atmel FPGA Key Points and Architecture
- ATF280E Radiation Test Results
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ATF280E Block-Diagram

- **User I/O**
- **Boundary Scan Controller**
- **LVDS Interface**: 8 Rx / 8 Tx
- **FPGA Core**: 120 x 120 core-cells, 30 x 30 FreeRAMs
- **Config. SRAM**
- **Config. Control**
- **Configuration Self Integrity Checker**
- **Configuration Load Checker**
- **Differential Clocks**: 8 Global / 4 Fast
- **POR**
Atmel Radiation hardened FPGAs

- Layout rules
  - Improved to avoid multiple nodes charge collection during a single heavy ion impact

- SEU hardened Memory points
  - Core cell Flip-Flops, embedded memory, configuration memory based on radiation hardened Flip-Flops

- Controller protected by classical TMR
  - Including combinatorial logic and flip-flop of all states machines

- Clock and reset trees
  - Protected by DMR (resistive isolation path based on N and P isolated path carrying the same signal)

- Your Design is radiation hardened by construction
  - No need for SEU/SET mitigation
Hardened Memory Cell and Isolation Path

NAND

SET « high » only
To P transistors gates of next logic

SET « low » only
To N transistors gates of next logic
ATF280E Key Features

- 288K equivalent ASIC gates
- 50 MHz clock speed
- 14400 core-cells (each 2 LUT + 1 DFF)
- 115 Kbit FreeRAM (900 modules of 32x4 blocks)
- 1.8V Core / 1.8V and 3.3V Cold-sparing I/Os
- Dedicated 1.8V LVDS buffers: 8 pairs Rx + 8 pairs Tx
- 3.3V PCI-compliant I/Os

- ATC18KRHA 0.18um CMOS technology (same as ATC18RHA ASIC and AT697F LEON2 processor)
- MCGA472 (308 + 32 User I/O) / MQFP256 (148 + 32 User I/O)

- Configuration load integrity check
- Configuration self-integrity check
- Boundary scan interface
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- Application oriented SEU sensitiveness
ATC18RHA Radiation Performances

- ATF280 and AT697F (100MHz Leon2FT) use the same ASIC technology
  - ATC18RHA, 0.18µm technology
  - TID tested up to 300 Krad without parameters drift
  - No SEL up to 70 MeV.cm²/mg@125°C
  - SEU:
    - ATC18RHA SEU hardened DFF: LET threshold of 30 MeV/mg/cm2)
    - sensitivity of the standard DFF to SEU (LET threshold of 2 MeV/mg/cm2).

- Silicon size increase by 30% to ensure RHBD
  - To be compared to 3 to 4.5 for non RHBD
Test Principles

- **Functionality and Immunity Test configurations**
  - Reset: configuration memory reset to low level (‘0’).
  - Multiplier: configuration memory set to high level (‘1’).
  - Shift register: core cell flip-flops and clock tree to upset.
  - Inverted shift register: core cell flip-flops and clock tree to upset as the combinatorial path to transients.
  - And chain: combinatorial path to transients.
  - Free RAM: integrated FreeRAM block tested as 4K words of 16 Bits dual-port RAM.
  - Free RAM with EDAC: integrated FreeRAM block tested as 4K words of 16 Bits dual-port RAM with an “Error Detector and Correction” EDAC system.

- **Test conditions**
  - Configuration clock frequency 1MHz
  - IOs supply in the range 3V to 3.6V, nominal 3.3V
  - Core voltage in the range 1.65V to 1.95V, nominal 1.8V
  - Package temperature control for Latch-Up sensitivity

- **Test operator and location**
  - Test is run by HIREX (France)
  - Test locations:
    - UCL Louvain, Belgium
    - BNL Berkeley, USA
    - RADEF Jyvaskyla, Finland
Test Results

- Single Event Latch-up
  - No SEL detected over all the runs performed and in particular with the runs performed at 1.95V core voltage and 3.6V I/O buffer at LBNL with Xenon and 45 deg tilting angle that corresponds to a LET of 76 MeV/(mg/cm²) and a device under test (DUT) temperature of 125°C, up to fluence of 1.10+7 part/cm².

- Cross section
  - The configuration SEU error cross section per device versus effective LET is derived from the tests performed in UCL, LBNL and RADEF.
    - Configuration memory SEU saturated cross-section better than 5.10-3 per device (3.10-9 cm² per bit) with a LET threshold around 30MeV at Vcc min.
    - No SET was recorded with a LET of 43 MeV/(mg/cm²).
    - SET error cross-section per device about 1.6 10-4 at 60MeV/(mg/cm²).
    - FreeRAM Asymptotic SEU error cross-section per bit about 6.5 10-8 cm².
SEU sensitivity of ATF280E configuration bits

![Graph showing SEU sensitivity for different configurations of ATF280E.]
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Conclusion

- **RHBD FPGA**
  - ATF280
    - samples already available and designs on going
    - Improvement of power-on current (maximum in worst case conditions 1A during 10μs)
    - Application note on-going on How to design board for proven start-up current

- **Multiple die package AT697F + ATF280**
  - High performance AT697F (Leon2 FT SPARC V8 100MHz)
  - Peripherals in FPGA
  - One version under development under CNES contract (SPARC slave, memories controlled by FPGA)
  - One version with SPARC master to be developed

- **ATFS450 development on going using 130nm SOI process**
- **New architecture for 2.5Mgates RHBD SRAM based FPGA for 2012, 65nm process**