New capabilities for fault tolerance in FPGA synthesis

ESA Radiation Effects Workshop

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Evolution of PLD/SEE parameters

- Anti-fuse devices evolved
  - Increased capacity & operating frequency
  - Increased SET occurrence
- Adoption of SRAM-based devices
  - Further increases to capacity & operating frequency
  - Typically less hardened, needs scrub
- New mitigation approach needed for SRAM- and antifuse-based devices

<table>
<thead>
<tr>
<th>Process Geometry</th>
<th>1999</th>
<th>2009</th>
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</thead>
<tbody>
<tr>
<td>Device Capacity</td>
<td>~20k gates</td>
<td>~20M gates</td>
</tr>
<tr>
<td>Operating Frequency</td>
<td>~20MHz</td>
<td>~150MHz</td>
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<tr>
<td>Relevant SEE</td>
<td>SEU</td>
<td>SEU &amp; SET</td>
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Precision RTL Plus Overview

- **Start Right**
  - Vendor Independence
  - Standard language support

- **Synthesize & Optimize**
  - Out-of-the-box Quality of Results
  - Physically aware synthesis
  - ASIC Prototyping Support

- **Achieve Design Closure**
  - Award-winning analysis & debug
  - Incremental flows
What Synthesis Provides Today

*Capabilities for fault tolerance*

<table>
<thead>
<tr>
<th>Feature</th>
<th>User Benefit, Problem Solved</th>
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<tbody>
<tr>
<td>Safe FSM</td>
<td>Protection against getting stuck in invalid state caused by Single Event Upset (SEU)</td>
</tr>
<tr>
<td>TMR support (Local)</td>
<td>SEU mitigation for Actel anti-fuse Families</td>
</tr>
<tr>
<td>Message customization &amp; reporting</td>
<td>- Easy to find relevant messages</td>
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<td></td>
<td>- Messaging policies</td>
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<tr>
<td>Repeatability</td>
<td>Provides deterministic netlist for configuration sign-off</td>
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<tr>
<td>FormalPro Integration</td>
<td>Automated setup and launch of formal equivalence check</td>
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Recommended SEU Detecting FSM Approach

- **Coding style**
  - Describe normal FSM operation through “case” statement
  - Specify a one-hot FSM encoding
  - Specify error reporting mechanism in “default” / “when others”

- **Synthesis tool behaviour**
  - Implements all possible states (including those unspecified in RTL)
  - Generated logic has a defined behavior for each possible $2^n$ values of state bits
  - “Invalid States” transition to state specified in “default” / “when others”
Recommended Radiation Hardening Methods

1. Combinatorial-Combinatorial (C-C) mapping
   - Combines two combinatorial cells with feedback as opposed to using flip-flop

2. Triple Module Redundancy

3. Triple Module Redundancy using C-C mapping

C-C mapping prevents usage of the hardened clock trees
Local TMR Support
(What Synthesis Provides Today)

**Benefit:** SEU Protection

- Replace each sequential element with a macro of tripled flop + voter
- Combinatorial paths remain unchanged
- Recommended for Anti-fuse architectures
Messaging Customization & Reporting

**Benefit:** easier debug, deploy desired messaging policies

- Sort messages easily
- Cross-probe to relevant file and line number
- Control message settings in GUI (suppress, change severity)
- Control reporting level

**Tools > Set Options > Transcript Options**

![Screen shot of Transcript Options with options set for sorting and filtering messages.]

**Messaging Tabs**

![Screenshot of messaging tabs showing various messages with different severities and categories.]
FormalPro Integration

*Benefit*: Allows verification of synthesis results as desired

- Supports all families from Actel, Altera, Xilinx
- Automated setup of RTL vs. gates in Precision
- Post P&R check available also
  - See P&R tool docs for restrictions
FormalPro Integration (cont’d)

- Supported optimizations within synthesis
  - Merged registers
  - Duplicated registers
  - Inferred counters
  - Inferred static SRL
  - Eliminated registers
  - Re-encoded FSM

- Unsupported optimizations
  - Retiming
  - RAM/DSP inference
  - Gated-clock conversion
  - Physical synthesis
  - Incremental synthesis
Areas of Research

- Mentor Graphics is researching new technologies to facilitate mitigation of radiation effects
  - Automation of Requirements Tracing
  - Fault Tolerant FSM
  - Triple Module Redundancy

Attendees are encouraged to participate in the beta program

Contact precision_beta@mentor.com or your local Mentor Graphics representative for more information