New capabilities for fault tolerance in FPGA synthesis

R

ESA Radiation Effects Workshop

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R&D

Evolution of PLD/SEE parameters

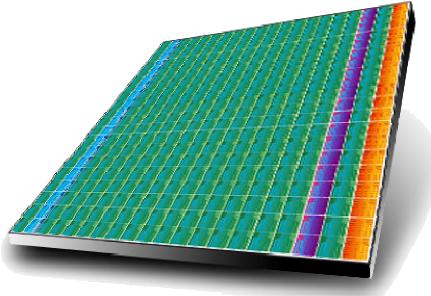
- Anti-fuse devices evolved
 - Increased capacity & operating frequency
 - Increased SET occurrence
- Adoption of SRAM-based devices
 - Further increases to capacity & operating frequency
 - Typically less hardened, needs scrub
- New mitigation approach needed for SRAM- and antifuse-based devices

	1999	2009
Process Geometry	~0.25µm	~65nm
Device Capacity	~20k gates	~20M gates
Operating Frequency	~20MHz	~150MHz
Relevant SEE	SEU	SEU & SET



Precision RTL Plus Overview

- Start Right
 - **Vendor Independence**
 - Standard language support
- Synthesize & Optimize
 - Out-of-the-box Quality of Results
 - Physically aware synthesis
 - ASIC Prototyping Support
- Achieve Design Closure
 - Award-winning analysis & debug
 - Incremental flows





What Synthesis Provides Today

capabilities for fault tolerance

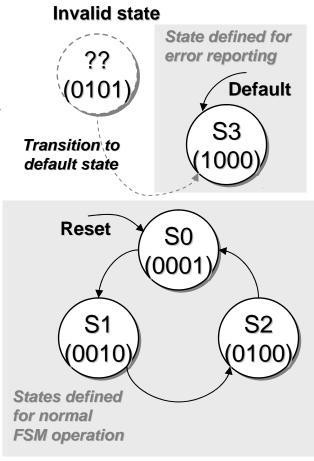
Feature	User Benefit, Problem Solved	
Safe FSM	Protection against getting stuck in invalid state caused by Single Event Upset (SEU)	
TMR support (Local)	SEU mitigation for Actel anti-fuse Families	
Message customization & reporting	 Easy to find relevant messages Messaging policies 	
Repeatability	Provides deterministic netlist for configuration sign-off	
FormalPro Integration	Automated setup and launch of formal equivalence check	



Recommended SEU Detecting FSM Approach

- Coding style
 - Describe normal FSM operation through "case" statement
 - Specify a one-hot FSM encoding
 - Specify error reporting mechanism in "default" / "when others"
- Synthesis tool behaviour
 - Implements all possible states
 (including those unspecified in RTL)
 - Generated logic has a defined behavior for each possible 2ⁿ values of state bits
 - "Invalid States" transition to state specified in "default" / "when others"

Safe FSM





Recommended Radiation Hardening Methods

DECIN CLK CLR

DEC 18

1. Combinatorial-Combinatorial (C-C) mapping

- Combines two combinatorial cells with feedback as opposed to using flip-flop
- 2. Triple Module Redundancy
- 3. Triple Module Redundancy using C-C mapping

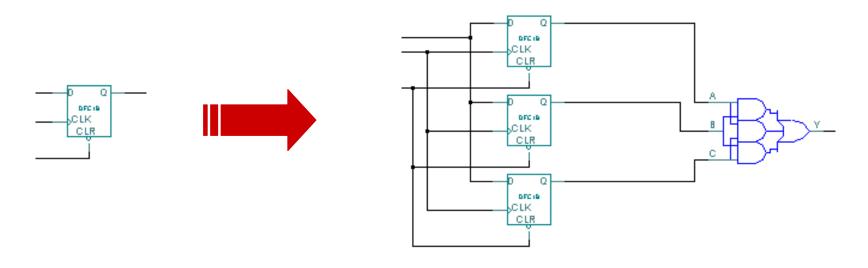
C-C mapping prevents usage of the hardened clock trees

2009 ESA Radiation Effects Workshop

Local TMR Support (What Synthesis Provides Today)

Benefit: SEU Protection

- Replace each sequential element with a macro of tripled flop + voter
- Combinatorial paths remain unchanged
- Recommended for Anti-fuse architectures





Messaging Customization & Reporting

Benefit: easier debug, deploy desired messaging policies

- Sort messages easily
- Cross-probe to relevant file and line number
- Control message settings in GUI (suppress, change severity)
- Control reporting level

Tools > Set Options > Transcript Options

29 Options						
Session Settings Editor Options	Transcript Options					
Transcript Options	Transcript					
Schematic Viewer	Show Message IDs Collapse Previous Command					
	Warning/Error Indicator foreground					
	Maximum Transcript Window Length (ines)					
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Messaging Tabs Messages View Warnings Information

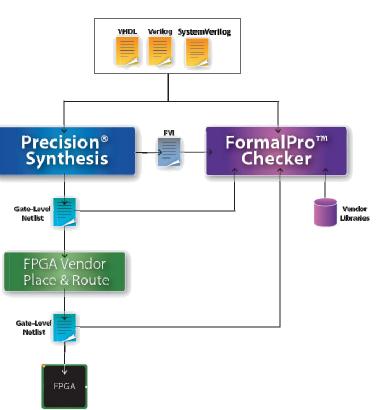
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FormalPro Integration

Benefit: Allows verification of synthesis results as desired

- Supports all families from Actel, Altera, Xilinx
- Automated setup of RTL vs. gates in Precision
- Post P&R check available also
 - See P&R tool docs for restrictions





FormalPro Integration (cont'd)

- Supported optimizations within synthesis
 - Merged registers
 - Duplicated registers
 - Inferred counters
 - Inferred static SRL
 - Eliminated registers
 - Re-encoded FSM
- Unsupported optimizations
 - Retiming
 - RAM/DSP inference
 - Gated-clock conversion
 - Physical synthesis
 - Incremental synthesis



Areas of Research

- Mentor Graphics is researching new technologies to facilitate mitigation of radiation effects
 - Automation of Requirements Tracing
 - Fault Tolerant FSM
 - Triple Module Redundancy

Attendees are encouraged to participate in the beta program

Contact precision_beta@mentor.com or your local Mentor Graphics representative for more information

