XRTC Use of Fault Injection to Simulate Upsets in Reconfigurable FPGAs

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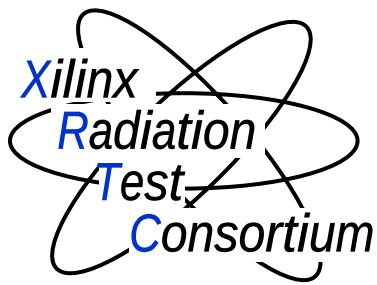
Overview

- Introduction - Reconfigurable FPGAs
  - Design-Level vs. Configuration-Level
  - Radiation Test Consortium (XRTC)
- XRTC Beam Tests - Methodology and Results
- Verifying Redundant Designs
- XRTC Fault Injector
- Lessons Learned So Far
- Future Directions

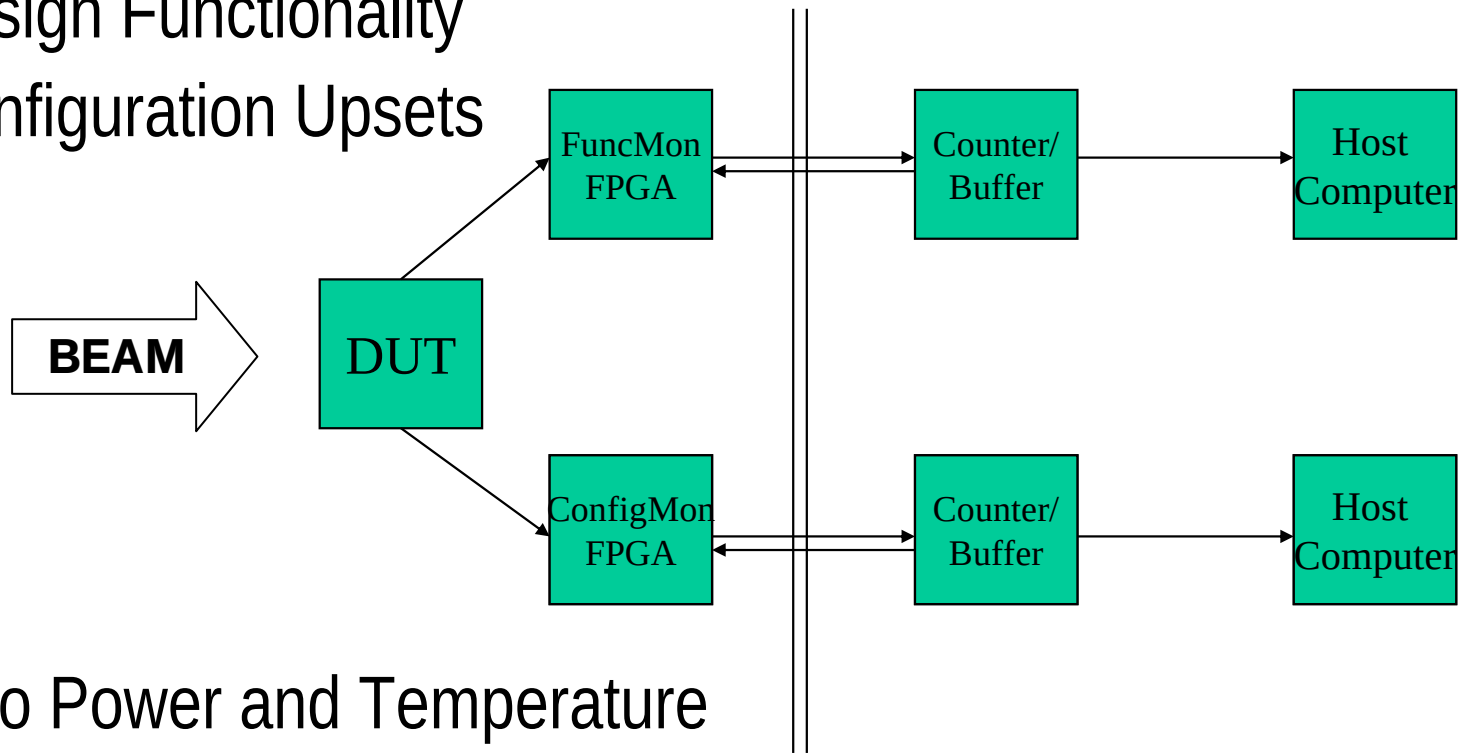


Introducing Virtex-4QV FPGAs

- Space-Grade Reconfigurable Family of Four
  - Guaranteed 300 krad(Si) and Latchup Immune
  - Bigger and More Powerful = More Complex
- Design-Level vs. Configuration Level
  - Triple Modular Redundancy XTMR
    - Resides in Design-Level Providing Upset Robustness
    - Protects Both Levels, but many more Configuration Upsets
      - Errors only on statistically “unlucky” coincident upsets
        - In two domains, same voted segment
        - During single scrub cycle (fraction of a second)
  - SRL16s, LUTROM, and LUTRAM Cross Levels
    - Formerly forbidden, new Virtex-4 feature allows their use

XRTC Beam Tests

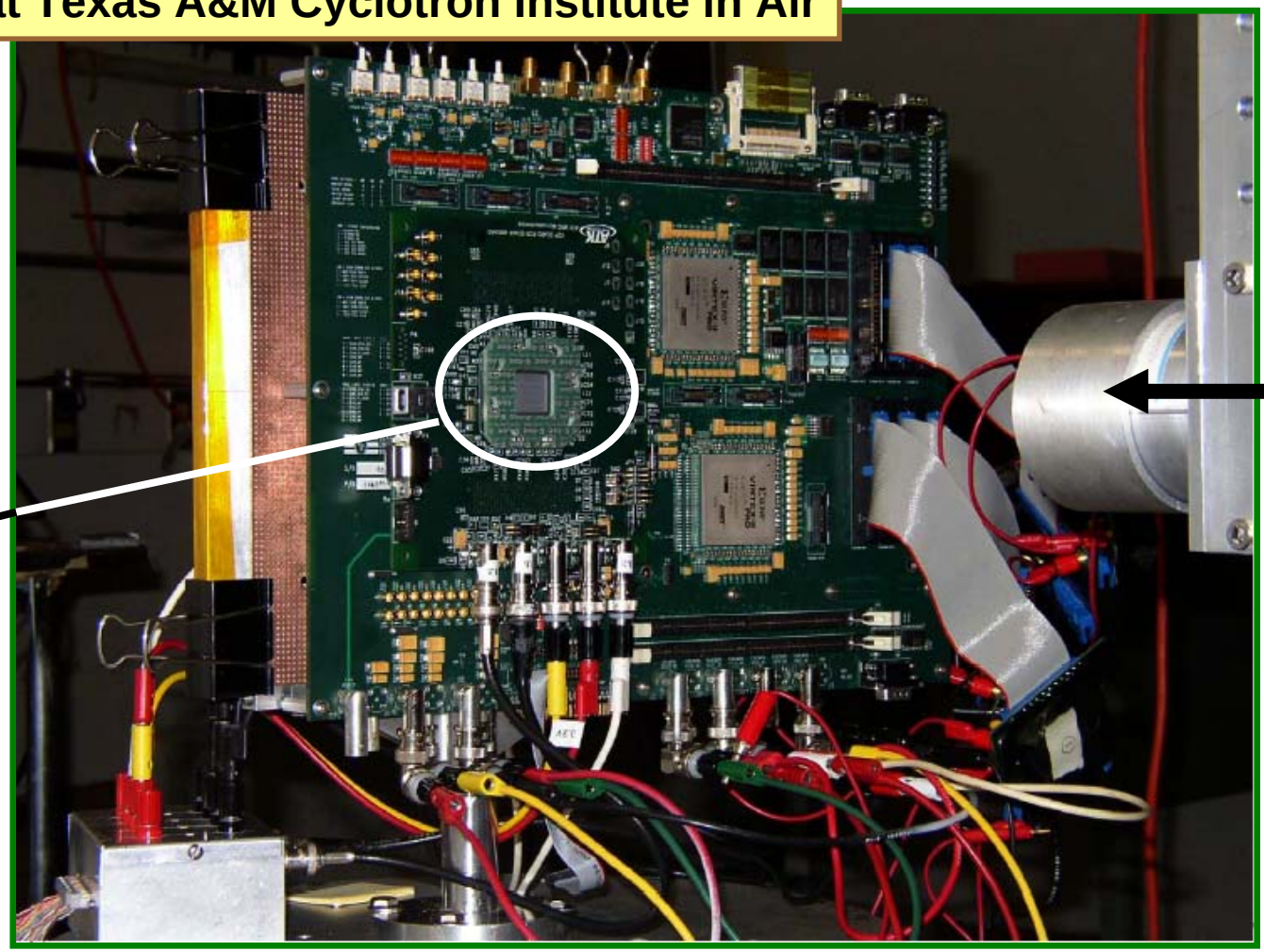
- Basic Philosophy: Continuous Monitoring with In-Beam Strip Charts of:
  - Design Functionality
  - Configuration Upsets



  - Also Power and Temperature

XRTC Apparatus

Testing at Texas A&M Cyclotron Institute in Air



XRTC Results – Space Upset Rates

- SEFI Rate is about one per century
- Unprotected Designs: a few upsets per day in GEO
- Mitigation makes these upset negligible
- Robustness at one error per century (SEFI Rate) with:
  - Design-Level: Triple Modular Redundancy
    - Assures no single-point of failure
  - Config-Level: Configuration Management
    - Prevents upset accumulation (transparent to design operation)
    - SEFI detection logic triggers reconfiguration (intrusive)

XRTC Fault Injector

Requirements

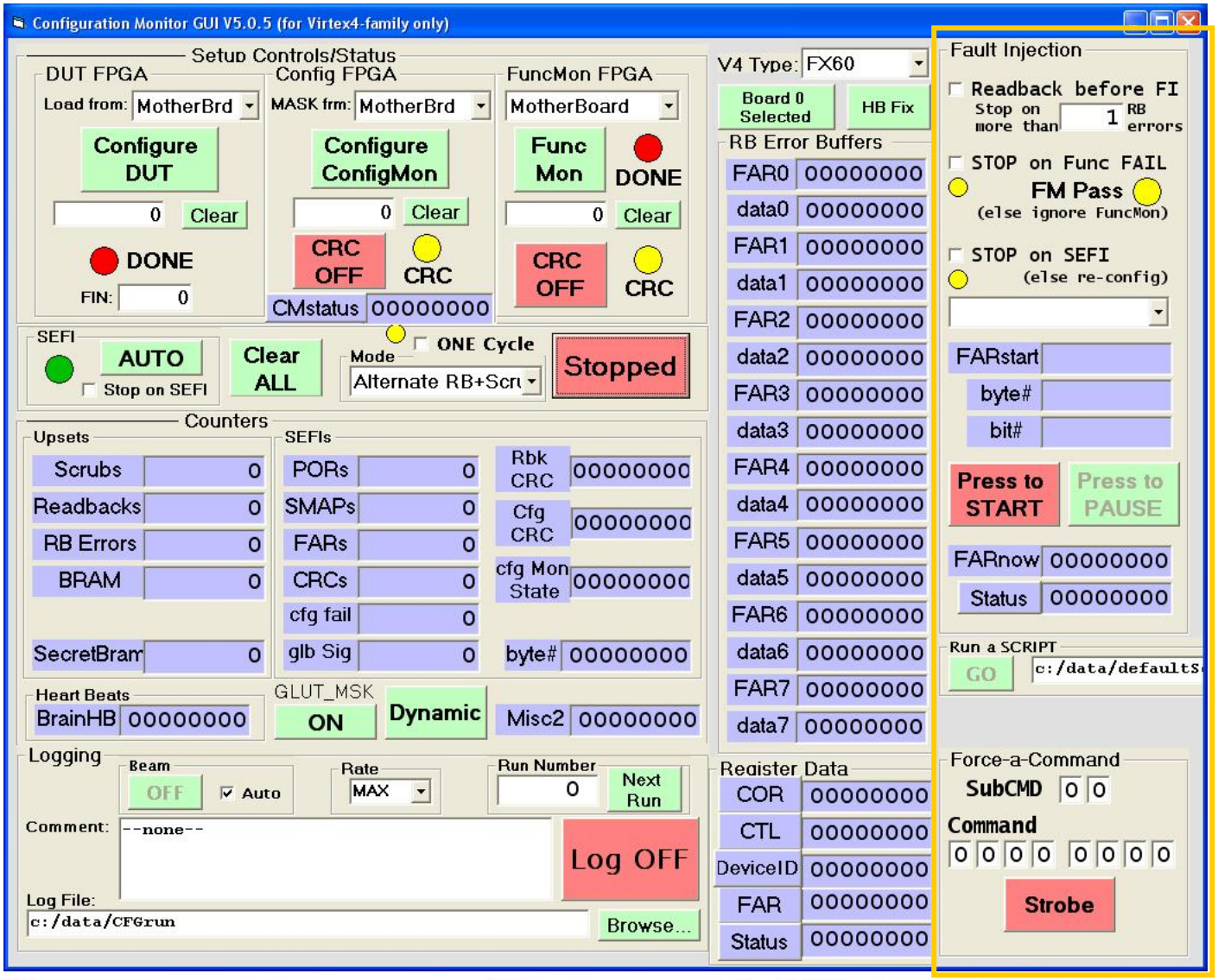
- Configuration-level Fault Injector (or Upset Simulator)
- Speed and ease of comprehensive single-bit injection
- Kernel command set allows any middle-ware approach
  - Either hardware or software generated commands
- No impact on DUT designs
- Minimum impact on FuncMon design
  - Only need to add-on error signalling to ConfigMon
  - Introduce an easy-to-adapt template for FuncMon add-on

XRTC Fault Injector

Same apparatus as for beam testing

- Leverage ConfigMon functionality without breaking it
- Kernel is add-on to ConfigMon
- First priority – Inject as fast as possible
  - Saves time by skipping intermediate “clean” frame
- Requires three- way coordination
  - Injector hands off to FuncMon after injecting fault
  - FuncMon tests functionality and reports results
  - Certain results cause ConfigMon to scrub or re-configure
- Scripting of kernel commands was natural addition

FaultMon GUI Addition



Same (new) ConfigMon GUI with FaultMon GUI "sidecar"

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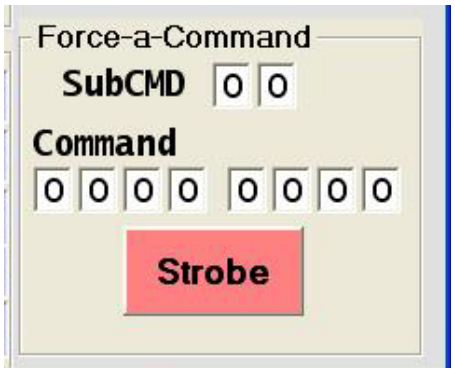
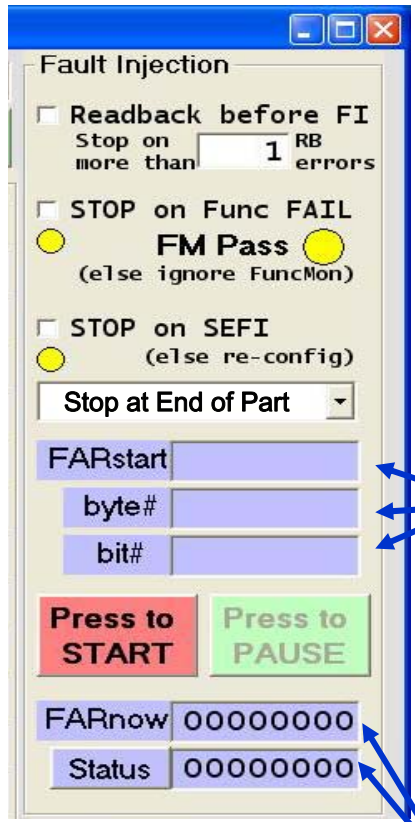
Three FaultMon GUI Controls

Manual Control
One operation at a time





1. Choose STOP condition(s)

Auto Control
Comprehensive single-bit fault injection

2. Choose starting point

3. Kick it off

Script Control
Execute a list of kernel commands

4. Observe it run

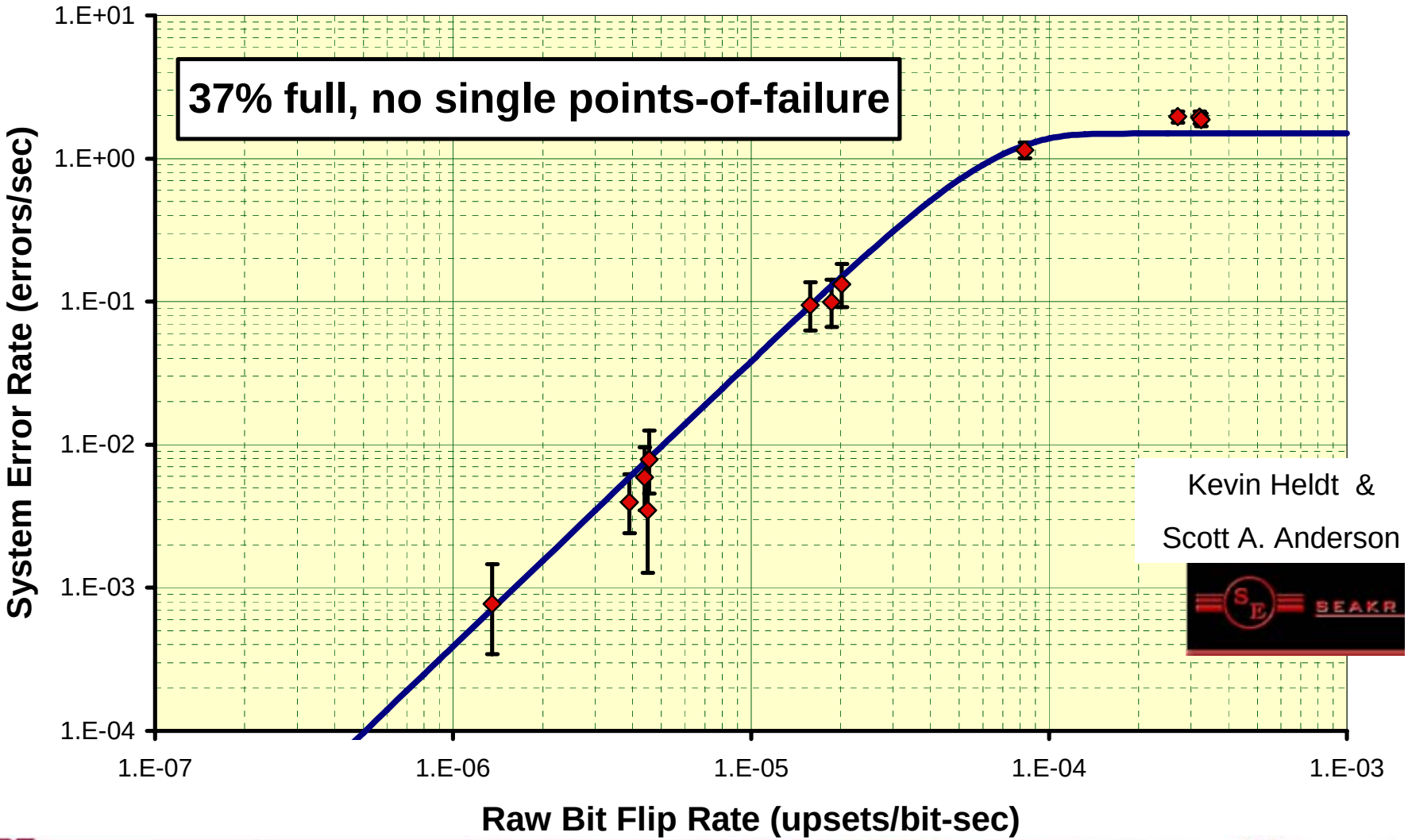
Fault Injection Lessons So Far

- Very useful to designers and beam testers
- Found 9 SelectMAP SEFI bits
- Found an I/O Test Bit on certain pairs of I/Os
- Many problems trace to state machine implementation
  - Modern synthesis tools may “optimize” in bad ways
    - Trimming “extra” states
    - Changing the type of state machine
- Still working out complications
  - Half-latches give inconsistent results
  - Not all detected single faults are “real”
  - Other inconsistencies being worked

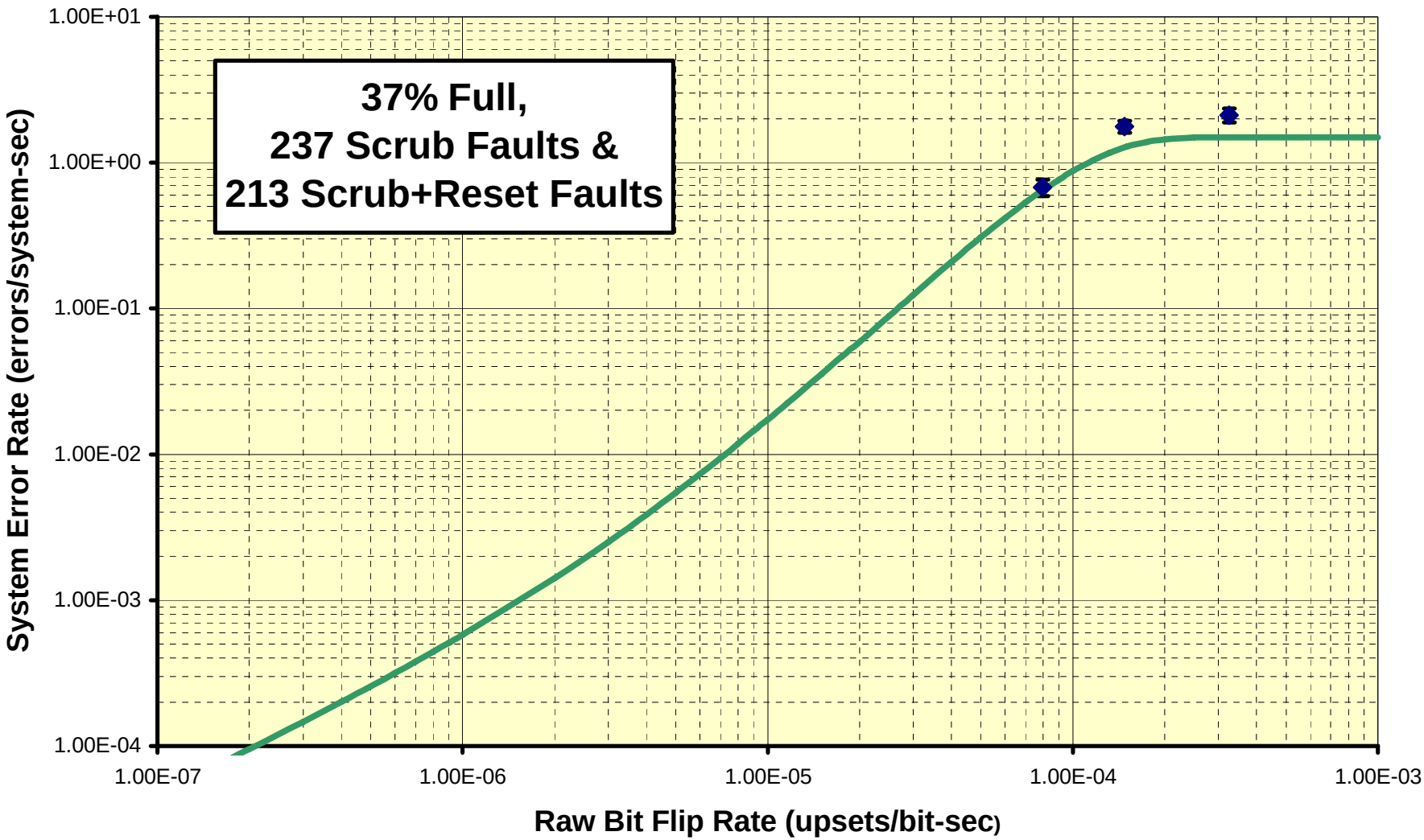
Future Directions

- Near-term – Replace and augment beam tests
  - Simulate tri-flux test
  - Simulate multi-bit upsets (MBUs)
    - Limitations of in-beam testing for robust TMR
      - Beam Time Required is Expensive
      - No Help with Locating of Problem Areas
- Longer-term – Expand to Flight Design Qual
  - May require expanded test platform

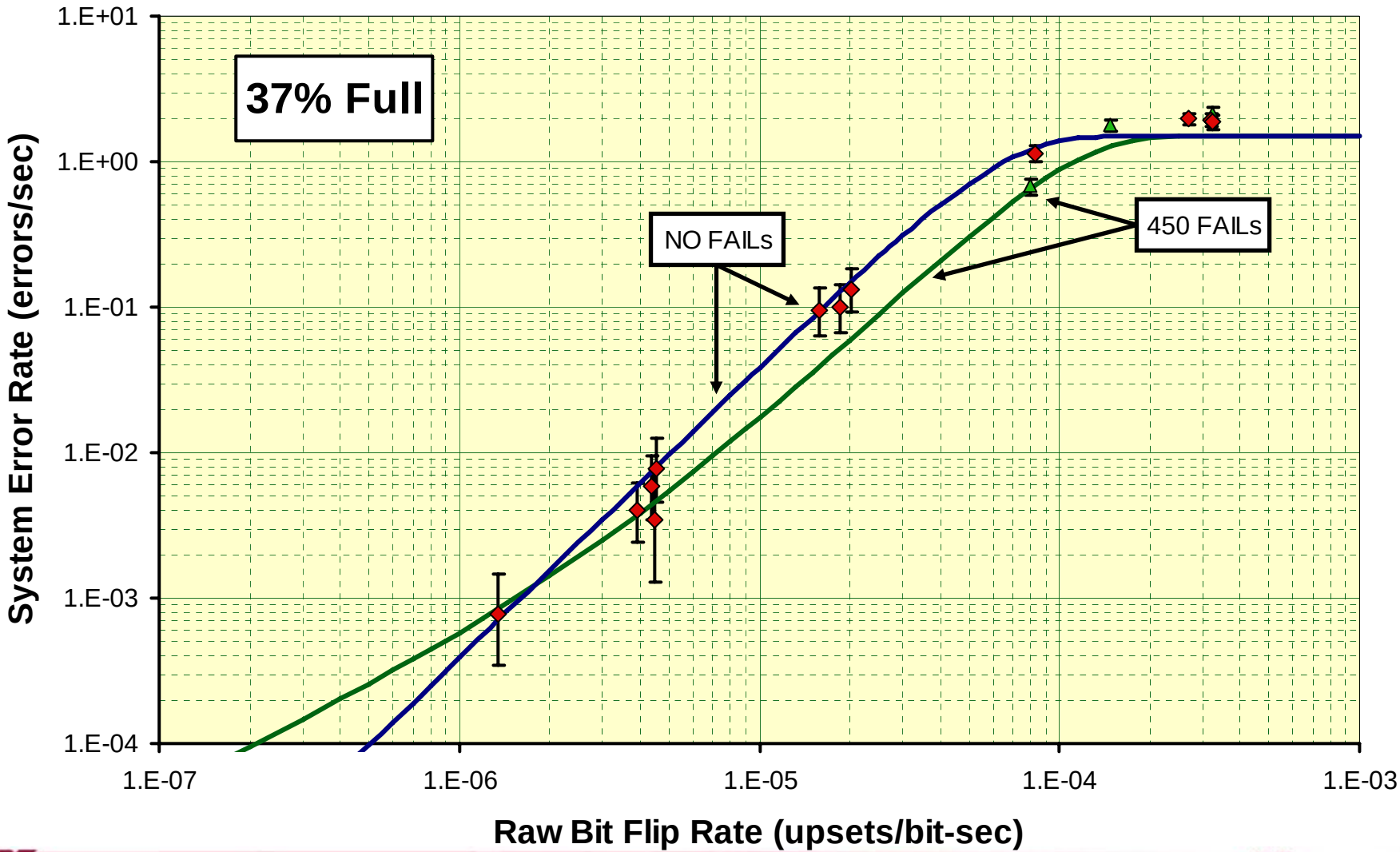
V-4QV TMR-Counter Results



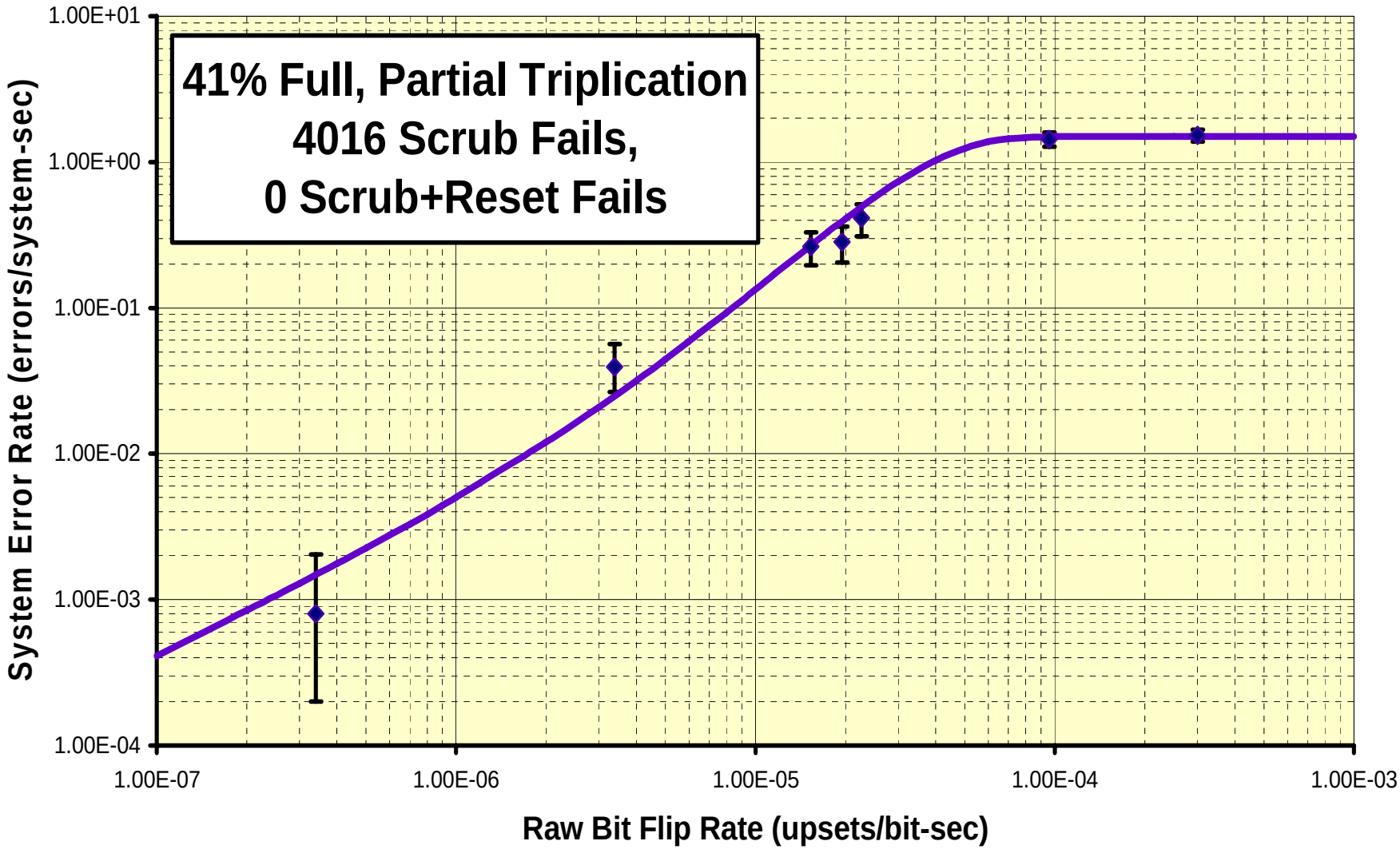
V-4QV TMR-Counter Results



V-4QV TMR-Counter Results



V-4QV TMR-Counter Results



Backup Material

- Virtex-4QV Devices and Features
- Space Upset Rate Examples
- Photos of XRTC Apparatus In Use

Virtex-4QV Devices

Architectural Features

	Description	XQR4V SX55	XQR4V FX60	XQR4V FX140	XQR4V LX200
CFG*	Configuration Bits* (millions)	15.4	14.5	34.5	43.0
BRAM	Block Memory Bits	5,898,240	4,276,224	10,174,464	6,193,152
LOGIC	Slices (2 Lookup Tables/slice)	24,576	25,280	63,168	89,088
DSP**	18x18 MACs**	512	128	192	96
PPC	PowerPC405 Processors	-	2	2	-
DCM	Clock Managers	12	12	20	12
MGT***	High-speed Transceivers***	-	N/A	N/A	-
IOBs	Input/Output Blocks	640	576	896	960

* Only real memory cells in the Configuration Bit Stream are counted here (not counting BRAM)

** MAC=multiply-and-accumulate block for digital signal processing (DSP)

*** MGTs are not supported for Virtex-4QV devices

Example Space Upset Rates

Configuration Cells

Orbit	Altitude (km)	Incl*	XQR4V SX55	XQR4V FX60	XQR4V FX140	XQR4V LX200	HI%
LEO	400	51.6º	0.73	0.69	1.61	2.03	69
	800	22.0º	7.56	7.12	16.7	21.1	2
POLAR	833	98.7º	6.02	5.67	13.3	16.8	22
MEO	1200	65.0º	23.3	21.9	51.6	65.1	5
GEO	36,000	0º	4.28	4.03	9.5	11.9	94

* Incl = Inclination HI% = fraction from heavy ions

Example Space Upset Rates

BRAM Cells

Orbit	Altitude (km)	Incl*	XQR4V SX55	XQR4V FX60	XQR4V FX140	XQR4V LX200	HI%
LEO	400	51.6º	0.72	0.52	1.24	0.75	84
	800	22.0º	4.05	2.94	6.99	4.25	5
POLAR	833	98.7º	4.00	2.90	6.90	4.20	37
MEO	1200	65.0º	13.3	9.63	22.9	13.9	10
GEO	36,000	0º	4.49	3.26	7.75	4.71	98

* Incl = Inclination HI% = fraction from heavy ions

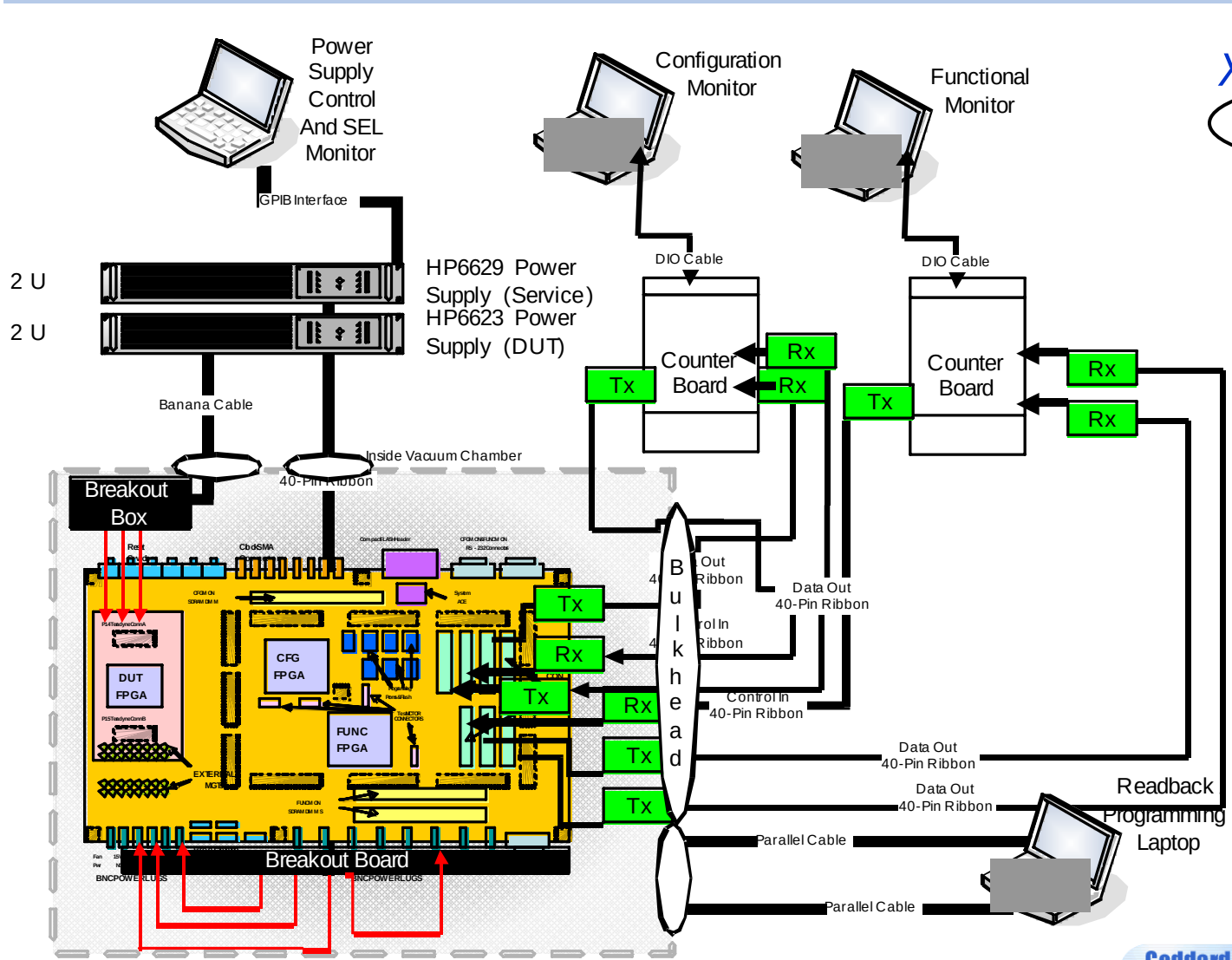
Example Space Upset Rates

Virtex-4QV SEFIs

Orbit	Altitude (km)	Incl*	SEFIs POR	SEFIs GSIG	SEFIs SMAP+	SEFIs **TOTAL**	SEFIs HI%
LEO	400	51.6º	1225	2161	1500	**515**	58
	800	22.0º	100	114	112	**36**	13
POLAR	833	98.7º	131	165	146	**49**	14
MEO	1200	65.0º	32	37	35	**11**	3
GEO	36,000	0º	225	560	290	**103**	91

* Incl = Inclination HI% = fraction from heavy ions
SMAP+ = SMAP & FAR SEFIs combined

Mature Test Methods & Apparatus



Xilinx Radiation Test Consortium

JPL

Boeing

SEAKR

NASA Langley Research Center Hampton, Virginia

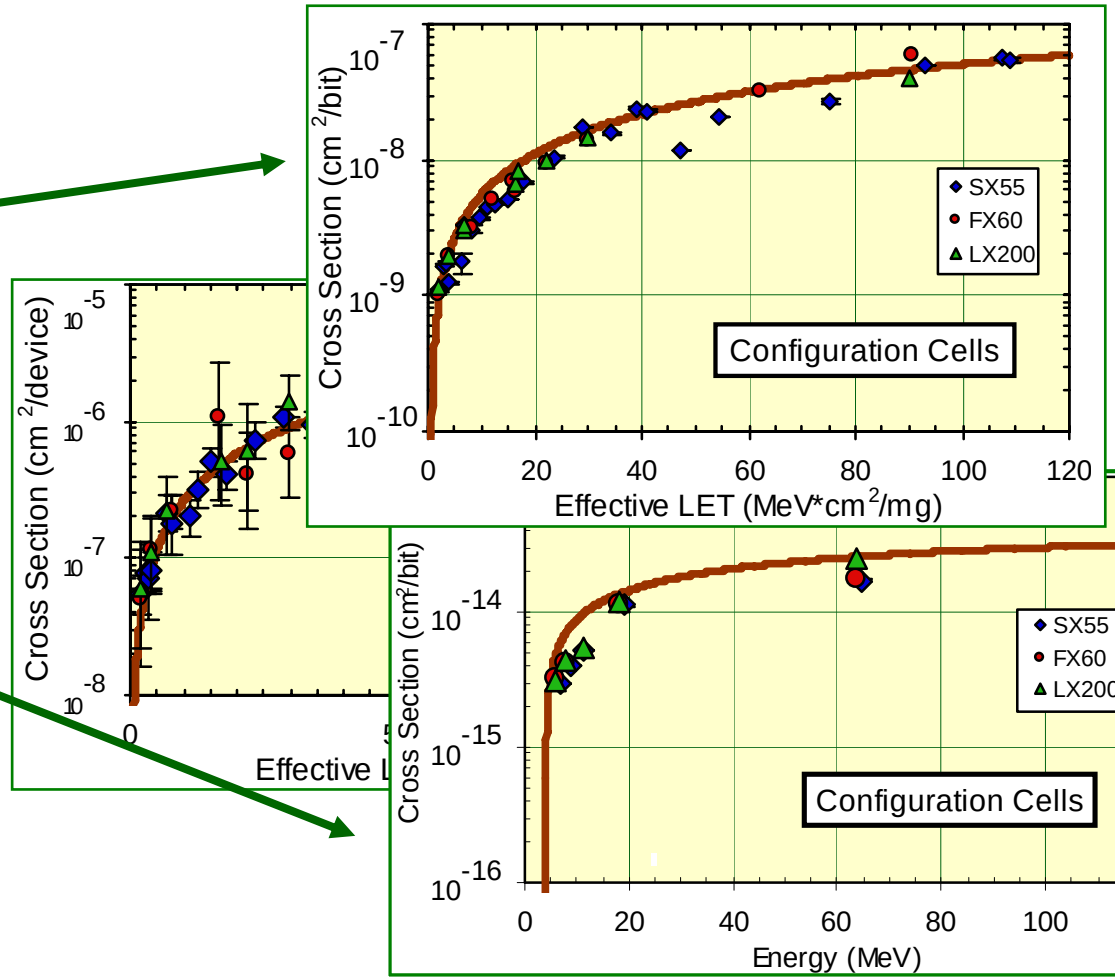
Los Alamos NATIONAL LABORATORY EST. 1943

NORTHROP GRUMMAN

Goddard Space Flight Center NASA

XRTC Beam Tests

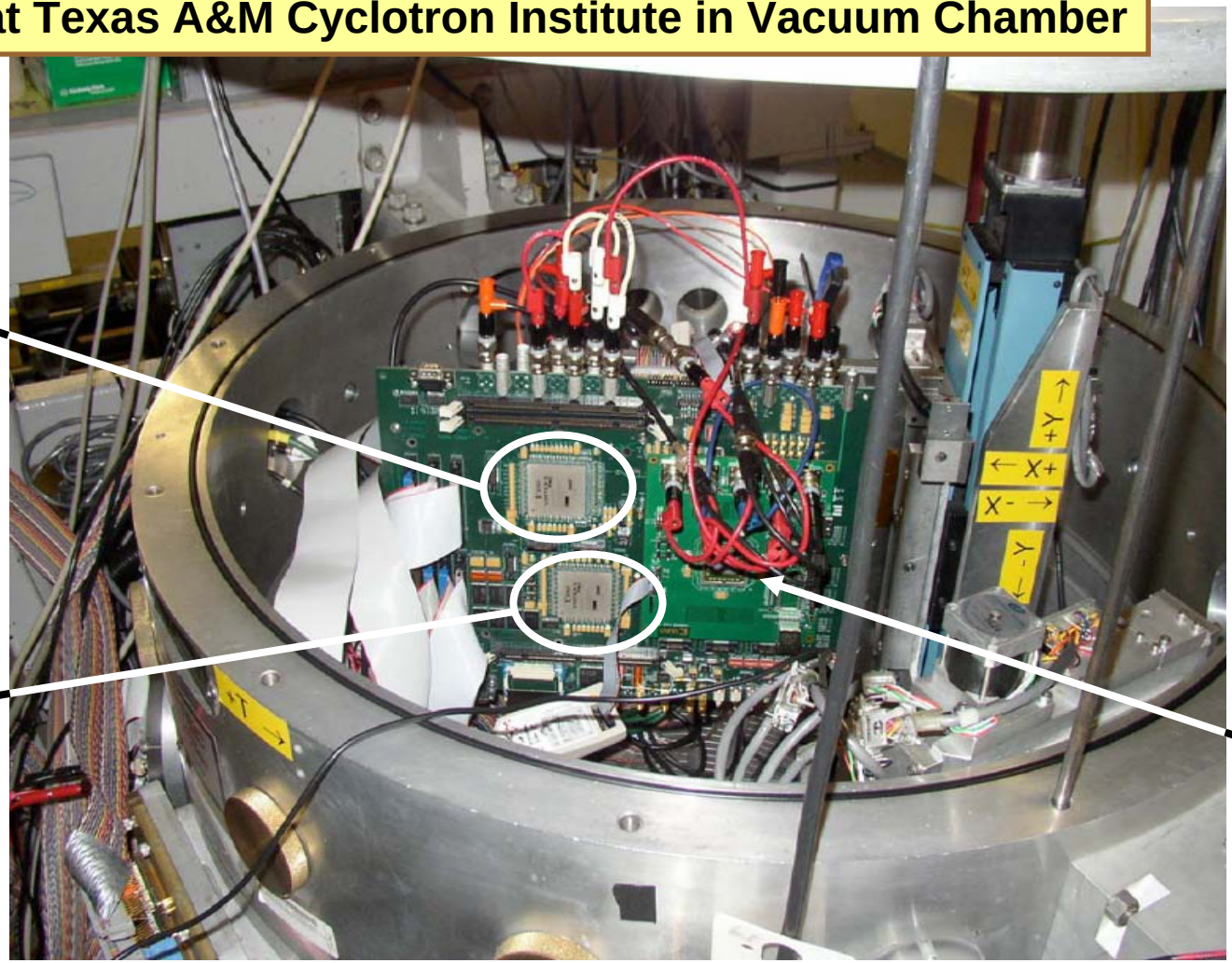
- Static Results
  - Config cells
  - User BRAM & FFs
  - Functional Upsets (aka SEFIs)
  - Both Protons & Heavy Ions



- Dynamic & Mitigation Campaigns Underway

XRTC Apparatus

Testing at Texas A&M Cyclotron Institute in Vacuum Chamber

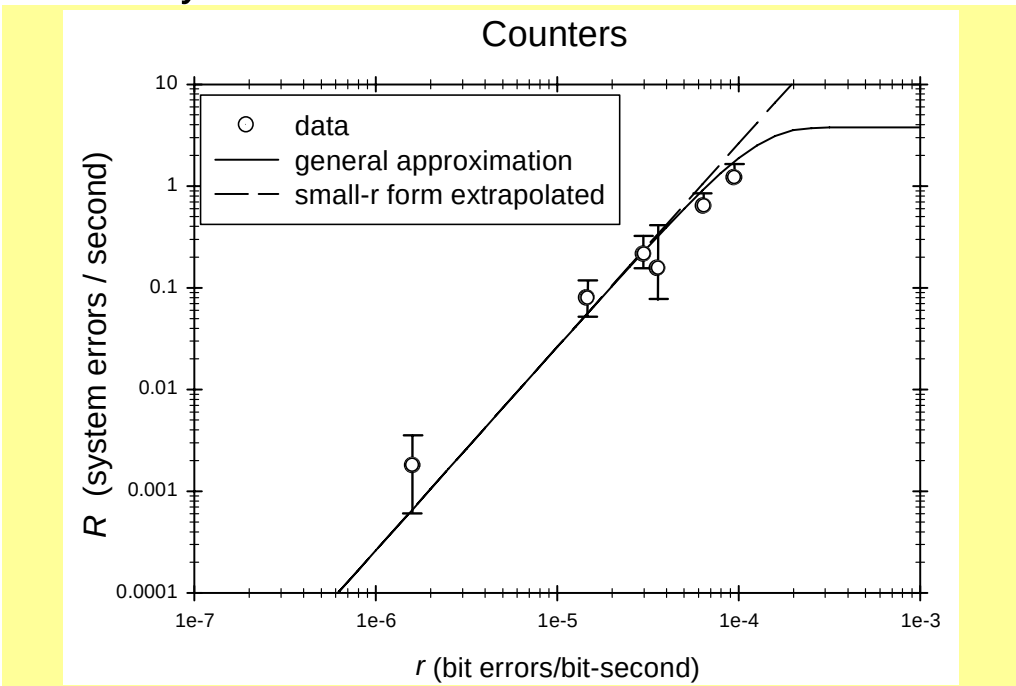


The TMR Verification Problem

- "Working" TMR may actually be broken
  - Stuck-at faults
  - Domain criss-crossing
- In the pathological case of only two working domains, a design's error cross-section is double!

The TMR Verification Problem

- Benchtop smoke test for three-leg functionality
- In-beam tri-flux test (expensive and non-specific)
  - Probability of a system error is approximately proportional to the square of upsets per scrub cycle



- Fault Injection (again)