SYDERAL

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1 INTRODUCTION

This document is the executive summary report of the contract 22043/08/NL/JK - Synthesizable VHDL IP Cores.

2 PROJECT OBJECTIVES AND SCOPE

The objective of the project was the development and validation of 2 IP cores:

- Advanced Memory Controller IP Core (AMEMCTL IP Core)
- Embedded File System Manager (EFSM IP Core)

The AMEMCTL IP Core executes following memory management functions:

- Mode management of the memory devices
- Initialization sequence at power-up according to the memories used
- Auto-refresh management (DDR2 only)
- Self-refresh management (retention mode, DDR2 only)
- Operational read/write mode according to the memories used
- Low-level interface with the memory devices
- Individual management of addresses according to read and write process
- Full or reduced memory test
- Scrubbing (with higher-level assistance for Flash)
- Local status management and switch-off control
- Data protection EDAC (Reed Solomon)

It interfaces two memory types:

- non–volatile NAND Flash memory
- volatile DDR2 SDRAM memory

The EFSM IP Core is a mass memory file system manager using a file allocation table principle. It main functions are to:

- provide sector address for data storage in a mass memory (write command)
- provide sector address for read data from the mass memory (read command)
- provide sector address in function of time (seek command)
- remove sector from files (delete command)

3 PROJECT PHASES

The project was divided into 3 phases:

- IP Definition Phase

  This phase was dedicated to the top-level functionality understanding and to the system requirements definition. This requirements definition phase was based on the preliminary IP Specification issued in the frame of the proposal and on the ESA comments and advices.

  The steps of the system development and the description of the test and validation execution were defined and described in the IP Verification Documents.

  The IP Datasheets were generated.

  The Specifications Review (SR) concluded this first phase.

- IP Architectural Design Phase

  Based on the documents issued during the definition phase, the IP architectural design was started. The design was broken down into modules and functions which were defined and described in the Architectural Design Documents.

  The functional description of the IP was then developed in VHDL code including test benches dedicated to the test and verification of the implemented functionalities. A preliminary IP database was issued.

  The IP Datasheet was updated to reflect the IP evolutions.

  The validation strategy of the IP was described in the Verification Plan document.

  This phase was concluded by the Architectural Design Review (ADR).

  On ESA request, the Datasheet, the Architectural Design Description and the Verification Plan (test case as well as database description) were compiled into one document, the IP User Manual.

- IP Detailed Design Phase

  During this project phase the IP was synthesized in the selected technologies and placed and routed in FPGA technologies.

  The IP Datasheets and Verification documents were updated with the performance and place and route results.

  The User Manuals were updated.

  The IP databases were updated.

  This task was concluded by the Final Review (FR).

4 DELIVERABLES

The following main items have been delivered during the project:

Title	Reference
EFSM IP core Specification	VIPC-SPE-001-SYD
EFSM IP core Architecture	VIPC-ADD-001-SYD
EFSM IP core Verification Plan	VIPC-PLN-002-SYD
EFSM IP Validation Report	VIPC-RPT-002-SYD
EFSM IP core Data Sheet	VIPC-SPE-003-SYD
EFSM IP Database (including source code and test bench)	
AMEMCTL IP core Specification	VIPC-SPE-002-SYD
AMEMCTL IP Architectural Design Description	VIPC-ADD-003-SYD
AMEMCTL IP Verification Plan	VIPC-PLN-003-SYD
AMEMCTL IP Design and Validation	VIPC-RPT-001-SYD
AMEMCTL IP core Datasheet	VIPC-MAN-001-SYD
AMEMCTL IP User Manual	VIPC-MAN-003-SYD
AMEMCTL IP Database (including source code and test bench)	

5 KEY-POINTS

The kick-off meeting took place on 13.11.2008 (with a T0 on 01.12.2008) and the contract was signed in December 2008.

The draft versions of the specifications of both IP Cores have been issued on 20.02.2009 and reviewed on 09.04.2009 with ESA. After several iterations, the EFSM IP Core specification has been updated on 02.11.2009 and 19.01.2010, the AMEMCTL IP Core specification on 22.01.2010. The Specification Review (SR) took place on 04.2.2010. After the update of both specifications (26.02.2010 and 07.07.2010 resp. 27.08.2012), the issue of the data sheets (27.04.2010 and 07.07.2010 resp. 27.08.2012) and of the verification plans (27.04.2010), the SR could be closed on 01.09.2010.

In the meantime (mid May 2010), SYDERAL gained the Earth Care MMFU contract (Mass Memory and Formatting Unit). This project was very challenging. Part of the team working on VHDL IP Core (VIPC) activities has been assigned to this new project, so putting VIPC de facto in second priority. Furthermore, as it was foreseen to reuse both IP Cores on Ng-SSMM and EC-MMFU, we have spent time to check the IP Core specifications against these two projects. This has delayed the issue of the new versions of the specifications, and consequently of the effective start of the VHDL IP coding.

The development and validation activities of the AMEMCTL IP Core have been subcontracted to the HES-SO (Swiss engineer school) on 18.05.2010 to compensate for the lack of resources. The EFSM IP Core activities have been for their part kept at SYDERAL.

The first version of the VHDL code for both IP Cores has been transmitted in Dec '10.

Year 2011 has been spent on the coding of the VHDL codes and of the test benches. This activity could be finished that year for the AMEMCTL IP Core that was subcontracted, but not for the EFSM IP Core that was developed internally and that faced resources problems. A letter concerning the delay of activities and the lack of reporting was received in Nov '11.

Year 2012 has been spent on the finalising of the VHDL codes and the test benches, and on the verification activities of both IP Cores. Two telecons took place in May with ESA and our subcontractor. The Architectural Design Review (ADR) took place on 29.11.2012 based on the documentation and data bases sent on 10.09.2012. At this review, ESA asked to merge, for each IP Core, the Datasheet, the Architectural Design Description and the Verification Plan (test case as well as database description) into one document, an IP User Manual.

A second letter concerning the delay of activities was received in June '13 as SYDERAL had difficulties to terminate the contract due to the high pressure put by our Customer on the EC-MMFU project. Finally, the EFSM and AMEMCTL IP Core databases could be updated according to ADR outcomes and delivered on 09.07.2013, so leading to the closure of the ADR milestone on 16.07.2013.

6 DIFFICULTIES ENCOUNTERED

The main difficulties encountered during the realization of this contract concerned the elaboration of the specifications, the management of the resources and the scope of the project.

Elaboration of the specifications

The difficulty was twofold. First, a difficulty inherent to the activity, i.e. to have the same understanding of the IP Cores functionality shared between ESA and SYDERAL. Second, we have tried to incorporate into the generic specifications the specific requirements of two projects (NgSSMM and EC-MMFU) gained by SYDERAL.

Management of the resources

The key resources foreseen at the beginning of the project could not be allocated as needed, due to the gain, in the meantime, of a challenging contract (Earth Care MMFU) and to the underestimation of the work to be performed. These two aspects have led to a significant delay in the execution of the contract, though part of the work has been subcontracted.

Scope of the project

Already during the discussion of the draft specifications (09.04.2009), SYDERAL has identified discrepancies between the contract negotiation and the current view of IP Cores.

This has also been discussed during the telecon held on 27.11.2009: "The complexity of the memory management (AMEMCTL IP) has significantly increased since proposal and negotiation. This IP has evolved from a "simple" memory chip controller to a mass memory controller with redundancy management. In consequence, SYDERAL is no more able to develop an IP including all foreseen memory types. It has been agreed to describe in the AMEMCTL IP specification only the Flash and DDR2 memories and to decide at Specification Review if only one or both types have to be implemented."

In addition, in the progress report dated 20.12.2010, SYDERAL has written: "The complexity of the work to be performed under the VHDL IP Core contract has been significantly underestimated.

Furthermore our understanding of the scope of the IPs has evolved in a non-negligible way since our proposal, as already mentioned at the SR. This is in this sense that we propose a descoping of the activities." The descoping was partially accepted by ESA.

7 CONCLUSION

Despite the time needed to get to the end of this project due to the numerous iterations that were necessary in each phase and to the lack of resources allocated to the activities, two new configurable IP Cores, one dedicated to file management (EFSM), the other one to memory control (AMEMCTL) are now available for further developments.

SYDERAL would like to thank here all participants to this project.