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ESA Contract 18533/04/NL/JD

CALL-OFF ORDER 3, Development of LEON3-FT-MP

SUMMARY REPORT

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1 Introduction

1.1 Scope

This document summarizes work performed under Call-Off Order 3 for the ESA Contract 18533/04/NL/JD, Development of LEON3-FT-MP. The objective of the project was to evaluate and validate multi-processing and fault-tolerant capabilities of LEON3-FT and GRFPU cores. A multi-core design based on the two IP-cores was defined and served as verification and validation platform. eCos and RTEMS operating systems multi-processing extensions were also verified and validated.

1.2 Reference documents

The LEON3-FT-MP design is based on GRLIB, and uses the GRLIB AMBA plug&play configuration method. The following manuals should therefore be carefully studied in order to understand the design concept:

- RD1: GRLIB User's Manual 1.0.5
- RD2: AMBA Specification 2.0
- RD3: GRLIB IP Core's Manual 1.0.5
- RD4: LEON3-FT-MP Requirement Analysis Report(L3FT-REP-0001, issue 1, rev 2)
- RD5: LEON3-FT-MP Design Specification (L3FT-REP-0002, issue 1, rev 2)
- RD6: LEON3-FT-MP Verification and Validation Plan (L3FT-REP-0003, issue 1, rev 3)
- RD7: LEON3-FT-MP Design Modifications Report with Architectural Description, (L3FT-REP-0005, issue 1, rev 2)
- RD8: LEON3-FT-MP Verification Report (L3FT-REP-0006, issue 1, rev 2)
- RD9: LEON3-FT-MP Validation Report (L3FT-REP-0007, issue 1, rev 2)
- RD10: GRMON User's Manual, version 1.1.11
- RD11: LEON3-FT-MP Validation Board Specification, rev 0.1
- RD12: LEON3-FT-MP Validation Board User's Manual, rev 0.1

2 Overview

The main purpose of the work that has been performed by Gaisler Research during the Call Off Order 3 of the ESA Contract 18533/04/NL/JD was to prepare the development of the future generation of ESA microprocessor. The project code name for that processor is GINA (Giga INstruction Architecture) that has the ambition to provide installed 1GIPS and 1 GFLOPS computing capability in a single device and provide multiprocessing capability.

The work has been performed by Gaisler Research in the Call-Off Order 3 under the ESA Contract 18533/04/NL/JD in the period from September 2005 to April 2006.

The main objective of activity was to develop a multiprocessing system which would serve as a platform for verification and validation of LEON3-FT and GRFPU IP-cores that could be used for the GINA processor. The full multiprocessor system has been first verified and then implemented on a Virtex 4 FPGA.

The work was divided into three work packages.

2.1 Work Package 1: Requirements Analysis and Specification

The main tasks of the WP1 were to produce LEON3-FT-MP Requirements Analysis Report (RD4) and LEON3-FT-MP Design Specification (RD5). The proposed design is a multi-processing system based on 4 LEON3-FT cores, each one with GRFPU floating-point unit and SPARC V8 Reference MMU (SRMMU). Design also includes several communications interfaces such as Spacewire, Ethernet, PCI and CAN. The design meets requirements on future space products based on LEON3-FT and GRFPU IP-cores which are assumed to be implemented on 0.13 um CMOS process and will run at approximately 250 MHz. Requirement analysis focused on multiprocessing and fault-tolerant capabilities of LEON3 and GRFPU IP-cores. Requirements on eCos and RTEMS operating systems multi-processor extensions were also identified. LEON3-FT-MP Verification and Validation Plan (RD6) was produced under this work package.

2.2 Work Package 2: Design Adaption and Verification

VHDL design of the LEON3-FT-MP system was performed during the Work Package 2. The work included configuration of GRLIB IP-cores to meet the requirements on the multi-processing and fault-tolerance capabilities identified during the WP1. Multi-processing extensions of eCos and RTEMS operating systems were added. The design architecture and modifications of eCos and RTEMS operating systems are described in Reference Document 7, LEON3-FT-MP Design Modifications Report and Architectural Description. Verification was focused on two IP-cores: LEON3FT and GRFPU and eCos and RTEMS operating systems. Verification of the IP-cores was performed by means of VHDL simulations, while the correct function of the operating system extensions was verified using the GRSIM behavioral simulator.

2.3 Work Package 3: Board Development and Validation

Hardware/software validation was performed during Work Package 3 (WP3). GR-CPCI-XC4LX200 board was used as platform. The board hosts a high-capacity Xilinx Virtex-4 FPGA device which was used to implement the LEON3-FT-MP design. The validation was performed by running eCos and RTEMS test suites on LEON3-FT-MP design. GRMON error injection feature was used to simulate SEU errors in LEON3-FT and GRFPU on-chip memories.

3 LEON3-FT-MP Architecture

3.1 Overview

The LEON3-FT-MP consists of four LEON3-FT processor cores and a configurable set of additional IP cores. The requirements analysis showed that it is not feasible to use one clock-domain for the whole design since this would limit the maximum achievable clock frequency. The bus architecture is therefore based on two AMBA AHB buses; a high-speed bus connecting the processor cores and the SDRAM memory controller, and a low-speed bus for communications IP cores (figure 1).

LEON3-FT-MP / GINA

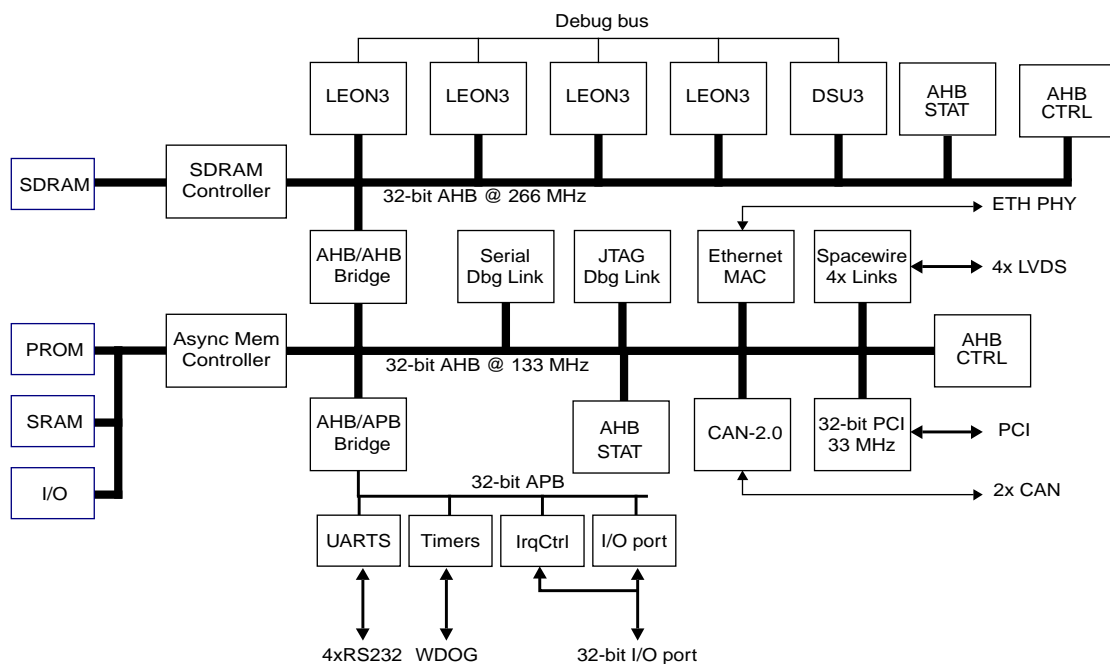


Figure 1. LEON3-FT-MP block diagram

The on-chip communications interfaces include four spacewire links, one ethernet 10/100 Mbit MAC, two CAN-2.0 interfaces, one 32-bit PCI interface and four serial UARTs. For debugging, both serial, JTAG and Ethernet debug DSU interfaces are provided. Legacy cores such as an interrupt controller and timer unit is provided to support the hosting of common operating systems. A 32-bit I/O port is provided for controlling of external devices.

3.2 LEON3-FT IP-core

The LEON3-FT-MP design is based on the LEON3-FT SPARC V8 processor. The processor configuration consists of 16 + 16 Kbyte I/D cache with 2-set LRU replacement. The SRMMU is enabled and configured with 16 + 16 separate I/D TLB entries and LRU replacement. Each CPU in the design is configured to use GRFPU floating-point unit. SEU protection is enabled for the register files and cache memories.

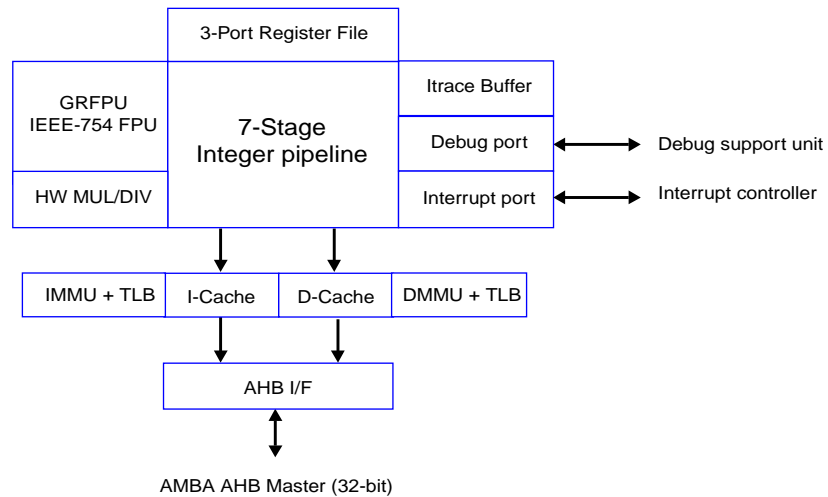


Figure 2. LEON3FT processor core block diagram

3.3 Communication Interfaces

3.3.1 Spacewire links

The LEON3-FT-MP includes four Spacewire links. Each link is controlled separately through the APB bus, and transfers received and transmitted data through DMA transfer. Two of the Spacewire links are configured with Remote Memory Access Protocol (RMAP) support in hardware. All links can operate up to 400 Mbit/s.

3.3.2 CAN interface

A dual CAN-2.0 interface is provided in form of a Philips SJA1000-compatible CAN core.

3.3.3 Ethernet

An ethernet interface based on Gaisler Research's GRETH ethernet MAC is included. The MAC has a built-in debug communication protocol and provides debug communication link (EDCL). The EDCL allows debugging and downloading of applications with up to 50 Mbit/s.

3.3.4 PCI Interface

A 32-bit PCI interface is provided, based on the GRPCI core. The PCI operates at 33 MHz and supports Master, Target and System Controller operations. The PCI core includes one DMA channel for autonomous data transfers, but can also be accessed directly by any AHB master. A separate PCI arbiter provides PCI arbitration and bus control.

3.3.5 UARTs

Four UARTs can be configured in the design. The UARTs are configured with flow-control, 16 byte transmit and receive FIFOs.

3.3.6 General purpose I/O port

A general purpose I/O port (GPIO) is provided in the design. The port is 32 bits wide, and each bit can be dynamically configured as input or output. GPIO can route external inputs to 15 APB interrupt lines allowing external devices to generate interrupts.

3.4 Other IP-cores

3.4.1 Timer unit

The timer unit consists of a common 16-bit scaler and 7 individual timers. The timers can work in periodical or on-shot mode. Timer 7 can optionally be configured as a watchdog. One timer per CPU is used to generate time ticks used by operating systems (eCOS, RTEMS), while other three timers can be used by applications. The timers use individual interrupts.

3.4.2 Interrupt controller

The interrupt controller handles up to 15 interrupts in two priority levels. The interrupt are automatically assigned and routed to the controller through the use of the GRLIB AMBA plug&play system. Interrupt controller contains one watchdog per CPU.

4 Software

4.1 Introduction

Software tools used in this project were based on proven BCC and RCC cross-compiler systems. eCos and RTEMS operating systems were adapted to support multi-processing capabilities of the LEON3-FT-MP system. eCos and RTEMS represent two approaches to multi-processing, eCos uses true shared memory synchronous multi-processing (SMP), while RTEMS nodes use message passing for communication between nodes. Both eCos and RTEMS were adapted to run simultaneously on different CPU nodes. Additional tests were performed in order to test certain behavior which is not tested by eCos and RTEMS test suites.

4.2 RTEMS

Each CPU node in an RTEMS multi-processing system runs its own program image. Communication between nodes is done by message passing through a shared memory buffer. The Shared Memory Support Driver which provides routines for message-passing between CPU nodes has been added. 4 Kbyte large memory buffer is reserved for Shared Memory Driver and used for message passing between CPU nodes. Atomic (exclusive) access to the shared memory buffer is implemented using SWAP instruction.

4.3 eCos

eCos supports true shared-memory multi-processing (SMP). All CPU nodes execute the same program image. A multi-threaded application is automatically distributed on available nodes without need for message passing. eCos has been adapted to be able to run simultaneously with RTEMS on different CPU nodes.

5 Verification

5.1 Introduction

The main objective of the verification was to verify multi-processing and fault-tolerant capabilities of LEON3-FT and GRFPU cores, and to verify correct function of multi-processing extensions of eCos and RTEMS operating systems. Verification of LEON3-FT and GRFPU IP-cores was done by means of VHDL simulations, while the verification of the eCos and RTEMS multi-processing extensions was performed by simulation in GRSIM behavioral simulator.

5.2 VHDL Simulations

LEON3-FT-MP model was simulated inside three different test benches:

- GRLIB test bench: Tests basic functionality of LEON3-FT core including: IU register file, SPARC V8 multiply/divide instructions, cache system and interrupt handling. Peripherals which are not part of the LEON3-FT core but are essential for multi-processing systems are also tested. These tests include multi-processor interrupt controller, timer unit and DSU operation tests.
- SPARC V8 Test Suite: test that all (implemented) instructions are compliant with SPARC V8 architecture specification.
- GRFPU test bench: Test all floating-point operations, both in single and double precision mode.

Fault-tolerant capabilities of the cores was tested by enabling error-injection in VHDL model. This feature inserts single-bit error in all on-chip memory blocks of LEON3-FT core including IU and FP register files and cache memories. More than 100 000 errors were injected during the verification. All tests were successful, both with error injection disabled and enabled.

5.3 GRSIM Simulations

Correct function of multi-processing extension of eCos and RTEMS operating systems was verified by running test suites in GRSIM behavioral simulator. GRSIM does not implement error injection and thus correct function of multi-processing extensions was verified in non-fault conditions.

5.4 Verification Results

Basic functionality of the LEON3-FT and GRFPU IP-cores has successfully been verified by means of VHDL simulations. Fault-tolerant capabilities of the cores have been successfully verified through error injection on VHDL level.

Correct function of eCos and RTEMS multi-processing extensions has been successfully verified on the GRSIM behavioral simulator.

Result of the LEON3-FT-MP verification are described in Reference Document RD8, LEON3-FT-MP Verification Report.

6 FPGA Design

GR-CPCI-XC4V-LX200 board which incorporates large capacity Xilinx Virtex-4 FPGA device was used as validation platform. The large capacity FPGA device fits whole LEON3-FT-MP system. The synthesis was performed using following tools:

- Synplify Pro, version 8.4 and 8.5
- Xilinx ISE Foundation tools, version 8.1

Synthesis scripts were automatically generated using GRLIB's built-in functions in completely automatic manner. Whole FPGA design process was intended to be completely automatic, however a large number of problems and difficulties showed up during synthesis process.

Synplify Pro crashed when synthesizing LEON3-FT-MP system. The tool reported internal error and exited when performing optimization on GRFPU. The problem was solved by partitioning design. The GRFPU was synthesized with Synplify Pro, version 8.4 and linked with the rest of the design during the place&route step.

Xilinx ISE Foundation tools had also problems with the design. The Xilinx Mapper crashed on the LEON3-FT-MP netlist with segmentation fault without giving any error message and making it very difficult to identify the problem. Since it was possible to synthesize smaller designs, based on GRLIB cores, a lot of effort was done to identify the part of LEON3-FT-MP design which caused the internal error in the mapper. However, we discovered that the problem was related to on which platform the Xilinx tools were running. The same netlist that crashed Xilinx mapper running on Linux was successfully mapped on a Windows workstation (Linux and Windows mappers had same version number). To run Xilinx tools on Windows was not a complete solution to the problem since the Xilinx Place&Route program (par) crashed on Windows (also with internal error). But this time the output from the mapper could be given to place&route program running on Linux which completed successfully and produced correct bit-file which was used to program the FPGA. The final process was to run mapper in Windows and to run place&route in Linux. Obviously, the Xilinx tools have problems with large designs such as LEON3-FT-MP since a perfectly correct netlist or ncd-file (mapper output) crashed a Xilinx tool on one platform but completed successfully on another one.

Mapper completed successfully only when running with default options. If the effort level was changed or mapping mode changed to timing-driven mapping which usually gives much better results, the mapper crashed.

With this problematic synthesis flow maximum achievable clock frequency was 40 MHz for the high-speed bus and 20 MHz for low-speed bus. The area usage was 130 000 LUTs which is 65% of the devices available logic cells.

7 FPGA Board

An FPGA board incorporating high capacity Virtex-4 FPGA has been developed during this activity. The objective was to provide a validation platform for the complete 4-processor LEON3-FT-MP system. The developed GR-CPCI-XC4LX200 board provides a capability to host LEON3-FT-MP system and all necessary interfaces.

The features of the GR-CPCI-XC4VLX200 board include:

- Compact-PCI plug-in form factor
- Virtex-4 XCVLX200-FG1513-10 FPGA
- 16 Mbyte FLASH PROM
- 1 standard SO-DIMM socket for up to 512 Mbyte SDRAM
- Ethernet PHY 10/100 Mbit transceiver
- Standard RS-232 UART port
- 120-pins memory and custom I/O expansion connectors
- CPCI system controller (clock distribution & PCI arbitration)

The block diagram of the GR-CPCI-XC4VLX200 board is shown in figure 3.

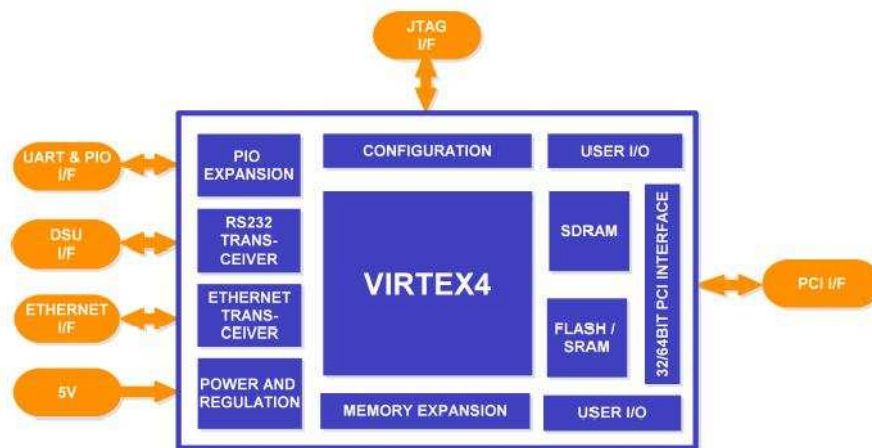


Figure 3. GR-CPCI-XC4VLX200 block diagram

High-capacity Virtex-4 FPGA and set of standard interfaces makes the GR-CPCI-XC4VLX200 board suitable as platform for the LEON3-FT-MP system. The design was successfully implemented on the board which served as platform for hardware/software validation.

For GR-CPCI-XC4VLX200 board specification and user's manual refer to Reference Documents 11 and 12: "LEON3-FT-MP Validation Board Specification" (RD11) and "LEON3-FT-MP Validation Board User's Manual" (RD12).

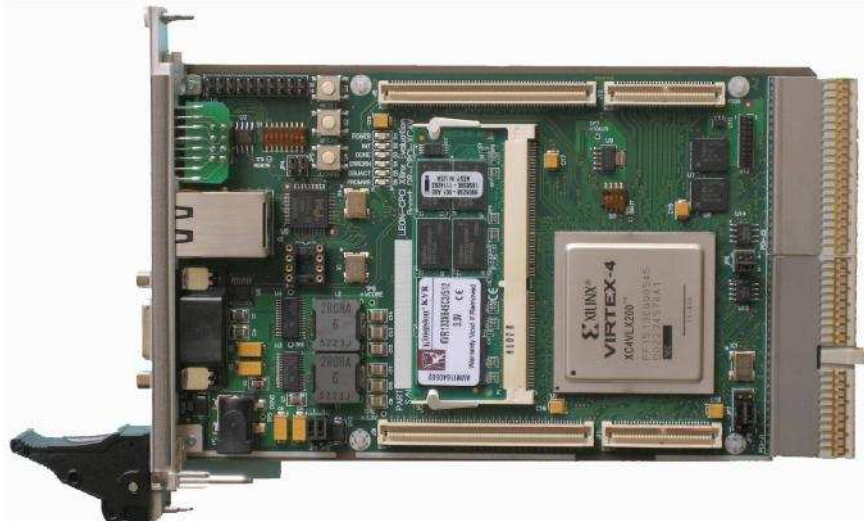


Figure 4. GR-CPCI-XC4VLX200 board

8 System Validation

8.1 Introduction

The system validation was processor driven and based on GR-CPCI-XC4V-LX200 board, GRMON debug monitor and LEON-3 software environment including eCos and RTEMS operating systems and BCC and RCC cross-compilers. The RTEMS and eCos multi-processing test suites have been prepared and downloaded to the board and run using GRMON debug monitor. Additional test including RTEMS network communication tests have also been performed.

8.2 System Validation Results

The hardware/software validation of the LEON3-FT-MP system performed by running eCos and RTEMS test suites was successful. All (applicable) test cases executed correctly which validated LEON3-FT multi-processing capabilities and multi-processing extensions of eCos and RTEMS operating systems in non-faulty environment.

Additional test have been performed to validate certain behavior which is not validate by eCos and RTEMS test suites. An RTEMS network communications test has been performed to validate MMU and cache snooping.

Fault-tolerant capabilities of LEON3-FT and GRFPU cores has been validated by running eCos and RTEMS test suits and additional test with GRMON's error injection feature enabled (RD10). This feature injects random errors in LEON3-FT and GRFPU on-chip blocks while CPU is running. GRMON's error injection model is very realistic and performed in real-time, effectively emulating an SEU testing. All test cases executed correctly with error injection enabled.

The results of LEON3-FT-MP validation are described in Reference Document 9, LEON3-FT-MP Validation Report.

9 Summary

A verification and validation platform has been developed by Gaisler Research in the Call-Off Order 3 under the ESA Contract 18533/04/NL/JD in the period from September 2005 to April 2006 as preparation for the development of the future ESA microprocessor (GINA). A 4-processor system based on LEON3-FT and GRFPU cores was developed during the activity. The system served as platform for verification and validation which focused on fault-tolerant and multi-processing capabilities of the LEON3-FT and GRFPU cores.

The fault-tolerant and multi-processing capabilities were first successfully verified by means of VHDL simulations. A FPGA board (GR-CPCI-XC4VLX200) was then developed to serve as platform for hardware and software validation. The full fault-tolerant and multiprocessor system was successfully implemented on that FPGA board on which the hardware and software validation was successfully performed by running the test suites for the eCos and RTEMS operating systems.

The work performed in that Call off Order 3 has demonstrated the capability of the LEON3-FT, the GRFPU and other additional IP cores from Gaisler Research to satisfy the needs of the future generation of ESA microprocessor.