SUMMARY REPORT

AT697 Validation

Call-off order 2

ESA CONTRACT :Design and Verification of Validation Techniques for On-Board Microprocessors, 18533/04/NL/JD,

1 INTRODUCTION

The objectives of the activity was to perform an independent validation of the AT697 by manufacturing a dedicated board to host the device and to execute appropriate validation programs in order to validate that first ATMEL implementation and to consolidate the design for the future flight implementation of the AT697 by ATMEL.
To support the validation of the AT697 ATMEL Microprocessor, a development board in Compact PCI format was developed, manufactured and tested, and software validation of the AT697 processor was performed using this board.

2 WORK PERFORMED WITHIN THE ACTIVITY

The following main tasks have been performed within the activity:

- Preparation of the AT697 validation board specification
- Preparation of a AT697 validation test plan
- Design and manufacturing of the AT697 validation boards
- Preparation of a board manual
- AT697 validation
- Preparation of a AT697 validation report, including recommendations for improvements
- Final presentation a ESTEC of the AT697 validation

Four fully equipped AT697 boards have been manufactured, whereof two has been delivered to the Agency and 2 boards has been kept at Pender Electronics Design and Gaisler Research. The 2 boards at Gaisler and Pender will be used to provide support in the frame of the call-off order 1 of the present contract.

3 VALIDATION ENVIRONMENT

The validation has been performed on the GR-CPCI-AT697 board developed specifically for this activity. The board has been designed for LEON2 software development, and incorporates all the necessary features and interfaces. The aim has been to provide a platform which enables the validation of correct functioning of AT697 device, by exercising its features and interfaces in its different configurations. The features of the GR-CPCI-AT697 development board are as follows:

- 3U format Compact PCI card
- ATMEL AT697 device in MCGA349 package (socketted)
- 1.8V and 3.3V power regulators
- On Board memory
- PROM 4 Mbyte FLASH (organized x8 bit)
- SRAM 1 Mword SRAM (organized 40 bit wide supporting EDAC)

- SODIMM socket for 64-bit SDRAM (organized 40 bit wide supporting EDAC)
- Memory expansion
- On Board oscillators
- 16-bit I/O port
- Debug Support Unit serial interface (RS232)
- 32-bit PCI interface, including arbiter (configurable as PCI System Controller or Peripheral)
- LAN91C111 10/100Mbit/s Ethernet interface
- JTAG

The GR-CPCI-AT697 development board has been used in stand-alone mode for the instruction execution validation and in a Compact PCI rack for the interface validation.

4 VALIDATION TESTS

The validation tests were run on the target hardware as defined in the AT697 Validation Test Plan. The validation tests consisted of four main categories:

- Functional tests divided in 5 categories
  - SPARC International SPARC V8 validation test suite
  - IEEE-Std-754 validation
  - RTEMS test suite
  - eCos basic test suite
  - uClinux operating system
- Performance measurement
  - Dhrystone
  - Stanford
  - GNC
  - Linpack
- Power consumption was measured under a number of frequencies and conditions.
- Hardware interfaces
  - PROM and SRAM interfaces
  - I/O port
  - The PCI interface
  - Serial ports and DSU interface
  - SDRAM interface

For more details see the AT697 Validation Test Plan.

5 SUMMARY OF THE VALIDATION RESULTS

The software validation showed that the AT697 is fully functional and executed all validation tests correctly.

In addition to the three previously known deficiencies, four new ones were found. These are associated with

- FPU exception handling
- Single-stepping in debug mode,
- Condition code generation in the divider
- Fault-injection in the register file.

They do not affect operation under normal conditions. The hardware validation showed that all interfaces except the SDRAM interface worked correctly at nominal (100 MHz) frequency. These include the SRAM, PCI and serial interfaces. The SDRAM interface operated correctly up to frequency of 90 MHz. At higher frequencies, correct operation could only be achieved with SDRAMs from certain manufacturers. The reason for the incorrect SDRAM operation at high frequencies has not been determined.

The performance was measured and in line with the expectations:

- Dhrystone 83,9 MIPS
- Stanford 121 ms
- GNC 1928 ms
- Linpack 5949 KFLOPS

For more details see the AT697 Validation Report

6 SCHEDULE AND DELIVERIES

There was a delay in the reception of the customer furnished of the AT697 prototypes, 2 AT697 prototypes were received in April and the 2 final prototypes in July. Thus the final presentation was postponed by one month and the delivery of the boards by 3 months.

Event/Delivery	**Actual Date**
Board Specification	2004-12-20
Specification Review	2004-12-15
Validation Test Plan	2005-04-15
Board Design and Test Plan Review	2005-05-01
Validation Test Report	2005-06-10
Board Manual	2005-06-29
AT697 Boards	2005-08-12
DSU Monitor	2005-08-12
Cross-compiler	2005-08-12
Newly developed validation software	2005-08-12
Validation test users guide	2005-08-12
Viewgraphs of final presentation	2005-06-14
Final Presentation	2005-06-14

7 DOCUMENTS ISSUED

Title	Reference/Revision	Date
Board Specification Review MoM	MIN-2004-0031	2004-12-15
GR-CPCI-AT697 Development Board - Board Specification	Rev 1-1	2004-12-20
Progress Report #1	Rep-2004-12-01, Issue 2	2005-01-13
Progress Report #2	Rep-2005-0201, Issue 2	2005-03-15
Progress Report #3	Rep-2005-0401, Issue 1	2005-04-15
AT697 Board Design and Test Plan Review	Min-2005-0021, rev 1	2005-05-04
AT697 Validation plan and report	GR-AT697-001, ver2	2005-05-04
AT697 Board Users manual	GR-CPCI-AT697, rev 1	2005-06-29
Board level test procedure and report	GR-CPCI-AT697, rev 1	2005-05-13
Board level test procedure and report	GR-CPCI-AT697, rev 1.2	2005-06-10
AT697 Validation Report	GR-AT697-002, ver 1.2	2005-06-10
Final presentation viewgraphs		2005-06-14

8 CONCLUSION

The validation of the AT697 has been carried out according to the validation plans. It was found that the device was fully functional, although four new design deficiencies were found. The power consumption was measured to ~ 0.7Watts@100 MHz, and in line with simulations. All hardware interfaces were found fully functional, with the exception of the SDRAM which only worked up to 96 MHz. The reason for this limit is not known and will be further analysed.

To assure optimal operation of the flight version of AT697, the following actions should be taken:

- All identified design deficiencies should be correct in the LEON2-FT VHDL model.
- The SDRAM operation should be analysed further to fully understand, and if possible circumvent, the limit in operational frequency.
- If compatible with the device timing, the LEON2-FT VHDL configuration should be changed to remove the extra ICC branch delay cycle in order to improve performance.