CIRCUMVENTING RADIATIONS EFFECTS BY LOGIC DESIGN

EXECUTIVE SUMMARY REPORT

EUROPEAN SPACE AGENCY CONTRACT REPORT

ESTEC Contract No. 3240/97/NL/FM

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ESA STUDY CONTRACT REPORT

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ABSTRACT:

The main objective of this R&D is to establish design methods to mitigate the Single Event Effects (SEE) in Very Large Scale Integration components (VLSI).

The first part of this study consists in describing the natural space radiation environment and its effects on electronic devices, by compiling literature and available data from different component manufacturers.

A second phase of the R&D examines different circumvention methods against the Single Event Upsets (SEU) effects for the main functions encountered in logic design. These methods can be either at logical design level or at physical design level.

Protection methods against Single Event Latchup (SEL) effects are discussed in a third part of this study. These methods are mainly applicable to Printed Circuit Board (PCB), but some of them can also be applied to VLSI chips.

The fourth step of this R&D consists in checking the efficiency of some protection methods against SEU. A specific test vehicle (including protected and unprotected structures) was developed and irradiated at the Cyclotron of Louvain-la-Neuve (CYCLONE) Heavy Ion Facility (HIF) in Belgium.

Finally, a design manual (also called “cookbook”) has been written. The objective of this manual is to give practical information and advice to designers confronted with SEE constraints.

The work described in this report was done under ESA contract. Responsibility for the contents resides in author or organization that prepared it.

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Executive Summary Report

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1 INTRODUCTION

1.1 SCOPE

This document is the executive summary of the work that has been carried out under ESTEC contract 3240/97/NL/FM "Circumventing Radiation Effects by logic design".

The Final Report (also called "Cookbook") is the compilation of all documents issued from WP100, 200, 300 and 400.

The objective of the R&D was to study radiations effects of SEU, to design and manufacture a test vehicle ASIC implementing different methods of circumventing radiation effects, and to test it under radiations to analyze the behavior and evaluate the different methods.

Several samples of the ASIC are available.

Keywords : SEE, SEU, circumvention, VLSI, ASIC, radiation

1.2 ABBREVIATIONS

AD	Applicable Document
ASIC	Application Specific Integrated Circuit
ASSP	Application Specific Standard Product
DED	Double Error Detection
DFF	D Flip-Flop
ESA	European Space Agency
ESTEC	European Space Research and Technology Center
FSM	Finite State Machine
IEEE	Institute of Electrical and Electronics Engineers
ID	Identification
I/O	Input/Output
PCB	Printed Circuit Board
SEC	Single Error Correction
SEE	Single Event Effect
SEL	Single Event Latch-up
SEU	Single Event Upset
SGL	Single level
SRAM	Static Random Access Memory
TMR	Triple Modular Redundancy
VHDL	Very high-speed integrated circuit Hardware Description Language
WWW	World Wide Web

2 OBJECTIVES AND CONSTRAINTS

The objectives of the study are the following:

- To make a review on the natural space radiation environment and its effects on electronic devices, particularly for microelectronics (WP100)
- To analyze different design methods to mitigate Single Event Effects (SEE) :
  - Logic design methods (WP210)
  - Analog and Semi-analog design methods (WP220)
- To define, to design and manufacture a test vehicle ASIC for evaluating and comparing some circumvention design methods against Single Event Effects (SEE). These design methods are either logic design methods (described in WP210) or cell design methods (described in WP220) (WP400)
- To submit this ASIC to radiations and test the effectiveness of the implemented methods (WP400)
- To compile the results of the study under a practical “cookbook” format. This report is written to help the designers when they shall use circumvention methods against SEE (WP500).

3 WORK ORGANIZATION

The overall frame contract is split into 3 parts:

- The first part contains WP100, WP200 (including WP210 and WP220) and WP300. It consists in reviewing the available knowledge concerning the natural space radiation environment and its effects on electronic devices, and the different methods to mitigate Single Event Effects (SEE). This study is based on ASTRIUM and IMEC experience in the concerned domains (radiation and logic design for ASTRIUM, cell and library design for IMEC), but also on a bibliographical study.
- The second part, which is the WP400, includes the definition, design, manufacturing and tests of the test vehicle ASIC. ASTRIUM and IMEC worked together in this part.
- The third part, which is the WP500, includes the writing of the design manual (ASTRIUM).

The following table summarizes the work organization in Work Packages for this R&D :

What ?	Who ?	When ?
WP100 "The Radiation Environment and Its Effects on Microelectronics"	ASTRIUM	Q4/97 Q2/98
WP210 "Design Methods to Mitigate Single Events Upset Effects"	ASTRIUM	Q1/98 Q2/98
WP220 "Analog and Semi-Analog Methods"	IMEC	Q1/98 Q2/98
WP300 "Design Methods to Protect Against SEL"	ASTRIUM	Q2/98
WP400 "Verification and Validation of Design Methods"		
Test vehicle definition and design (WP210 part)	ASTRIUM	Q3/98 Q4/98
Test vehicle definition and design (WP220 part)	IMEC	Q3/98 Q4/98
Test vehicle foundry (Europractice)	IMEC	Q4/98 Q1/99
Test vehicle irradiation and test	ASTRIUM	Q1/99 Q1/01
WP500 "Establishment of Design Manual"	ASTRIUM	Q1/99 Q2/99

4 RESULTS OF THE STUDY

4.1 SUMMARY OF THE STUDY

The first part of this study describes the natural space radiation environment and analyzes its effects on microelectronic devices. The study is mainly focused on Single Event Upset (SEU) and Single Event Latchup (SEL) phenomena induced in VLSI; total dose effects are briefly addressed. The results of this Work Package are written in a report.

The second part of this study describes the different methods used by designers to mitigate Single Event Effects (SEE). Two kinds of methods are detailed and assessed : logic design methods (including triplication, error detection and correction codes, parity …) and analog (or semi analog) methods (including cell design at transistor or layout level : drive strength hardening, capacitive hardening, resistive hardening, glitch-filtering, transistor hardening, combinatorial cells and clock buffers hardening). The results of this Work Package are written in 2 different reports (WP210 and WP220).

The third Work Package of this study concerns Single Event Latchup (SEL) hardening and mainly concerns board level design. Latchup occurrence mechanisms are analysed, some anti-latchup designs are described and a design analysis method is given : the choice of anti-latchup solutions depends on the Ilatchup/Iaverage ratio. The results of this Work Package are written in a report.

The fourth part of this study consists in assessing the efficiency of a selection of circumvention methods by defining a specific test vehicle ASIC. This test vehicle is split in two independent parts : an analog part designed by IMEC and a logic part designed by ASTRIUM. Both parts contain unhardened and hardened structures, such as clock buffers and combinatorial cells (for the analog part), or counters and fsms (for the logic part). This allows to make comparisons between protected an unprotected structures. This test vehicle uses a BiCMOS/SOI technology (DMILL) in order to be latchup free. Placement/Routing and foundry follow-up has been performed by IMEC. Heavy Ion tests at Louvain-la-Neuve and results analysis have been carried out by ASTRIUM; two test campaigns have been necessary to characterize the DMILL technology and the hardening methods. The results of this Work Package are summarized in five different reports (“Test Structure Definition”, “Heavy Ion SEU Characterization of Test Vehicle”, “Heavy Ion SEU Characterization of Test Vehicle Test Report”, “Heavy Ion SEU Characterization of Test Vehicle – Complementary Experiments Test Plan” and “Heavy Ion SEU Characterization of Test Vehicle – Complementary Test Report”)

The fifth and last Work Package of this R&D consists in writing a design manual on the basis of the previous Work Packages. This design manual is also called a “cookbook” because its main objective is to give practical advice and tricks to designers when they shall use circumvention methods against Single Event Effects.

4.2 DETAILED OF THE WORK PERFORMED

4.2.1 WP100: The Radiation Environment and Its Effects on Microelectronics

In this work package, the various components of the natural space radiation environment are presented in terms of particle composition and energy spectrum (solar flare, galactic cosmic ray and Van Allen belts). Particle flux interactions with geomagnetic field and material shielding are discussed, the effect of the orbit inclination and altitude are presented in order to define the typical energy spectrum at device level in a satellite.

The effects of ionizing particles (charge collection mechanism in a PN junction) induced by heavy ions and protons are discussed, and some orders of magnitude are given. Three types of effects are analyzed in detail : Single Event Upset (SEU) in storage elements, SEU in combinatorial logic and Single Event Latchup (SEL) on CMOS devices. The effects of SEU in digital systems can be classified in two categories :

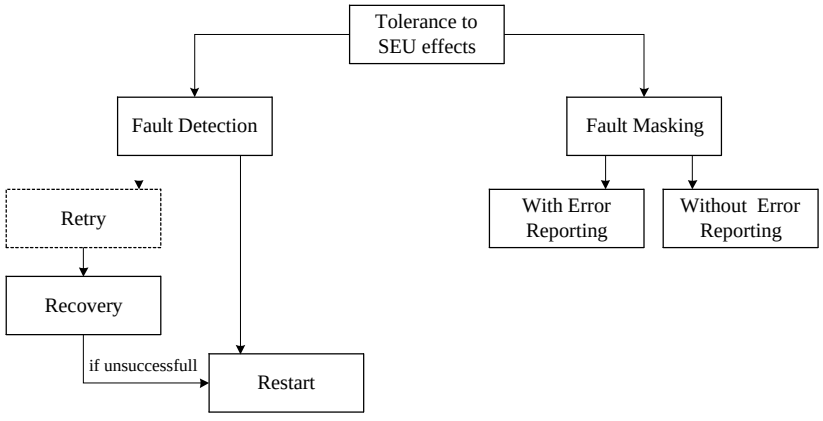
- Either a change of the state of a storage element (DFF, memory cell)
- Or a temporary glitch on combinatorial logic : this glitch can be transmitted by a combinatorial path to a clock input of a flip-flop and cause an unwanted memorization, or can be transmitted to a D input of a flip-flop and may corrupt the value of the data stored.

Finally, based on existing heavy ions/protons device characterization, in orbit failure rate predictions are performed and compared considering LEO, MEO and GEO orbits.

WP100 report has been accepted by ESA in May 1999 (e-mail from Peter SINANDER, dated May 18 1999).

4.2.2 WP210: Design methods to mitigate SEU effects

In this work package, different hardening methods at function design level are analyzed to prevent from errors in storage elements and to take into account glitches in combinatorial logic. The effects of SEU shall be evaluated : if they are not acceptable, fault detection or fault masking techniques shall be implemented, according to the following SEU tolerance strategy :



All the presented methods can be implemented by using VHDL. It is preferable that the protection part can be separated from the functional part, for better design validation, understanding, modification,

troubleshooting and documentation. Depending on the structure to protect, different methods can be applied :

- For finite state machines (fsm), fault detection can be achieved by parity, fault masking can be achieved by Triple Modular Redundancy (TMR) or error correction code
- For counters, fault detection is not commonly required and fault masking can be achieved by TMR or error correction code
- For data storage registers, redundancy techniques or TMR can be used.
- For resynchronization functions, TMR can be used.
- For memory, fault detection can be achieved by parity or error detection codes, fault masking can be achieved by error correction codes along with scrubbing
- For combinatorial logic, the limitations of SEU effects are limited : glitch filtering at the inputs of DFFs and use of the less sensitive cells from the library.

WP210 report has been accepted by ESA in May 1999 (e-mail from Peter SINANDER, dated May 18 1999).

4.2.3 WP220: Analog and Semi-Analog Design methods to mitigate SEU effects

In this work package, a practical method for SEU assessment is proposed. For a single cell, the error rate tends to be dominated by the most sensitive node. The hardening methods at cell design level use three different principles:

- by minimising the amount of charge Q_{coll} that can be collected by a sensitive node per event. This can only be accomplished by technological process enhancements:
    - Use of highly doped substrate: this limits the extension of the electrical field in the depletion region following an ion strike, and thus reduces the funneling effect and the charge collection.
    - Use of an epitaxial layer instead of bulk CMOS: this limits the charge collection distance to the thickness of the epitaxial layer.
    - Use of CMOS SOI/SOS instead of standard CMOS, with the drawback of lower density and higher processing costs
- by maximising the critical charge necessary to produce a logical upset; different design methods can be used independently of the technological process:
    - enhancement of stored information (capacitive hardening, drive strength hardening)
    - addition of redundancy to stored information (transistor hardening)
    - isolation from stored information (resistive hardening, capacitive hardening, glitch filtering)
- by minimising the area of the sensitive node. At layout level this can be accomplished by sharing as much as possible the sensitive areas of the same type (p/n) connected to the same node.

WP220 report has been accepted by ESA in May 1999 (e-mail from Peter SINANDER, dated May 18 1999).

4.2.4 WP300: Design methods to protect against SEL

In this work package, the triggering causes of Single Event Latchup (SEL) are described. When latchup free technologies (CMOS/SOS and CMOS/SOI) cannot be used, SEL triggering can be avoided by using specific latchup protection methods.

The anti-latchup function shall be located close to the circuit to protect on the PCB. It consists in detecting as fast as possible the latchup current and limiting it, or switching off the component to protect. The maximum average current of the circuit to protect shall be evaluated in worst case conditions of voltage, temperature, radiation and loads. The best suited latchup protection depends on this calculated maximum average current:

- For components with maximum average current ≤ 40 mA (latchup current at least 4 to 5 times greater than average current), a simple resistor for current limitation or a transistor used as a comparator (with a current probe made with a resistor or an inductor) shall be used.
- For components with maximum average current between 40 mA and 100 mA (latchup current greater than average current but not so far : ASICs or microprocessors, for example), a comparator with a current sensor made with a resistor or an inductor shall be used. The sensed current shall be filtered to get the average current of the sensitive component.
- For components with maximum average current ≥ 100 mA (latchup current similar or lower than average current), anti-latchup function will be hard to design and sensitive to other disturbances (common mode, overshoot on input signals). Latchup current cannot be directly measured with a resistor, an inductor is required for this. Latchup detection shall be enabled only when average current is less than latchup current.

WP300 report has been accepted by ESA in May 1999 (e-mail from Peter SINANDER, dated May 18 1999).

4.2.5 WP400: Design, Manufacturing and tests of the ASIC

In this Work Package, the design methods proposed in the previous work packages shall be evaluated by an ASIC demonstrator. Since it is not possible to implement all the described methods in the test vehicle, a selection of some of them has been made.

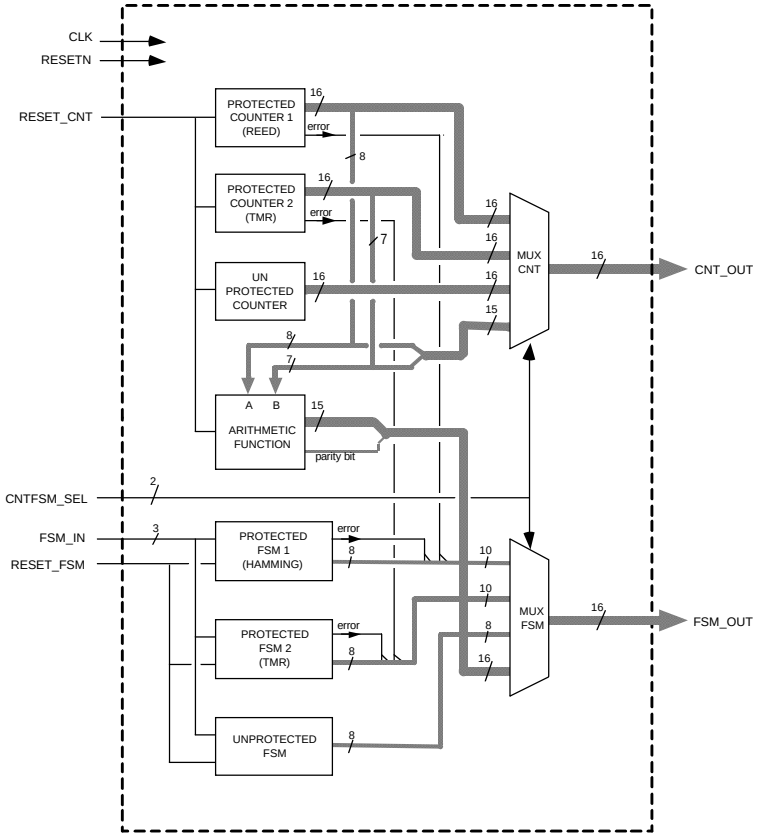
In accordance with the organization of the WP200, the test vehicle contains 3 parts:

- one test structure which implements mitigation methods by logic design, derived from WP210. This part has been defined and designed by ASTRIUM. Three different “real life” type and medium complexity functions have been designed :
  - one 16-bits counter, available in 3 different versions
    - unprotected,
    - with a Reed-Muller code protection,
    - with a Triple Modular Redundancy (TMR) protection
  - one 8-bits fsm, available in 3 different versions
    - unprotected,
    - with a Hamming SEC-DED code protection,

- with a Triple Modular Redundancy (TMR) protection

o one arithmetic function (combinatorial structure) with a parity bit

This test structure is detailed in the following figure :



The methodology adopted for designing this test structure uses top-down approach and VHDL coding, with a VHDL testbench, synthesis (SYNOPSYS) and simulation. Postlayout simulations have been run by ASTRIUM, after placement and routing made by IMEC.

- one test structure which implements analog and semi-analog mitigation methods, derived from WP220. This part has been defined and designed by IMEC. Two different circuits are tested:
  - clock buffers, available in 2 versions
    - hardened clock buffers
    - unhardened clock buffers
  - combinatorial logic, available in 4 versions
    - jiv1 inverters + FastFl flip-flops (flip-flops not hardened against glitches on their inputs))
    - jiv1 inverters + GfreeFl flip-flops (flip-flops hardened against glitches on their inputs by glitch filtering technique)
    - jiv1 inverters + semi-digital filter + FastFl flip-flops
    - nand2 cells, nor2 cells, EXOR tree + FastFl flip-flops

The test vehicle has the following characteristics :

- technology : DMILL (BiCMOS/SOI, 0,8 µm for NMOS and PMOS, 1,2 µm for bipolar NPN and PJFET, lateral and vertical SOI insulation, latchup free)
- area : 4,8 x 4,5 mm = 21,2 mm^2
- package : JLCC84
- power supply : 5V
- foundry : EuroPractice (start in October 1998, samples delivered in January 1999)

The SEU tolerance of the test vehicle has been evaluated in heavy ion accelerator test facility at Louvain-la-Neuve (Belgium). Two different ions have been used for this : Xe (LET=56 MeV/mg/cm^2) and Kr (LET=34 MeV/mg/cm^2). The test campaigns held on March 1999 and February 2001. The results are the followings:

- For the test structure with logic design hardening methods: the best protection against SEE is achieved by using TMR
- For the test structure with analog and semi-analog design hardening methods:
  - the hardened clock buffer is better than the unhardened clock buffer,
  - simple inverters are SEU sensitive. A good precaution consists in protecting the DFF inputs by using glitch-hardened flip-flops, or semi-digital filters
  - more complex combinatorial cells (nand2, nor2 and exor) are not SEU sensitive

4.2.6 WP500: Writing of the Design manual

The design manual contains the results of the works of WP100, 200 (WP210 and WP220), 300 and 400. A methodology for design hardening is presented, and a compilation of all interesting results of the R&D will provide some help to electronic designers confronted with SEE constraints.

This document is useful for electronic designers (in the fields of ASIC, FPGA and board design), but project managers looking for information in the domain of SEU and hardening can also read it.

4.3 SUMMARY OF EXPERIENCE

The study has shown that the application bit error rate shall be accurately evaluated in order to choose the best solution for hardening design against SEE. The best solution is defined by balancing between ASIC technologies sensitivity and hardening design solutions. There are many design solutions to cope with SEE constraints, which shall be selected with respect to the implementation complexity and the required performances.

The study also gave ASTRIUM the opportunity to access to a new type of foundry interface by using EUROPRACTICE multi-projects foundry service. This solution is very attractive for its moderate cost and can be efficiently used for prototyping. In addition, it allows access to a large number of ASIC technologies. This solution can be chosen in place of FPGA.

The last and important experience was acquired during the test campaign. The test setup and the tests were difficult to work, due to the medium complexity of the test vehicle and the low sensitivity of the

DMILL technology. So, if these circumventing techniques are used in further complex or very complex ASIC, a great attention shall be put in the ASIC testability and in the test set-up to be able to qualify the design under SEE environment.

5 CONCLUSION

A lot of circumventing design methods against SEE are available when considering ASIC or FPGA design, for a given technology and library. Therefore, it is necessary to identify precisely the functions to protect, according to an acceptable bit error rate for a given mission. The study performed in the frame of the “Circumventing Radiation Effects by Logic Design” R&D gives the designer some help to choose the adequate hardening method. To know if a data shall be protected or not, and how to protect it, it is necessary to answer to these questions:

- How much time is the data available in a storage cell (DFF, latch or memory cell) ? Depending on this duration (a corresponding bit error rate can be calculated), the data shall be protected or not
- From a system point of view, is this data essential or not ? If not, simple error detection is sufficient (parity, error detecting codes). If yes, TMR or error correcting codes shall be used.
- What kind of structure shall be protected ? For counters, fsms, resynchronisation DFFs and small registers: TMR is well adapted. For memory and registers : error correcting codes shall be used, eventually with scrubbing.

Logic design methods for circumventing Single Event Effects shall be used along with an hardened library if it is available. The exclusive use of an hardened library (without any logic design hardening method) shall be avoided, since the efficiency seems to be low. All the protection methods result from a compromise between hardening efficiency, complexity (i.e. area) and eventually a performance loss.

In conclusion, the use of SEU sensitive technologies seem to be envisaged when circumventing methods are used. However, the performance (bit error rate) and the effort for this shall be compared with the use of an hardened technology.