Executive Summary

Manufacture and Validation of LEON4FT Multiprocessor Prototype Device

Contract: 18533/04/NL/JD

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1 INTRODUCTION

1.1 Scope of the Document

This document constitutes the Executive Summary Report for the Next Generation Microprocessor (NGMP) functional prototype (FP, NGFP) development.

The NGMP has been defined as part of an activity initiated by the European Space Agency under ESTEC contract 22279/09/NL/JK. The NGMP functional prototype was developed under ESTEC contract 18533/04/NL/JD.

The work has been performed by Aeroflex Gaisler AB, Göteborg, Sweden.

1.2 Reference Documents

[RD1] “18533/04/NL/JD, COO1: Maintenance and Support of LEON2FT”, http://microelectronics.esa.int/finalreport/SummaryReport-18533-COO1-2006-06-08.pdf

[RD2] “18533/04/NL/JD, COO2: Validation of AT697E”, http://microelectronics.esa.int/finalreport/SummaryReport-18533-COO2-2005-10-07.pdf

[RD3] “18533/04/NL/JD, COO3: Development of LEON3-FT-MP (GINA)”, http://microelectronics.esa.int/finalreport/SummaryReport-18533-COO3-2006-05-15.pdf

[RD4] “18533/04/NL/JD, COO4: Maintenance and Support of LEON2FT, namely during AT697F development”, http://microelectronics.esa.int/finalreport/SummaryReport-18533-COO4-2007-04-11.pdf

[RD5] "Quad Core LEON4 SPARC V8 Processor, Data Sheet and User's Manual", Aeroflex Gaisler, LEON4-N2X-DS 1.8, May 2013

[RD6] “Validation Report, Manufacture and Validation of LEON4FT Multiprocessor Prototype Device”, Aeroflex Gaisler, NGFP-VALR-0010-i1r1, May 2013

[RD7] “Technical Note on NGMP Verification”, Aeroflex Gaisler, NGMP-EVAL-0013-i1r1, December 2010

[RD8] “The ESA Next Generation Microprocessor (NGMP)”, ESA Microelectronics section, http://microelectronics.esa.int/ngmp/

[RD9] “GR-CPCI-LEON4-N2X, Quad-Core LEON4 Next Generation Microprocessor Evaluation Board”, Aeroflex Gaisler, http://www.gaisler.com/gr-cpci-leon4-n2x

1.3 Acronyms

ASIC	Application Specific Integrated Circuit
COO	Call-Off-Order
DDR	Double Data Rate
DSM	Deep-Sub-Micron ASIC technology
DSU	Debug Support Unit
EDAC	Error Detection And Correction
FIFO	First-In-First-Out, refers to buffer type
FLOPS	Floating Point Operations Per Second
FPU	Floating Point Unit
GINA	Giga Instruction New Architecture
GRLIB	Aeroflex Gaisler's IP core Library
HSSL	High-Speed Serial Link
I/O	Input/Output
IP	Intellectual Property
MAC	Media Access Controller, when referring to, for instance, an Ethernet MAC
Mb, Mbit	Megabit, 10^6 bits
MB	Megabyte, 10^6 bytes
MiB	Mebibyte, 2^{20} bytes, unit defined in IEEE 1541-2002
MIPS	Million of Instructions Per Second
NGMP	Next Generation Multi-Purpose microProcessor
OS	Operating System
PCI	Peripheral Component Interconnect
RAM	Random Access Memory
RMAP	Remote Memory Access Protocol
RS232	Recommended Standard 232, standard for serial data signals
RTL	Register Transfer Level
SDRAM	Synchronous Dynamic Random Access Memory
SEE	Single Event Effects
SEL/SEU/SET	Single Event Latchup/Upset/Transient
SMP	Symmetric Multi-Processing
SPARC	Scalable Processor ARChitecture
SOC, SoC	System-On-a-Chip
SoW	Statement of Work
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

2 BACKGROUND

During the past years Aeroflex Gaisler has been one of the main actors in the development of the latest generation of the SPARC architecture-based ESA microprocessor family that is called LEON and in particular the fault tolerant version for space use.

The Next Generation Microprocessor (NGMP) has been developed under ESTEC contract 22279/09/NL/JK. The activity has defined a quad-processor architecture that provides a significant performance increase compared to earlier generations of European space processors. During the course of contract 22279/09/NL/JK, several downsized versions of the NGMP architecture have been developed in the form of FPGA prototypes. These FPGA prototypes are limited in that no single FPGA prototype provides all the communication and memory interfaces specified for the NGMP. The maximum operating frequency of the FPGA prototypes is also considerably lower than the target frequency of the final NGMP devices.

Under the frame contract 18533/04/NL/JD with Aeroflex Gaisler, the support and validation of various ESA microprocessor developments has been ensured during the past 8 years. The frame contract comprised the following call-off-orders (COO):

- *COO1 [RD1]:* Maintenance and Support of LEON2FT, 11/2004 – 05/2006
- *COO2 [RD2]:* Validation of AT697E, completed in Oct. 2005
- *COO3 [RD3]:* Development of LEON3-FT-MP (GINA), completed in May 2006
- *COO4 [RD4]:* Maintenance and Support of LEON2FT 06/2006 – 03/2007, namely during AT697F development
- *COO5 (present activity):* Development of Functional Prototypes (NGFP) of the ESA Next Generation Microprocessor (NGMP), completed in May 2013

3 OVERVIEW OF THE ACTIVITY

In the present activity the processor configuration previously designed and validated in ESA Contract 22279/09/NL/JK was to be implemented and validated on a deep sub-micron ASIC technology.

The objectives of this activity were to:

- consolidate the previous prototyping on hardware at the target speed and allow real performance evaluation
- make an early identification and investigation of potential problems related to the design and to implementation of the architecture on a deep sub-micron technology in order to prepare the development of the future processor device
- provide to the European space community the access to an evaluation board to allow users to assess the suitability of the offered at speed performances and the offered functions for their future applications and give feedback to consolidate the future ESA processor specification.

The following companies were involved in the development of the functional prototype devices and validation boards:

- Aeroflex Gaisler – Aeroflex Gaisler (Sweden) was the prime contractor and performed the port of the NGMP VHDL design to the target technology, verification and validation.
- eASIC Corporation – The manufacturing of the device was eASIC (US, Romania) as an external service.
    - eASIC Corporation have headquarters in USA and the design centre that handled the functional prototype development is located in Romania.
    - The fabrication, for this chip, was done by GlobalFoundries (Chartered Semiconductor). Assembly, packaging and tests were also services provided via eASIC.
- The validation board development, manufacturing and test are performed by Pender Electronic Design (Switzerland) as an external service

4 WORK PERFORMED AND MAIN RESULTS

The architectural (VHDL) design of the NGMP, developed in a separate TRP activity, was ported to a 45 nm structured ASIC technology (eASIC Nextreme2). The target technology placed constraints on the parts of the NGMP architecture that could be implemented:

- The selected target technology did not allow to implement the high-speed serial links that are part of the NGMP specification, and envisioned to be used to support SpaceFibre.
- Lack of multi-standard IOs prevented the two main memory interfaces (DDR2 SDRAM and SDRAM) from sharing pins.
- The selected target technology is a commercial technology and the implemented design does not have all the fault-tolerance features specified for the NGMP.

Many of the issues encountered during the design and implementation work were specific to the structured target technology but insights that are applicable regardless of implementation technology selected for future NGMP devices were also obtained.

Following the design work done by Aeroflex Gaisler, eASIC Corporation performed the layout work and NGMP functional prototypes were manufactured. The worst-case sign-off frequency was 150 MHz, and therefore the frequency specified in the data sheet is 150 MHz. Nevertheless, the chip was found to work without problems at 200 MHz [RD6].

An evaluation and validation board was developed and manufactured and validation tests performed.

A few bugs were found in the implemented design, these have been corrected in the RTL code [RD5] [RD6]. In all other aspects the implemented architecture is fully representative of the NGMP architecture:

- Existing FPGA prototyping and simulation are in line with the results obtained from devices containing the full system. The NGMP functional prototype delivers four times the performance of the current FPGA prototypes (that have a 50 MHz operating frequency). Future ASIC implementations of the NGMP design are expected to achieve an even higher operating frequency and deliver higher performance than the functional prototype.
- Performance, apart from the bugs, was found to confirm the forecast from the FPGA prototypes, and the overall performance is a multiple of present generation AT697 and GR712 [RD6][RD7].

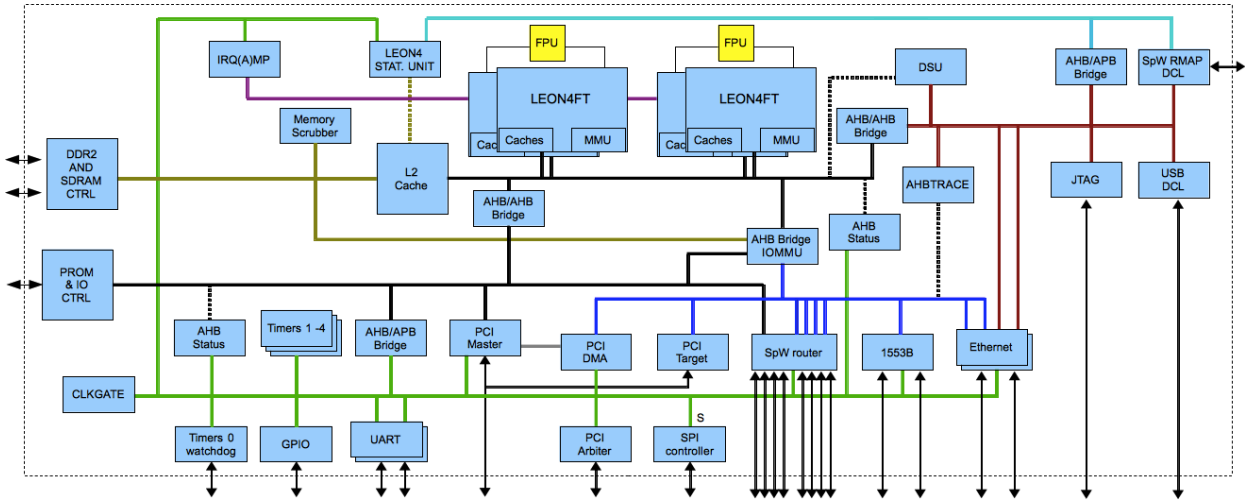

Illustration 1: Block diagram of implemented architecture

5 DELIVERABLES

The following deliverables have been produced within this contract:

- Development Plan (TN-2)
- Feasibility Analysis (TN-3)
- Architecture Verification and Optimization Report (TN-4)
- Netlist Generation and Verification Report (TN-5)
- Layout Generation Report (TN-6)
- Layout Verification Report (TN-7)
- Data sheet (TN-8)
- Validation Board User's Manual (TN-9)
- Validation Report (TN-10)
- Executive Summary Report (TN-11)
- Validation board with MDM9 connectors (2 pieces) (HW-1)
- NGMP eASIC devices (3 pieces) (HW-2)
- LEON4 GRFPU Binding Evaluation Report (added deliverable)
- Clocking and Reset Scheme Block Diagram (added deliverable)
- Configuration Comparison Report (between NGMP and functional prototype, added deliverable)
- Board product sheet (added deliverable)
- NGMP/NGFP Differences (document for end users, added deliverable)
- GR-CPCI-LEON4-N2X Quick-Start Guide (added deliverable)
- Device Documentation Package (for board designers, added deliverable)

For each update of the functional prototype data sheet, all applicable changes, updates and corrections have also been transferred to the main NGMP data sheet and new versions of the NGMP data sheet have been delivered to ESA.

6 CONCLUSIONS

The outcomes of this activity provides the European space community with a platform to evaluate the Next Generation Microprocessor architecture. The evaluation board (GR-CPCI-LEON4-N2X) is commercially available to prospective users of the NGMP.

The implementation work done for the functional prototype has provided insights that will be of value in future implementations of the NGMP. During the development of the functional prototype there were improvements made to the architecture. These have been validated and have been added to the NGMP design RTL and data sheet.

The development of a validation board and the validation work done has also provided insights and the collected feedback from first users is expected to be incorporated as improvements to the NGMP specification.

Progress for the NGMP development is reported at the ESA NGMP website [RD8]. The validation board product page on Aeroflex Gaisler's website is available at [RD9].