

Page: 1 of 14

Project ACN - HIFAS

Executive Summary

Document Number ACNTN9 Author Mikael Krus

Revision B

Reviewed by: Anders Emrich Date 2009-12-08

Date 2009-12-08



Change Record

Revision	Date	Paragraph	Comment
А	2009-11-20	All	Initial release
В	2009-12-08	2	New section
		All	Minor changes in all
			sections



Table of Contents

1	Docu	ments and abbreviations	4		
	1.1.1	Applicable Documents	4		
	1.1.2	Reference Documents	4		
	1.1.3	Abbreviations	4		
2 Intr	Intro	oduction5			
	2.1	Spectrometers in radiometer instruments	5		
	2.2	Objectives	5		
	2.3	Basic concept	6		
3	HIFA	AS Spectrometer chip	7		
	3.1	Overview	7		
	3.2	Correlator quantiser – Bipolar design	8		
	3.3	Correlator core - CMOS design	8		
	3.4	Redesign of chip	8		
4	Radia	Radiation tests			
	4.1	Single event tests	9		
	4.1.1	Cross-section calculations	9		
	4.2	Total dose tests	9		
	4.2.1	Test results	9		
	4.2.2	Performance test	10		
5	Perfo	ormance tests	11		
	5.1	Analog Bandwidth Test	11		
	5.2	Total Power Range	11		
	5.3	Maximum Speed and Power Consumption Test	12		
	5.4	Spectrometer Measurements	12		
	5.5	Test Results Summary	13		
6	Sum	mary	14		



1 Documents and abbreviations

1.1.1 Applicable Documents

The following documents contain requirements applicable to the activity:

1.1.2 Reference Documents

The following documents can be consulted by the Contractor as they contain relevant information:

1.1.3 Abbreviations

ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
CW	Carrier Wave
HIFAS	Highly Integrated Full-custom Autocorrelation Spectrometer
SEU/SEE	Single Event Upset/Single Event Effects
SRR	(Signal – Reference) / Reference
TBC	To Be Confirmed



2 Introduction

2.1 Spectrometers in radiometer instruments

In many applications when a signal is analysed with high spectral resolution, heterodyne receivers are employed. In signal to noise limited applications, such as limb sounding aeronomy, the system is often divided into a low noise "Front-End" and a spectrometer type "Back-End". Even if the noise level of the spectrometer is uncritical, it must be very efficient, i.e. a commercial swept filter spectral analyser, that process only one "channel" at a time, will not do.

The special environment of a satellite, or space probe, will add additional constraining requirements on the design of a "Back-End" spectrometer, such as low power consumption, size and weight. The quality aspect is also of outmost importance.

In its most general form, a spectrometer can be considered to be a device that receives an input signal, which is variable in time, and estimates its power spectral density. The estimate is given sampled at N equidistant frequency points, or channels, f₀,..., f_{N-1}, separated in frequency by B/(N-1), where B is the bandwidth of the signal. Critical parameters are the total bandwidth, the transfer function of each channel, and the stability of the spectrometer. Perhaps most important is that the spectrometer should add as little noise as possible to the overall system noise budget.

2.2 Objectives

Several prototype chips for autocorrelation spectrometers have been developed over the last decade by Omnisys. The latest chipset comprises 128 and 1024 channel digital autocorrelator chips in 0.25 um STM CMOS technology (HCMOS7) and a 1.5 bit ADC (Analog Digital Convertor, quantiser) chip in 0.6 um Ericsson bipolar technology (P71). The chipset allows a maximum processed bandwidth of 1.5 GHz.

Based on these results, a single chip autocorrelations spectrometer has been designed and is described in this report. It incorporates 1024 effective channels and support two sampling modes, real and complex. It provides potential for up to 8 GHz of processed bandwidth with 4 GHz as minimum requirement.

The chip design is 5.2x6 mm in size and is implemented in the IBM 7WL BiCMOS 0.18 m SiGe technology and will dissipate between 0.5-3 W depending on clock rate and configuration.

The main objectives are:

- Following-up previous autocorrelator chipsets with separate ADC and correlator chips: to integrate ADC and correlators into a single chip on 180 nm BiCMOS technology.
- Minimum requirements: Bandwidth 4 GHz, 512 channels, power consumption < 0.5mW/channel/GHz + 1000 mW for the ADC
- Design goal: Bandwidth 8 GHz, 1024 channels, power consumption 0.3 mW/channel/GHz + 300 mW for the ADC
- Prepare qualification by assembling a Process Identification Document with relevant information about the manufacturing and packaging flow
- Functional and performance test
- Radiation evaluation (total dose and single events)



Page: 6 of 14

2.3 Basic concept

The autocorrelation spectrometer is based on Wiener-Khintchines theorem;

 $S(\omega) = \int R(\tau) e^{j\omega t} d\tau$

Where $S(\omega)$ = power spectrum and $R(\tau)$ = autocorrelation function

For the (digital) autocorrelation function estimation, the digitized signal is delayed in a number of discrete steps, and the delayed samples are multiplied with an un-delayed version of the same signal. The products from the multiplications are then integrated and accumulated separately for each of the delay stages.

In the digital autocorrelator, we need to consider that the data is discrete in time and discrete in amplitude (and very coarse).

As long as we sample with a rate twice the input bandwidth or higher, the sampled values contain all the spectral information. That the data is sampled with very coarse accuracy, usually with one or two bit precision, has two implications. The major is that the signal to noise ratio is degraded, but for a 1.5-bit autocorrelator, the degraded efficiency is still better than 90%. The other implication is that the correlation estimate is biased, but this is easily taken care by an quantisation correction performed in the post processing of the output data.

The effective sensitivity of the complete instrument for radiometer application is critical, but also the stability, as differential measurements is needed for accurate observations. The system noise can be in the order > 1000 K and detailed features of a10 mK signal is observed and analysed. A total amplification of 80 dB can be needed between the sky and the detector in the system. Switched measurements are used to remove drifts in gain. Common switch rates are between 0.1-10 Hz.

HIFAS is a full-custom chip design, using asynchronous design techniques, semi-static logic and ripple counters. These techniques allow a performance/power ratio much better than standard-cell (semicustom) ASIC design.



Page: 7 of 14

3 HIFAS Spectrometer chip

3.1 Overview

The spectrometer chip consists of two main blocks, the digitiser/quantiser and the correlator core. The first block is based on bipolar transistors and the correlator core on CMOS.

The bipolar ADC (digitiser/quantiser) provides all signals to the correlator data path that is the heart of the correlator. In this data path, delayed and undelayed correlator signals are pipelined in parallel to the data clock. After the bipolar to CMOS interface, the signals are processed in the monitor blocks. The monitors count the samples at each ADC output, separately per quantisation level. This binning is used to calibrate the ADC reference levels, as well as in the post processing of the autocorrelation data.



Figure 3.1 Spectrometer chip

To increase the overall bandwidth at a given clock frequency, time de-multiplexing is used. The design allows for complex operation with a time multiplexing of 4 as well as real sampling with a time multiplexing of 8. The modes differ in real time by having the sampler clocks operating in phase for the complex mode and 180 degrees out of phase for the real mode.

Both modes utilise two inputs and two samplers. In the Real mode, both inputs are fed from the same signal, while for the Complex mode, the input signals are provided from an IQ down converter.

As an example, Figure 3.2 shows how complex auto correlation with time demultiplex factor of 2 can be implemented. In this project, a complex time demultiplexing factor of 4 is used. Note that only the sampling unit differs from real correlation example.



Page: 8 of 14



Figure 3.2 TM2 complex auto correlation path example

3.2 Correlator quantiser – Bipolar design

The complex quantiser is a dual channel 1.5-bit (three level) analog-to-digital converter.

There are two independent data signal chains, I and Q, with a time de-multiplexing factor of two. Each of these data chains has one signal input and two reference inputs.

The two operation modes (complex and real) are supported by a 0/180 degree phase shift control on one of the samplers, matched by a 0/180 degree digital delay. Both the complex and real operation is supported by the same correlator core.

3.3 Correlator core - CMOS design

In the correlator core, as shown in Figure 2.1., the (high speed) data path is routed in meander form across the chip. The data path consists of delayed and undelayed data to be correlated and the data path clock pipelined in parallel.

There are two active functions in the data path, resynchronisation blocks and delay blocks. The delay blocks provide the data delay function that is a part of the autocorrelation process and the resynchronisation provides the drive function of the data and clock lines as well as the synchronisation between the lines.

The correlators (multipliers and accumulators) are arranged to the left and right of the data path. The multipliers give a pulse rate output and simple asynchronous prescalers are used to reduce the data rate before the results are accumulated in semi static ripple counters.

3.4 Redesign of chip

The first version of the HIFAS chip contained a design bug. The ADC outputs were routed to the correlator core inputs in the wrong order. A bug fix was designed and manufactured as a metal fix. Test results show full functionality, and performance exceeds the specification.



4 Radiation tests

As the HIFAS chip has been produced in a commercial process, we have little knowledge on the radiation sensitivity of the device. One of the major effects of radiation on digital circuits is single-event upsets, where heavy particle radiation into the chip can cause bit flips in the circuits.

ESA has a radiation test facility called CASE, which uses a radioactive Californium source to provide the radiation. While Californium is not representative of the radiation the chip would get in a space environment, this gives an order-of-magnitude figure of the SEU sensitivity of the device.

Sahlgrenska (University Hospital in Gothenburg) has a CO-60 source used for total dose radiation. With a dose rate of 500 Rad/h, the HIFAS chip has undergone a total dose radiation of 30kRad over a 3-day test campaign.

4.1 Single event tests

4.1.1 Cross-section calculations

A total of 1056 SEUs occurred over a integration time period of 65863 seconds. This gives an error rate of 1056/65863 = 0.016 errors/s = 0.962 errors/min

The distance between the source and the chip was estimated to 7 mm. This gives an ion flux of approximately 3000 ions / cm^2 min. The measured SEU cross section thus becomes 0.962/3000 = 0.00032 errors cm^2 / ions.

We estimate the number of flip flops covered by the test as $2048 \times 2 \times (31-3) = 114688$ flip-flops.

The measured SEU cross-section per flip-flop therefore becomes: $0.00032/114688 = 2.8 \times 10^{-9}$ errors cm² / ff ions

An analysis shows that these SEU, if occurring on the MSBs of the correlation value, can be detected and corrected easily in post-processing, and if occurring on the LSBs, it will be noticed as a small additional noise.

4.2 Total dose tests

The HIFAS correlator was set up to run in complex mode with maximum number of lags (4x512) enabled. It was set to constantly correlate the input signal of 100 MHz with a 1 GHz clock during the irradiation period but no readout was performed.

Three times during the test period, the radiation source was paused for 5 minutes or so and a test measurement with an integration time of one second was performed to see that the correlator was still working as expected.

During the irradiation periods both the CMOS and Bipolar core voltages and currents were recorded, as well as the readout-buffers.

4.2.1 Test results

Figure 4.1 shows how current and voltage variations versus irradiated dose. No variations besides normal could be observed.





Figure 4.1 Current and voltage variations vs irradiated dose

4.2.2 Performance test

A performance measurement, maximum speed, was performed in our lab after the total dose radiation campaign. This test investigates the maximum possible clock frequency when running with a CW signal.

4.2.2.1 Test Results

The maximum clock frequency is 6100MHz which is the same as before radiation.



5 Performance tests

A number of performance tests have been done. The sections below describe some of them to show the HIFAS chip typical performance.

5.1 Analog Bandwidth Test

To meet the specified minimum requirement of analysing 4 GHz bandwidth, a RF bandwidth of at least 2 GHz is needed when the ASIC is operated in complex mode and 4 GHz is needed to meet the objective of 8 GHz bandwidth coverage. In Figure 5.1, the measured bandwidth is shown with a 3 dB bandwidth of >5 GHz with an associated complex bandwidth of 10 GHz. When allowing a loss of slightly larger than 4 dB, the analog bandwidth is 8 GHz with an associated complex bandwidth of 16 GHz.



Figure 5.1 Analog bandwidth test results after subtracting (in dB) the source power

5.2 Total Power Range

A noise source is measured with the correlator and the noise source power is then varied around this point using a step attenuator, while keeping the quantization levels constant. The quantization thresholds are calibrated with the attenuator at mid level (5 dB). From the monitor values, the input power can be estimated. The source and step attenuator is also characterized using a power meter. The two results can be compared.



Figure 5.2 Total power dynamic range test results



Over the full 10 dB range, we have a difference between readout and attenuation value of ± 0.3 dB. However, most of this error is due to the attenuator, as we can see the same trend in the power meter characterization curve. If we account for this, these results show an estimation accuracy of 0.05 dB over the entire range, which is close to the power meter's accuracy.

5.3 Maximum Speed and Power Consumption Test

With 1.8 V CMOS voltage, we can run the chip to 5 GHz with full resolution and up to 6 GHz with reduced resolution. With 2.1 V CMOS voltage, we can run the chip up to 8 GHz with 25% resolution. It might be possible to get even more performance by running at 2.3 V, but this is outside of the specified voltage range.

With 4 GHz clock and full resolution we consume about 1.6 W in total. Of that, 1.1 W is consumed by the correlator part giving a specific power consumption of 0.27 mW/GHz/channel. Thus, we meet the goal of 0.3 set for the correlator part.

The table below shows total power consumption with CW input:

Sample clock	Power consumption when running with CW input, total (mW)				
frequency	256 ch (1 bank)	512 ch (2 banks)	768ch (2 banks)	1024ch (4 banks)	
1 GHz	414	498	589	664	
2 GHz	519	682	841	986	
3 GHz	649	932	1206	1438	
4 GHz	688	980	1266	1522	
5 GHz	863	1324	1761	2135	
6 GHz	983	1489	2702	3250	
7 GHz	1232	1867	2915	3525	
8 GHz	1288	2382			
9 GHz	1791				

Legend: CMOS = 1.8 V CMOS = 2.1 V CMOS = 2.3 V Not available

5.4 Spectrometer Measurements

Figure 5.3 shows to the left, a SRR plot with a CW signal embedded in noise and to the right a channel shape plot.







Figure 5.4 shows to the left, a SRR linearity measurement over a 40dB range and to the right a sideband rejection and signal-to-spur peak ratio.



Figure 5.4 Left: SRR linearity, Right: Sideband rejection and signal-to-spur peak ratio

5.5 Test Results Summary

The maximum clock frequency is 5 GHz with 1024 channels and nominal (1.8 V), 6 GHz are reached with increased supply voltage (2.1 V), and 8 GHz are possible at reduced resolution (256/512 channels). This is within spec (4 GHz) but not as good as expected from simulations.

In complex mode, the overall bandwidth is equal to the clock frequency. In real mode however, the overall bandwidth is limited to 5 GHz in the analog path, but we have measurements suggesting that this is limited by the impedance matching of the test board. With this assumption, it should be possible to achieve 6-7 GHz analog IF bandwidth on the spectrometer module.

The CMOS part performs with full resolution up to 6 GHz sample clock (i.e. 1.5 GHz CMOS clock). With reduced number of correlator channels, the correlator can be run with up to 8 GHz clock speed. This is within spec (4 GHz) but not as good as expected from simulations.

The sampler shows very good linearity in the total power sense, measured over a 10 dB range.

Spectrometer measurements with CW signal embedded in noise have been performed with 4 GHz bandwidth in complex and real modes. We have measured a signal peak to spurious peak ratio of 20 dB, and spectrum linearity over a 40 dB range. The results were limited by the test setup due to reverse leakage of the sample clock and too low clock power.



6 Summary

An autocorrelation ASIC (HIFAS) with integrated ADC function has been realised in a 0.18 um BiCMOS process. It is capable of operating with bandwidths between 100-8000 MHz and it supports two modes of operation with either complex or real sampling. The number of resolved frequency channels can be set to 256, 512, 768 and 1024, with less power consumption for the lower resolution modes.

The HIFAS ASIC pass all performance tests, including dynamic range, linearity, channel shape and other criteria. Performance and power consumption largely exceed the minimum specification set at the beginning of the activity.

The HIFAS ASIC also pass the radiation tests, single event and total dose. The HIFAS chip was not visibly affected by the 30kRad radiation dose from the cobalt-60 source. Single event rate is low, if upsets occur, they can either be detected and corrected in post-processing, or they generate a negligible noise.

The HIFAS ASIC will be used in the STEAMR instrument in the ESA Premier mission (TBC) with 14 receiver channels. Two devices will be used for each receiver channel, supporting 12 GHz of processed bandwidth. The total processed spectrometer bandwidth will be two orders of magnitude wider than for the HIFI instrument on Herschel.

The HIFAS ASIC is also considered for the 56 GHz channel for post EPS radiometer instruments, under an ESA pre development.

Omnisys will use the HIFAS ASIC as back-end for 118 and 183 GHz receiver development, also intended for post EPS instruments.

There are sufficient stock of HIFAS chips to allow the use in other missions. HIFAS will be offered packaged into a spectrometer module, including power conversion, clock generator and read-out electronics.

Further information and a preliminary data-sheet of the spectrometer module can be obtained from Omnisys (www.omnisys.se).