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1 INTRODUCTION

This document describes in detail the different developments (Bread-Boards) of the MSREM contract and the corresponding change proposal.

2 CONCLUSION

The performed activities give a more clear overview about the design activities for a new radiation monitor. Never less the component availability and improvements of component to the time of a real developing contract has been analysed to this time.

Due to the fact of having no science institute in the program a general statement of the design acceptance could not be made. The activities will proceed in the CSAG “Further Radiation Monitor Strategy “ with a clear development contract for a new low mass monitor.

Detail conclusion of the individual Bread Boards:

Particle Detector Module Design:

The design shows the benefit as proposed by miniaturisation of the dimension. The tantalum could be reduced from original 25 mm diameter to 18 mm. The major mass reduction could be made by reducing the thickness of the shielding from 4.2 mm to 1 or ½ mm. The reduction must be analysed by the science institute and shall give clear requirements for the detection logic. The availability of only 0.5 mm thick detectors has required the stacking of eight detector in a detector module for a total detection thickness of about 4 mm. The parallel investigation of the philosophy has given the feedback, that a detector with D1 and D2 with 0.5 mm thick detectors in the field of view to Space and D3, D4 and D5 with 1 mm detectors will give enough information and will simplify the design and the signal conditioning. The already well known D3Plus process for stacking components shows a high benefit in the dimension reduction related mass reduction. On the other side the process is expensive and the testing of each individual bonded detector needs a high effort.

For the final design of the detector module, the tantalum shielding shall be included in the module and the front end electronic shall be placed direct beside the detectors.

PDFE Controller Bread Board Design:

The PDFE controller Bread Board wasn’t realised in Hardware. This was discussed a few times and agreed by ESA and CSAG related to the performance constraints and the high effort of the power supplies. The design in the present status is a very good baseline design but needs a high effort for the specific applications. The detection speed, the radiation hardness of the component shall be improved and the delivered documentation (specification) must be updated before a commercial application could make use of this development.

A/D Controller Bread Board Design

The manufactured Bread Board including the software shows very positive results related to the particle detection. The measurement range is split in 1024 thresholds and will help the science to perform very detailled analysis of the radiation environment. The high volume of data will require a data reduction by summarise of individual counters. To reduce power and volume we expect to reduce the memory by a clear definition of the amount of ranges. The range upper and lower limits shall be set by user commands. This will allow a high flexibility by low power and volume design.

The used A/D converter from Analogue Device already used and tested by a number of Space application (e.g. PSI by the Hessi program). A new low power and low volume radiation monitor shall include a additional evaluation phase for the A/D converter definition to get the most fitting device available at the development time.

SIP Controller Bread Board Design

This Bread Board has confirmed the replacement of the housekeeping circuits (voltage and current to frequency converter) by the SIP (Small Instrument Point) device. The new monitor will include this type of device. Within the development the interface specification was updated and in the present running strategy a design update including the RadFet and temperature sensor and an improvement by the sensor interface specification was discussed. The radiation hardness of this SREM function could be improved and the volume as well as the power consumption could be reduced. The interface to the external total dose sensors could be reduced by the serial line interface. The cable length limitation will be analysed by the update of this component (e.g. differential signal interface, RS422).

DC/DC Controller Bread Board Design

The DC/DC converter Bread Board was not realised. The availability of standard Space proofed DC/DC converter (e.g. Crane Interpoint) down to 1.5 Watt converters reduced the power consumption of the instrument from about 1 Watt by the presently used 15 Watt converter to about 300 mW.

A detail specification to a specific converter could be made after the definition of the PDFE or A7D converter signal conditioning.

High Voltage Controller Bread Board Design

The critical high voltage design and adjustment work of the present SREM circuits were analysed very carefully and a design with a regulation to a reference was designed. This circuit shows a high stability and only small changes by load changes. The design was already used in the optical terminal developments of CSAG.

This type of circuit will be used for the new monitor.

New Radiation Monitor concept:

The major functions of the SREM shall not change. The reduction in volume and mass could be realised by a special task of miniaturisation.

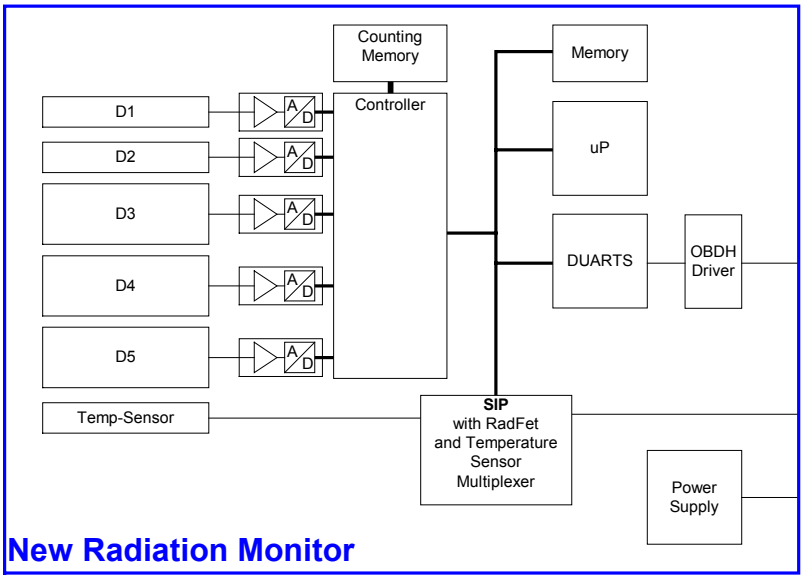

Figure 2-1 Proposed Block Diagram for New Radiation Monitor

The miniaturisation could be realised by the following tasks:

ASIC design of the VHDL designed FPGA controller.

3Dplus module design of the ASIC and memory modules top a single component.

The new radiation monitor design shall be include a design phase to verify all function and followed by a miniaturisation phase for ASIC development and high density packaging.

The VHDL coding performed under this contract was made by splitting the whole design in different blocks. The major VDHL design shall be used and has been updated only in accordance to the updated requirements.

3 CONTRACT SUMMARY

The overall MSREM contract has demonstrated the need of the bread board design for a new monitor. The following advantages could be used (with some upgrades related to the final design) for the new monitor:

- VHDL coding and the VHDL codes detail block SIP and A/D converter could be used for further developments. The use of an A/D converter in the detection must be analysed carefully during the start of the new monitor development. The approach between a commercial (low power, radiation verified component) and a possible update of the existing PDFE development must made with respect to long term availability, costs.
- Detector Module design must be updated in accordance to the new concept with tantalum inside the D3Plus design.
- The High voltage generation by using a reference voltage for the output accuracy was already improved by and CSAG R&D development (Optical inter-satellite communication Terminals)

Never less the following problems were found:

- The missing involvement and very small engagement of the scientists has produced a very critical situation. The interrupt during the start of the project with respect to new science requirement has produced a very critical situation. During a clarification meeting new requirement were presented but the agreed final specification were never submitted. This point was handled by the contractor him self without any support of the customer. The originally project idea was to miniaturise the present SREM with the current functionality with the following extended goals:
  - Improvement of the radiation hardness of critical components (V/F and IF converters)
  - Reduction in mass volume and recurring costs

  This goals has been changed to made general studies to present available components and design proposals coming form the science.

- The agreed change proposal has identified no update of the present SREM but the development of partial functional bread boards. The development with respect to the expected component information / specification has produced a considerable higher effort. This additional effort could be reduced by reduction of bread board manufacturing. The support and explanations of the component interface shows very high differences from company to company. In particular the support of Xensor System (SIP – development) must be noted. All information requests were supported within a very short time.

- The required parts could not be delivered from the AGENCY as required. The need of some components required contractor order of the needed components.

- The relation of the contract to a product of an other section of the agency has given an appearance of small support of them. We have missed to define a clear team with responsibilities during the exchange (retirement) of the project manager.

4 DESIGN

CSAG uses the Protel development system for electrical design entry. The Bread Board is designed with this system and stored at the delivered CD.

4.1 Particle Detector Module Design

The delivered and free of charge available detector chips designed by Detection Technology Inc were packaged in a very small D3Plus module. Major design points were

- Biasing voltage at about 100 Vdc
- Housing surface at ground potential
- Low volume and dimensions

After a draft layout (see at the delivered documents) the final design was made. The major problems of the design was to have enough detectors available for the design. 3D-Plus design work need normally in addition to the real deliverable models at least to sets for mechanical models. For this contract only 20 detectors were available and the mechanical models has been manufactured with mechanical replaced parts. The original planned schedule of 16 months were delayed by additional 4 months due to the manufacturing of the mechanical parts.

The final design report submitted with the final document deliverables.

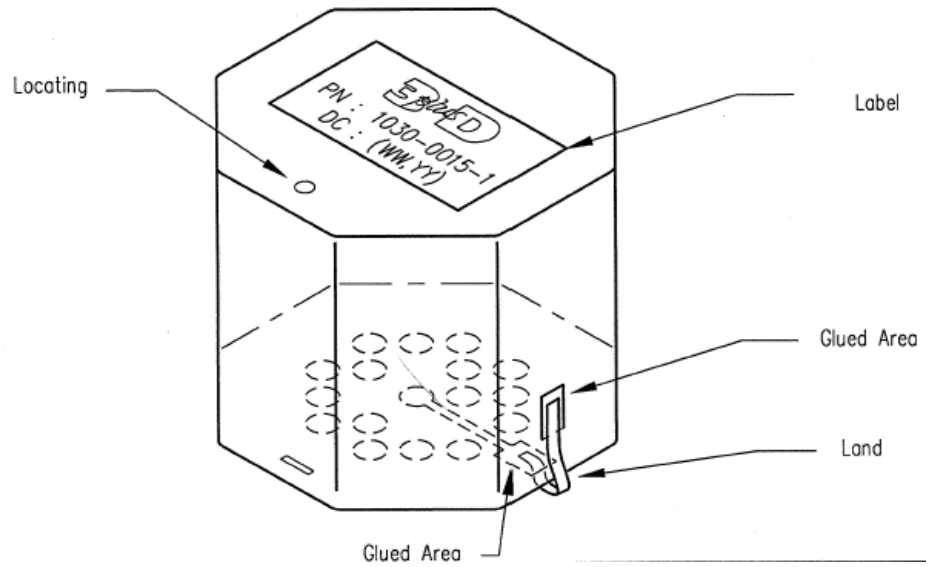

Figure 4-1 Detector Module final layout

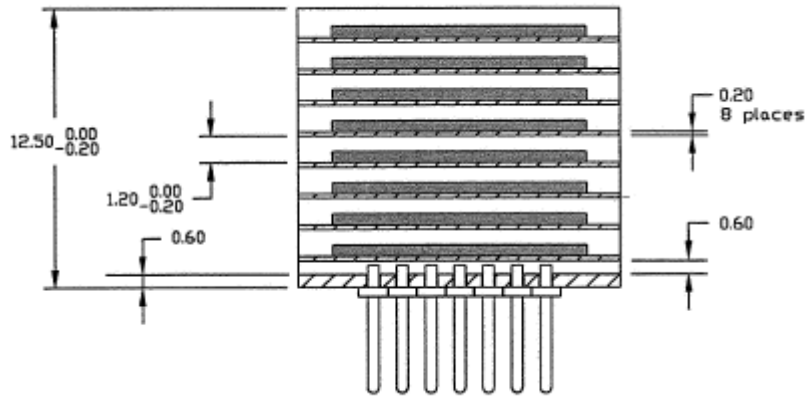

Figure 4-2 Detector Module cut view

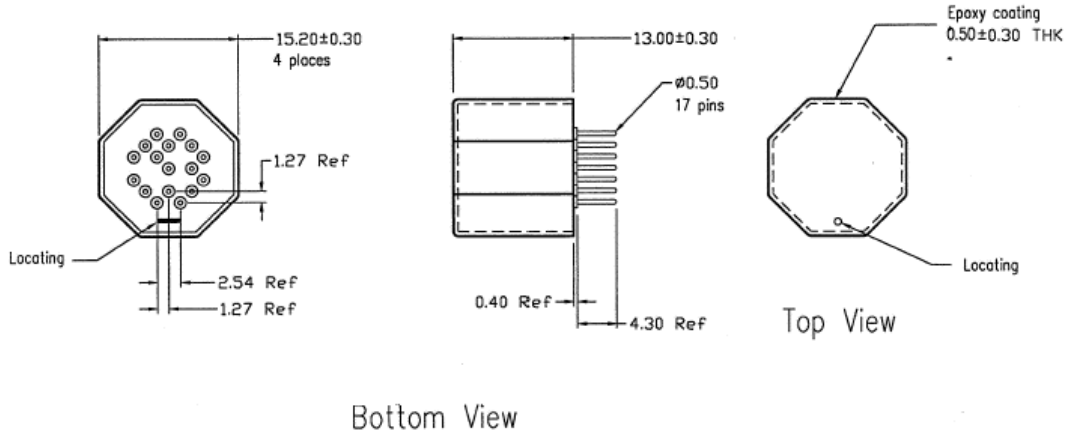

Figure 4-3 Detector Module overall dimensions

The following pictures represent the two Detector Modules each consists of 8 single detectors.

Figure 4-4 Detector Module final version

4.2 PDFE Controller Bread Board Design

The analysis of the PDFE chips shows the following problems:

1. There are five (5) different de-coupled power supplies needed.
2. The performance tests (performed by ESTEC) could be made only by a special CCA.
3. The radiation analysis (performed by ESTEC) shows a highly sensitivity of the analogue changes.

The design of the PDFE is a very important part for the independence of the European manufacturer. At the moment the present available PDFE devices are not useable for a flight application. Never less the basic of the design should be improved. There are many applications possible for such a device. During the project it was agreed to not realise this kind of bread board.

We have clearly to point out that a further radiation monitor application could use such a device by having the following improvements:

- The radiation hardness of the device shall be at least 100 kRad.
- The detection speed has to go up to at least 500'000 events per second.
- The device need a single power supply.
- The data sheet will be update in the matter of including all relevant time and timing information.

4.3 A/D Controller Bread Board Design

The bread board was designed to analyse the detection and counting of amplified signals. The main requirement of detection speed up to 500'000 events per second required a very high speed rate of the controller, related to a simultaneous detection of four channels. The detection starts with an output of the A/D converter (channel 1) not equal to 0. This start trigger will be used to detect the peak of the signal and count the corresponding counter. The Bread Board was realised with 1024 counters for each channels corresponding to the A/D output. The used gates for counting and storage as well as the readout of the counter-memory are very high and for the new radiation monitor the design shall be improved by using a section definition (software defined thresholds) of 12 sections in the measurement range. This reduces the memory capacity as well as the related power consumption and give the scientists very high flexibility.

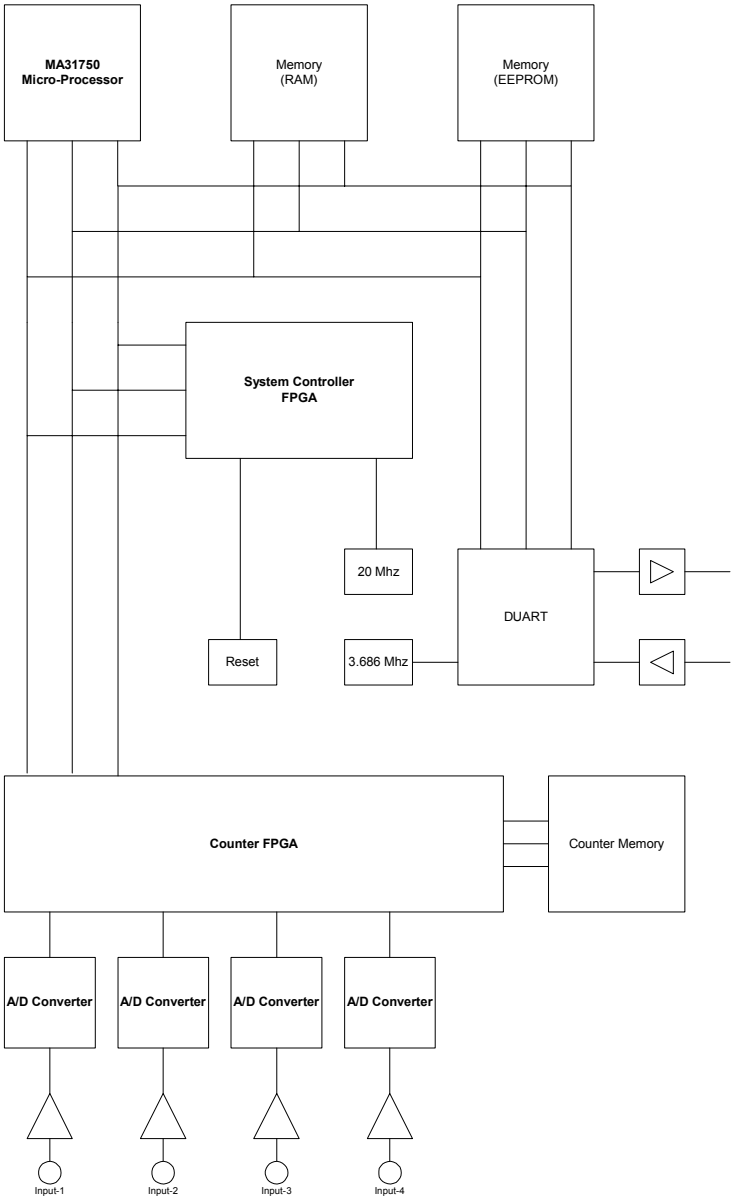

Figure 4-5 A/D Controller BB

The detail schematics of the Bread Board could be found at principle schematics of the AD-Controller Bread Board.

The A/D controller Bread Board consists of the following blocks:

- Microprocessor with Memory
- Serial Interface with Duart and Drivers/Receivers and Oscillator (3.686 MHz)
- System Oscillator (20MHz)
- System Controller FPGA
- Additional Counter Controller with Counter Ram

- A/D Controller with amplifier

The Additional controller for the counting was necessary related on the high amount of gates which was needed to detect a particle and to count the individual RAM memory .

Block Descriptions:

Microprocessor with Memory

The microprocessor and memory locates the overall microprocessor and related memories (EEPROM and RAM).

Serial Interface with Duart and Drivers/Receivers and Oscillator (3.686 MHz)

The block houses the duart with the corresponding serial clock source (Oscillator 3.686 MHz) and the RS422 driver and receiver.

System Oscillator (20MHz)

A system clock source of 20 MHz is used. This is the basic clock for the design general design.

System Controller FPGA

This FPGA includes all control logic for the microprocessor, reset and clock function. The VHDL design consists of:

1. DataMux_AD.src.vhd
   Multiplexer function for different register read.
2. ControlDUART_AD.src.vhd
   All function needed for the DUART interface.
3. InternalTimer_AD.src.vhd
   The scalar for the different internal timer and its control signals.
4. HealthConReg_AD.src.vhd
   Includes the board control register (exactly like SREM).
5. AddrDeco_MEM_AD.src.vhd
   The chip-select generation of the different memories and I/O sections.
6. RESET_AD.src.vhd
   Synchronises the reset signals to CP100 and processor clock
7. PRESCALER_AD.src.vhd
   Prepares different clocks which are needed in the FPGA internal.

Additional Counter Controller with Counter Ram

There exists four counters located in the FPGA. The values detected by the ADC's control logic are stored in a external RAM (each ADC generates 1024 different values which are used as address for the 32-bit counter). After the peak detection from a measured pulse, the following steps are necessary:

1. Read from memory (in the PFGA-Counters)
2. Increment one
3. Write back to memory

In parallel houses the counter controller the interface for the microprocessor counter readout. A request of the counter values is implemented by this controller with key point of the synchronisation of counting and readout.

1. DataMux_CO.src.vhd
   Multiplexer for different registers needed to process a detected pulse.
2. PartCou_CO.src.vhd
   32 bit particle counter.
3. REG_COMP_CO.src.vhd
   Registers and comparators needed to count a detected pulse.
4. CounterControlStM_CO.src.vhd
   State machine for detected pulse processing.
5. IOControl_CO.src.vhd
   Register access decoder and control of the counter RAM access.
6. RESET_CO.src.vhd
   Reset synchronising to CP50 (50 nsec.)
7. PRESCALER_CO.src.vhd
   Generation of different internal PFGA clocks.

The design was realised with a spare place for an additional FPGA. This on the uncertainty of including the whole design of the counter PFGA in a singled device. The present design fits and therefore the additional place is unassembled.

A/D Controller bread board with amplifier

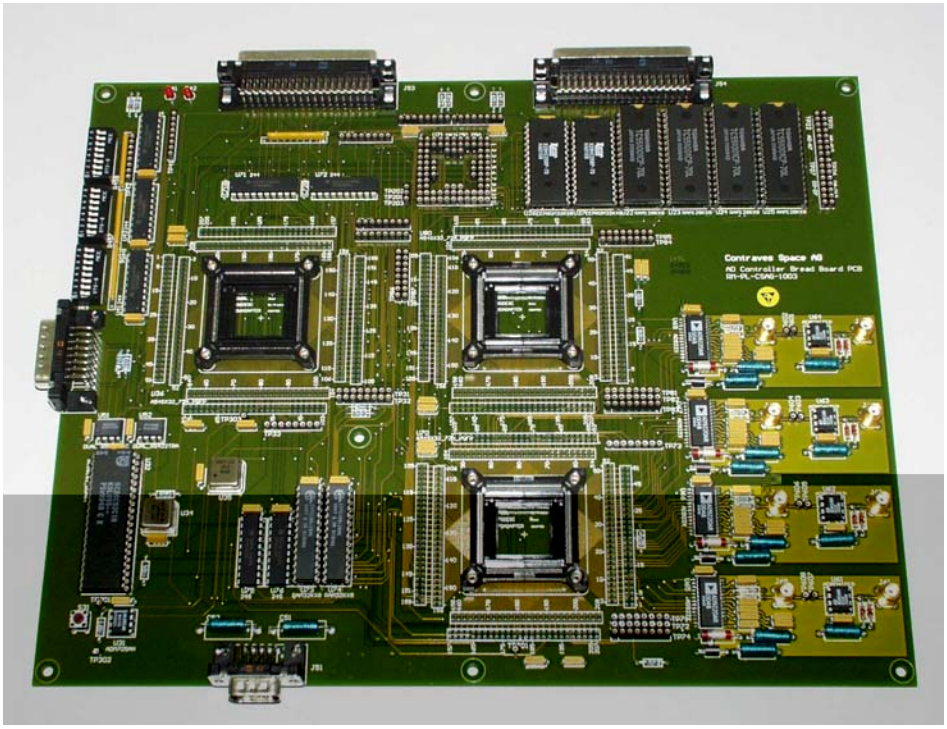

Figure 4-6 Picture of the A/D Controller BB

4.4 SIP Controller Bread Board Design

The SIP controller bread board was designed to analyse the use of the SIP (Small instrument Point) for further SREM application. The design includes a detail interface to a SIP. Two sip-chips are ordered for the Bread Board and delivered in a LCC package. Some problems by pin allocation was solved and the final application has worked. The goal to demonstrate a benefit using the SIP for total dose monitoring and housekeeping voltage and temperature monitoring could be demonstrated. The design is based on the following block diagram:

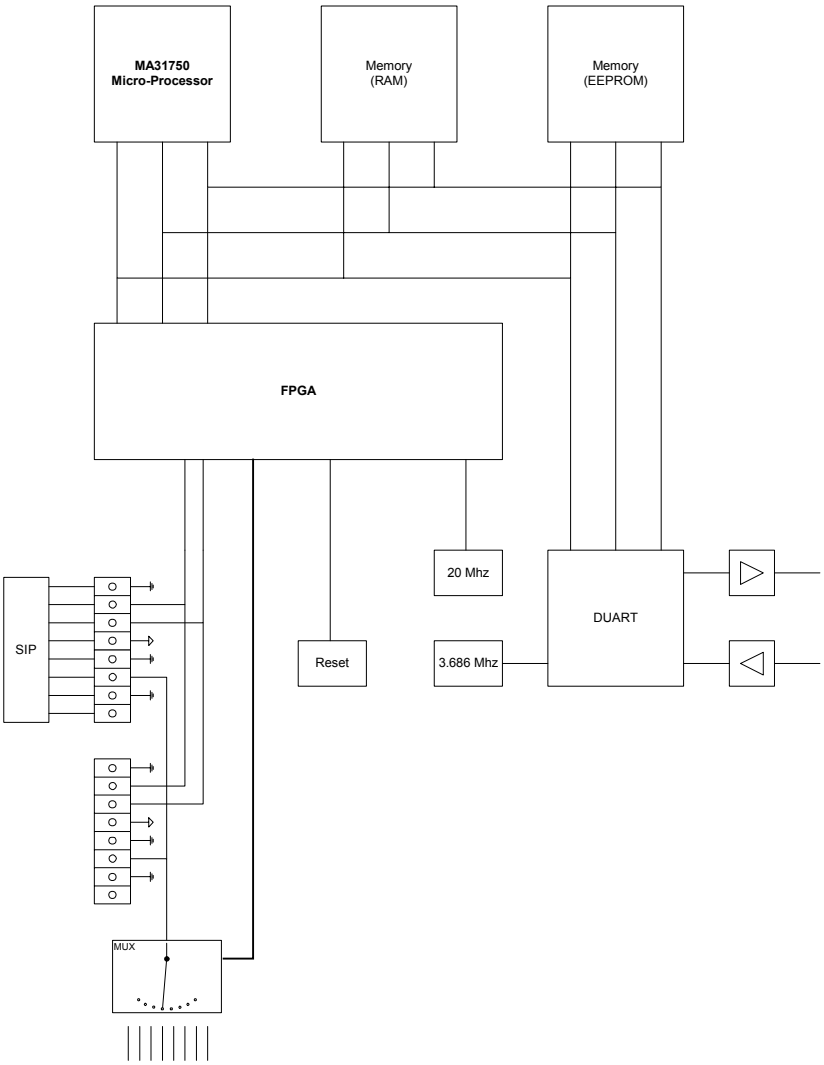

Figure 4-7 SIP Controller BB

The Bread Board consists of the following major blocks:

- Microprocessor with Memory
- Serial Interface with Duart and Drivers/Revivers and Oscillator (3.686 MHz)
- System Oscillator (20MHz)

- Interface for the SIP
- Multiplexer for channel expansion of the SIP voltage input

The whole control logic is implemented in the FPGA (Actel A54SX32A) The VHDL code is split itself in the following blocks (See ReadMeAboutFPGAStruct.TXT of the dedicated directory):

- DataMux.src.vhd Multiplexer for the databus
- SIPController_StM.src.vhd State machine for SIP interface
- ControlDUART.src.vhd DUART controller
- InternalTimer.src.vhd
  The scalar for the different internal timer and its control signals.
- HealthConReg.src.vhd
  Includes the board control register (exactly like SREM).
- AddrDeco_MEM.src.vhd
  The chip-select generation of the different memories and I/O sections.
- RESET.src.vhd
  Synchronises the reset signals to CP100 and processor clock.
- PRESCALER_SIP.src.vhd
  Prescaler for the SIP

More detail could be found on the detail schematics.

Figure 4-8 Picture of the SIP Controller BB

4.5 DC/DC Controller Bread Board Design

The DC/DC converter Bread Board could only be made by a detail design of all function of the miniaturised radiation monitor. The difficulties by the PDFE let us not develop the converter. A draft of the block diagram is shown, missing the real output voltages of the converter.

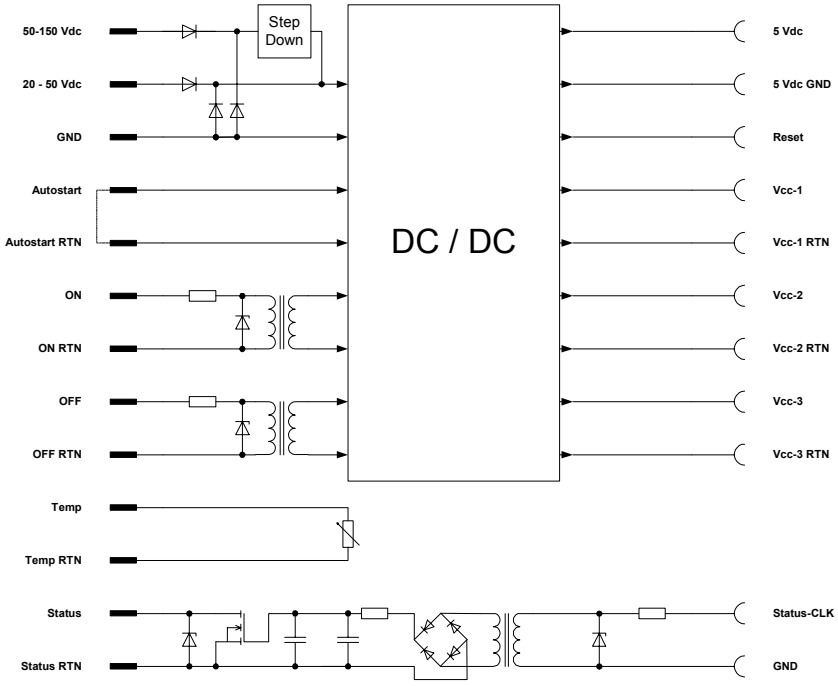

Figure 4-9 DC/DC concept for a new radiation monitor

Description of the different functions and blocks:

The input shall include two voltage section. One with the nominal input voltage from 20 to 55 Vdc and a second with an input voltage range from 50 to about 150 volts. The high voltage input shall be down converted by a simple step down converter and power the standard input range converter. The design shall be a option for high voltage power buses. The power consumption for such application will be not a key parameter and a solution with step down converter is sufficient. The main power voltage input shall be 20 to 55 Volt as it is presently for SREM. The converter shall be designed specially for this application or shall based on available DC/DC converter such as Crane Interpoint 1.5 Watt converter.

The control of the converter shall include all possibilities in parallel and shall require no action on the unit as it is manufactured. The "Autostart" shall power up the unit after a few milli -

seconds and the ON and OFF commanding shall be isolated. The power connector shall include all pins for this application.

The status signals of the unit shall be made by an isolated output. The present design from SREM with a connection to secondary voltage shows some problems by special spacecraft designs. This function could be easily implemented by using a clock signal from a few kHz from a small divider of the system clock in the Digital Electronics (ASIC of FPGA) and will power a small transformer for the isolated part. With only about 9 components the isolated part could implemented by a FET. Benefits of this design is that the status will be active only of the system clock is running. That means the secondary power of the digital electronics has to be work in the defined range.

One option which shall be discussed during the realisation of the DC/DC converter is to include a rest circuit such as the radiation hard HS705 device from Harris. This produces a clear reset as long as the digital voltage is not in range.

4.6 High Voltage Controller Bread Board Design

The High voltage Bread Board is presented in the document HV-Converter.

5 METHODICAL VDHL DESIGN

The design of the FPGA was performed in the following steps:

1. Analysis of the requirement
2. Principle design approach (including gate estimation) and block diagram
3. Detail design including simulation of each individual block
4. Overall design verification by simulation of the full function of the FPGA

To perform a most reliable design a key focus are given to the action for unused state in the design of state machines. All unused states jump to the corresponding reset (idle) state. With this solution after a possible time out of the program could activate the function again.

6 SIMULATION

Simulation philosophy:

Each FPGA contains one top entity and different sub-entities. This sub-entities was simulated isolated. Finally after each dedicated simulation of the sub-entities a simulation was performed over all.

However within the different key simulations of the sub-entities and the of the whole FPGA are performed to prevent malfunctions.

The workview office system will be used at CSAG for the VHDL development tool. The system includes a compiler (Fusion) and a simulator (Waves). The following version are present released at CSASG and used:

Workview office Version 7.5 dated Nov. 16 1998

Fusion version 2.4.1

Vwaves Version 2.4.1

The Fusion includes the Actel device programming drivers. With this tools the FPGA are programmed.

6.1 A/D Controller Bread Board Simulation

The whole VHDL code was simulated in detail. A simulation of the individual parts and interfaces was necessary (e.g.: Micro Processor interface). This extreme work was performed and the result was a full functional FPGA in the first run. The simulation was made for both FPGA's. Principle simulation work was:

1) Simulation of the detail blocks.
2) Simulation of the overall FPGA.

6.2 SIP Controller Bread Board Simulation

The simulation was performed for the system parts (microprocessor control logic) and the SIP controller. As for the A/D controller BB the simulation takes a long time and manpower but give a result with a full functional design in the first run. Principle simulation work was:

1) Simulation of the detail blocks.
2) Simulation of the overall FPGA.

7 TESTS

7.1 A/D Controller Bread Board tests

The controller work as expected in a very high accuracy. The design could be used one to one for the flight design. The tests with a frequency oscillator show only a very small noise level of plus minus one counter up to a few counts.

The following diagrams shows the test set-up:

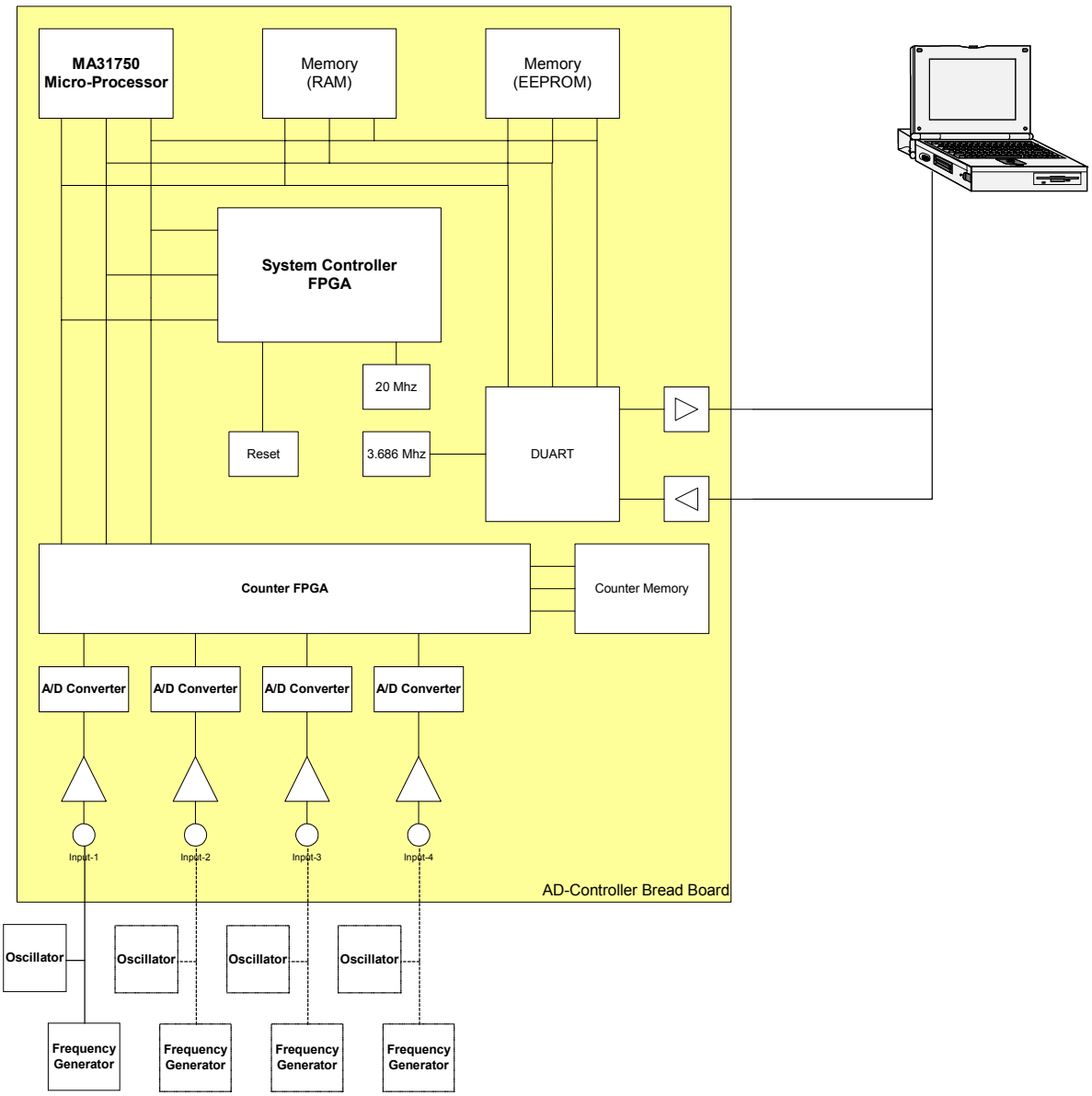

Figure 7-1 AD Controller bread board test set-up

The test are performed by connecting a frequency generator (particle simulation).

7.2 SIP Controller Bread Board tests

Table 5-1 shows the measurements of the SIP bread boards. The accuracy of the device and the connected multiplexer at the input is about 1 %. This accuracy could be reached by measuring the ground at each state to compensate some offset voltages. Disadvantage is the loss of one input of the multiplexer for this reason.

The following diagrams shows the test set-up:

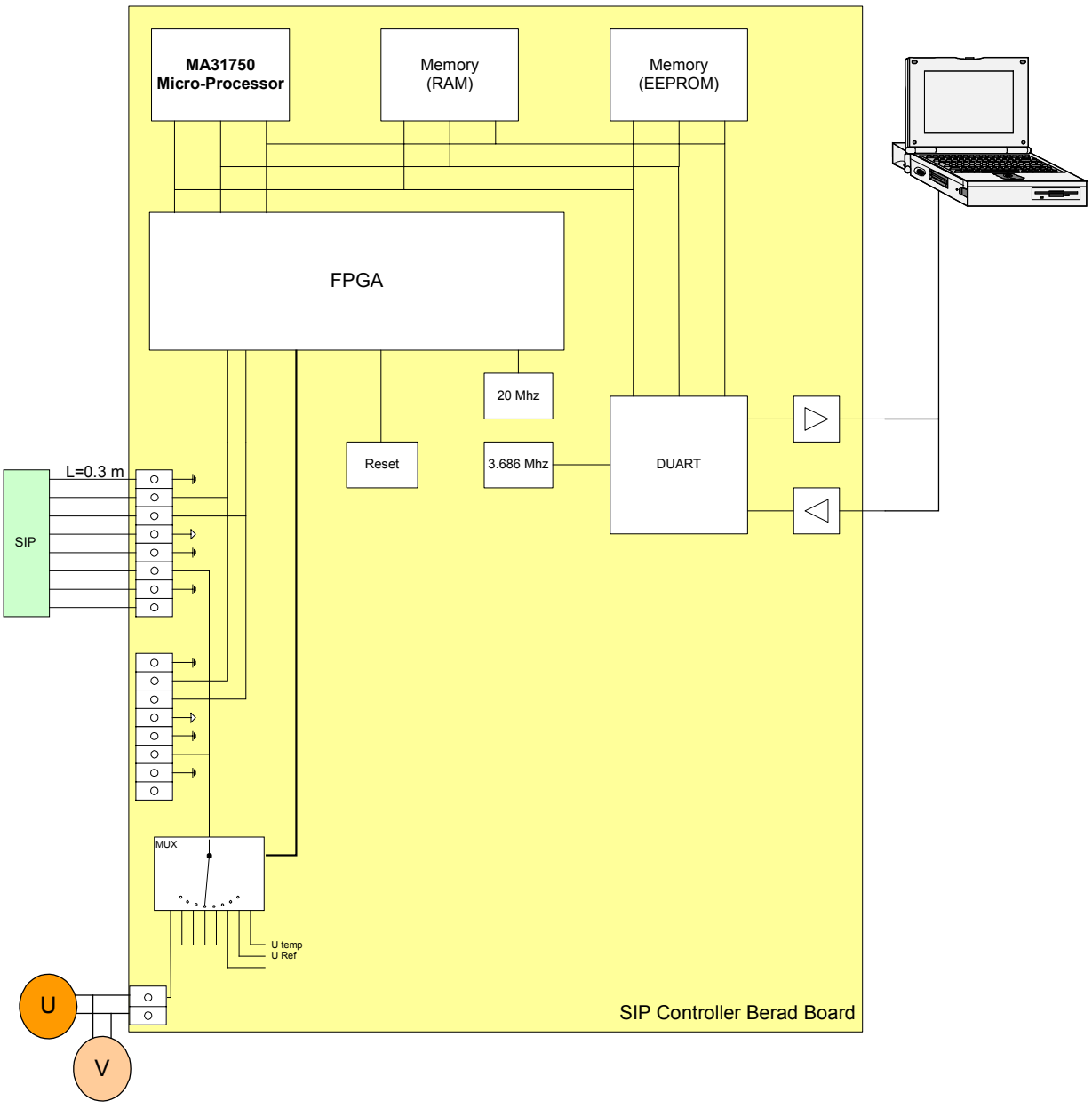

Figure 7-2 SIP Controller bread board test set-up

The tests are performed by an external high precision voltage source connected to the external user input.

SIP Measurements

		+/- 42 mV								
Input Voltage [mV]		0	10	-10	20	-20	30	-30	38	-38
Zeros	8 bit	119	89	150	59	179	28	210	3	235
Ones		136	166	105	196	76	227	45	252	20
Total		255	255	255	255	255	255	255	255	255
	9 bit	238	177	300	118	360	56	420	7	470
		273	334	211	393	151	456	91	504	41
		511	511	511	511	511	512	511	511	511
	10 bit	357	267	449	176	540	84	691	12	705
		410	500	318	591	227	683	136	755	62
		767	767	767	767	767	767	827	767	767
	11 bit	595	444	749	295	900	141	1053	20	1173
		684	835	530	984	379	1138	226	1259	106
		1279	1279	1279	1279	1279	1279	1279	1279	1279
	12 bit	1072	800	1349	528	1621	254	1895	36	2114
		1231	1503	954	1775	682	2049	408	2267	189
		2303	2303	2303	2303	2303	2303	2303	2303	2303
	13 bit	2025	1512	2549	998	3063	479	3579	69	3994
		2326	2839	1802	3353	1288	3872	772	4282	357
		4351	4351	4351	4351	4351	4351	4351	4351	4351
	14 bit	3932	2935	4938	1939	5949	929	6947	134	7750
		4515	5512	3499	6508	2498	7518	1500	8313	697
		8447	8447	8437	8447	8447	8447	8447	8447	8447
	15 bit	7743	5780	9745	3818	11716	1832	13684	263	15266
		8896	10859	6894	12821	4923	14807	2955	16376	1373
		16639	16639	16639	16639	16639	16639	16639	16639	16639
	16 bit	15367	11472	19341	7574	23256	3636	27163	520	30299
		17656	21551	13682	25449	9767	29387	5860	32503	2724
		33023	33023	33023	33023	33023	33023	33023	33023	33023
	17 bit	30497	22768	38393	15015	46142	7208	53912	1054	60125
		35038	42767	27142	50520	19393	58327	11623	64481	5410
		65535	65535	65535	65535	65535	65535	65535	65535	65535
Measurement Range [mV]		42	42	42	42	42	42	42	42	42
Calculated	8 bit	2.8	9.9	-10.2	19.8	-19.8	30.0	-30.0	38.2	-38.2
Value [mV]	9 bit	2.9	10.0	-10.2	19.7	-20.1	29.9	-29.9	38.0	-38.1
	10 bit	2.9	9.9	-10.1	19.8	-20.0	29.9	-31.1	37.8	-38.1
	11 bit	2.9	9.9	-10.1	19.7	-20.0	29.8	-30.1	37.8	-38.0
	12 bit	2.9	9.9	-10.1	19.8	-20.0	29.8	-30.0	37.8	-38.0
	13 bit	2.9	9.9	-10.1	19.8	-20.0	29.8	-30.0	37.8	-38.0
	14 bit	2.9	9.9	-10.1	19.8	-20.1	29.9	-30.0	37.8	-38.0
	15 bit	2.9	9.9	-10.1	19.8	-20.1	29.8	-30.0	37.8	-38.0
	16 bit	2.9	9.9	-10.1	19.8	-20.1	29.8	-30.0	37.8	-38.0
	17 bit	2.9	9.9	-10.1	19.8	-20.1	29.9	-30.0	37.7	-38.0
Input Voltage [mV]		0	10	-10	20	-20	30	-30	38	-38
Deviation [%]	8 bit		-1.2	2.1	-1.2	-1.2	-0.1	-0.1	0.6	0.6
	9 bit		0.3	1.9	-1.4	0.3	-0.2	-0.3	-0.1	0.4
	10 bit		-1.4	0.8	-0.9	0.2	-0.3	3.6	-0.6	0.3
	11 bit		-0.8	1.1	-1.5	0.2	-0.6	0.3	-0.6	-0.1
	12 bit		-0.8	1.0	-0.8	0.1	-0.5	0.1	-0.6	0.0
	13 bit		-1.0	1.2	-0.9	0.2	-0.5	0.0	-0.6	0.0
	14 bit		-0.9	0.6	-0.9	0.3	-0.5	-0.1	-0.6	-0.1
	15 bit		-0.9	1.1	-0.9	0.3	-0.5	0.0	-0.6	-0.1
	16 bit		-0.9	1.1	-0.9	0.3	-0.5	0.0	-0.6	0.0
	17 bit		-0.9	1.2	-0.8	0.3	-0.5	0.0	-0.7	-0.1
Average deviation [%]			-0.9	1.2	-1.0	0.1	-0.4	0.4	-0.4	0.1
Max deviation [%]			0.3	2.1	-0.8	0.3	-0.1	3.6	0.6	0.6
Min deviation [%]			-1.4	0.6	-1.5	-1.2	-0.6	-0.3	-0.7	-0.1

Table 7-1 SIP measurement table

8 DRAWINGS

8.1 Particle Detector Module Drawings

3D-Plus Design Jan-2002.pdf

8.2 A/D Controller Bread Board Drawings

PS-AD-Cont-BB.pdf	Principle Schematics
AD-AD-Cont-BB.pdf	Assembly drawing
PCB-Layout-AD-Cont-BB.pdf	PCB layout
PL-AD-Cont-BB.pdf	Parts list

8.3 SIP Controller Bread Board Drawings

PS-SIP-Cont-BB.pdf	Principle Schematics
AD-SIP-Cont-BB.pdf	Assembly drawing
PCB-Layout-SIP-Cont-BB.pdf	PCB layout
PL-SIP-Cont-BB.pdf	Parts list

8.4 High Voltage Controller Bread Board Drawings

See the document HV-converter.pdf

9 ACRONYMS, ABBREVIATIONS AND SYMBOLS

A/D	ANALOGUE TO DIGITAL
BB	BREAD BOARD
CSAG	CONTRAVES SPACE AG ZURICH
CD	PHASE C/D (REALISATION)
EEE	ELECTRICAL, ELECTROMECHANICAL AND ELECTRONIC
EEPROM	ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY
ESA	EUROPEAN SPACE AGENCY
ESTEC	EUROPEAN SPACE RESEARCH AND TECHNOLOGY CENTRE
MSREM	MINIATURISED STANDARD RADIATION ENVIRONMENT MONITOR
PDFE	PARTICLE DETECTOR FRONT END
RAM	RANDOM ACCESS MEMORY
R&D	RESEARCH AND DEVELOPMENT
SIP	SMALL INSTRUMENT POINT
SRAM	STATIC RANDOM ACCESS MEMORY
VHDL	VHSIC HARDWARE DESCRIPTION LANGUAGE