FIXED FUNCTION ASICS

Final Report

Specification	:	Final Report
Authors	:	S. Redant, L. Folens, B. Van Thielen
Document no.	:	P61282-IM-RP-004
Status	:	Issue 2.0
Date	:	2002-04-26
ESTEC Contract	:	14177/00/NL/FM(SC)

ESTEC Technical Management: M. Hollreiser

European Space Agency
Contract Report

The work described in this report was done under ESA contract. Responsibility for the contents resides with the authors or organization preparing it.

Review list

Name	Date
S. Redant	24-04-002
J. Roggen	29-04-2002

Distribution list

ESA - ESTEC: M. Hollreiser (TOS-ESM)
A. Fernandez-Leon

IMEC: L. Folens (Invomec)
G. Beeckman (Invomec)
B. Van Thielen (Invomec)
S. Redant (Invomec)
J. Roggen (BD)

Document history record

issue	Date	description of change
1.0	2002-02-18	First Version
2.0	2002-04-26	Update according to ESA comments dated 2002-04-10

Table of contents

Purpose

This document is the Final Report on the Fixed Function Asics contract.

Scope

The goal of the project is to understand the usage of deep sub-micron commercial technologies by improving radiation performance through design techniques. This should lead to independence from foundries and would provide competitive, high-performance, low power solutions for on-board data handling and digital communications payload manufacturers.
This 'proof of concept' activity for "Radiation-Hardened by design" was performed under GSTP2, ESTEC Contract 14177/NL/FM/99).
The intention of the work is to develop cell libraries with a small number of elements on transistor level, which simplifies the re-targeting effort to different technologies, if this would prove necessary.
This radiation performance improvement through design techniques mainly is a decrease of the radiation- induced leakage current at the edge of the field oxide and the inter-device leakage. The radiation induced threshold leakage voltage variation can not be attacked with these techniques. In a 180nm technology this V_t shift becomes sufficiently small to no longer affect circuit performance.

List Of Acronyms

ASIC	Application Specific Integrated Circuit
BC	Best Case
CDL	Circuit Description Language
DICE	Dual Interlocked Storage Cell
DRC	Design Rule Check
DUT	Design Under Test
FET	Field Effect Transistor
FPGA	Field Programmable Gate Array
HIT	Heavy Ion Tolerant
IC	Integrated Circuit
MPW	Multi-Project Wafer
PC	Personal Computer
PCB	Printed Circuit Board
RHbD	Radiation Hardened by Design
SEE	Single Event Effect
SEL	Single Event Latch-up
SET	Single Event Transient
SEU	Single Event Upset
TID	Total Ionising Dose
VHDL	Very High Speed IC Hardware Description Language
VLSI	Very Large Scale Integration
WC	Worst Case

References

[1] M. Hollreiser, Strategy for Low Power Radiation Tolerant Commercial Technologies, ESCCON 2000

[2] A. Giraldo, A. Minzoni, Modelling of N-Channel MOSFETs with Enclosed Layout, RadTol/RD49 meeting CERN, October 27, 1998

[3] G. Sartori, D. Bisello, A. Giraldo, Evaluation of Deep Sub-micron Technologies with Radiation Tolerant Layout of Electronics in LHC Environments, Ph.D. Thesis University of Padova, Italy, December 1998

[4] D. Bessot, R. Velazco, Design of SEU-Hardened CMOS Memory Cells: The HIT Cell, radECS Conference Proceedings, 1994

[5] T. Calin, M Nicolaidis, R. Velazco, Upset Hardened Memory Design for Submicron CMOS Technology, IEEE Transactions on Nuclear Science, Vol. 43, No 6, December 1996

[6] P. Jarron et al, Deep Submicron CMOS technologies for the LHC experiments, Nuclear Physics B (proc. Suppl.) 1999

[7] S. Dupont, Analog and Semi-Analog Design Methods, (output of ESTEC Contract No. 12495/87/NL/FM (SC)) November 1998

[8] Fixed Function ASICs Test Report Document P61282-IM-RP-003

[9] Fixed Function ASICs Study of area and timing overhead as function of library size Document P61282-IM-RP-002

1 Effects on Silicon dioxide after ionising radiation

Radiation creates electron-hole pairs. The energy required to create an electron-hole pair is about 18eV, and the total number of electron-hole pairs generated per unit dose in silicon oxide (SiO_2) is ~ $8{,}1.10^{12} cm^{-3} rad^{-1}$. The electrons (negative charged particles) are very mobile and are typically swept out of the oxide rapidly (in times of the order of pico-seconds). The holes (positive charged particles), however, are much less mobile. Some of them will recombine with electrons, but typically a large fraction is trapped inside the oxide. The number of holes that is trapped depends on the material, electric field and type of radiation. The positive charge of these trapped holes is responsible for the primary changes in the device properties (Cf. [3]).

There are two main types of effects:

- **Total dose effects** result from the interaction of ionising radiation with device materials.
- **Single event effects** result from the interaction of a single energy particle passing through a device.

1.1 Total Dose Effects

The most important Total Dose Effects in MOS transistors are:

- *Change in threshold voltage, ΔV_{TH}.*
  A smaller thickness of the oxide (t_{ox}) reduces the threshold shift (e.g. a 018µm technology has a ΔV_{TH} between 20mV and 40mV).

- *Increase in leakage current.*
  The leakage current can be sub-divided into three parts:
  - When the threshold voltage shift of the n-channel device is negative it will be difficult to turn off the n-channel device. This usually causes an increase in the ***off-state current***.
  - The pre-radiation threshold of parasitic field oxide MOS transistors (formed by supply voltage and signal routing) are so large that inter-device leakage current can be ignored. As the total accumulated radiation dose increases, the ***inter-device leakage current*** will increase, and it can determine the total dose failure level of the circuit.
  - The ***bird's beak leakage*** current is caused by the overlap between thick field oxide and the polysilicon gate. This acts as a thick oxide parasitic transistor, which can turn in ON mode due to accumulated positive charges.

- *Degradation of propagation delay.*
  A degradation of the mobility in cannel conductance and transconductance and thus a decrease in gain.

A change in one or more of these parameters is an important measure for the sensitivity of a device to ionising radiation.

1.2 Single Event Effects

Single ionising particles can cause a variety of single event effects (SEE) in silicon devices: Single Event Upset (SEU), Single Event Transient (SET), Single Event Latch-up (SEL).

1.2.1 Single Event Upset (SEU)

An SEU is a reversible change in a digital logic state due to an energy particle passing through a device. SEU is often referred to as 'soft error'. The critical charge (minimum charge needed for a change) is proportional to the node capacitance and the supply voltage. SEU sensitivity increases with the scaling of VLSI technologies towards smaller device size.

1.2.2 Single Event Transient (SET)

Current transient induced by a passing particle can propagate through combinatorial logic and cause an error.

1.2.3 Single Event Latch-up (SEL)

SEL is a destructive SEE threatening all bulk CMOS and bipolar technologies in a radiation environment. It is triggered by excess current in the base of either a parasitic *pnp* or *npn* transistor, following the charge deposition from a heavily ionising particle. This switches the parasitic thyristor in a high current self-maintaining state that can cause destructive burnout. Therefor, it can be detected by monitoring the current consumption of the circuit.
The sensitivity of a design to SEL depends on the nature of the design.

1.3 Basic layout countermeasures

1.3.1 Total Dose Effects

No layout countermeasures can be applied to eliminate threshold voltage (ΔV_{TH}) shifts or to minimise the degradation of propagation delay.
To minimise the leakage current, the following leakage components can be eliminated:

- The *inter-device leakage* current by using p^+ guard rings around the NMOS transistors. Systematic use of these rings is also effective against SEL.
- The bird's beak leakage by using edgeless NMOS transistors. Such transistors make sure that no overlap will ever occur between field oxide and the gate polysilicon.

Both techniques have been used in the RHbD library.

1.3.2 Single Event Effects

Including as much as possible substrate and n-well contacts reduces SEL occurrences.
To harden memory cells against SEU, there are several alternatives: resistive, capacitive and drive strength hardening. Drive strength hardening also protects combinatorial cells against SET.

1.3.2.1 Resistive hardening

The resistive hardening method requires the introduction of extra resistors, e.g. in the feedback loop of the cross-coupled inverters that form the storage element. Because SEU immunity imposes a minimum delay in the feedback loop of the memory element, the value of the resistors increases with device scaling. This technique slows down the propagation of fast transients. To keep the area of the resistors as small as possible, high-ohmic polysilicon resistors must be used. These are only available in an extension of the normal digital CMOS processing flow. That is why this technique was not applied on the RHbD library.

1.3.2.2 Capacitive hardening

Capacitive hardening is done by making the sensitive nodes (source/drain areas) larger to increase the critical charge. This can be done by increasing the minimum design rules (e.g. active contact overlap, contact gate spacing, etc.) For example, in an edgeless transistor, the outer diffusion ring of the NMOS transistor can be taken as drain instead of the inner diffusion area. The outer diffusion ring is about 10 times larger in area as the inner area. The disadvantage of capacitive hardening is the area penalty. Because of the use of edgeless transistors and p^+ guard rings, "Rad-Hard-by-Design" standard cells are already 2 - 4 times larger than non-radiation hardened cells. Capacitive hardening will increase this ratio to 3 – 6 instead of 2 – 4 because the outer diffusion rings of the NMOS transistors cannot be shared anymore. This means that each NMOS transistor needs a separate p+ guard ring instead of one common ring for all NMOS transistors with equipotential outer ring.
To keep the area increase as low as possible, capacitive hardening was not used in the RHbD library.

1.3.2.3 Drive strength hardening

This technique increases the drive strength of the sensitive node by increasing the sizes of the transistors that drive the node. By increasing the node drive strength the charge necessary for the compensation of the event can be more easily provided. Drive strength hardening also implies capacitive hardening because parasitic capacitances increase if transistor dimensions increase.
Since the minimum Width (W) of the edgeless transistors is 2.42µm, these transistors already have a larger drive strength compared to their standard counterparts. Without extra effort, drive strength hardening is present in the RHbD library. The maximum drive of the different cells in the RHbD library is about 33% larger in comparison with a commercial library that uses the same channel length.

1.3.2.4 Hardening by additional transistors (redundancy)

This logic/circuit level design hardening technique ensures the immunity against single node upsets. It is not just an improvement in SEU tolerance as resistive or capacitive design hardening techniques are.
Redundancy in the memory circuit maintains a source of uncorrupted data after an SEU. This uncorrupted section provides is used to recover the corrupted data. One such a structure is the Dual Interlocked storage Cell (DICE, cf. [5]). It is SEU immune for hits on single nodes. The DICE cell is only used in the RHbD1 device (see chapter 2, p17.) Another of such structures is the Heavy Ion Tolerant (HIT, cf. [4]) cell. This cell needs a differential input D and Dbar and a single-phase clock. It is also SEU immune against hits on single nodes. The ratios of the different transistors are very important in the HIT cell. Even more critical as in the DICE cell (Cf. [7]). To determine the correct ratios, it is absolutely necessary to work with stable process parameters. Transistors that have the same W/L ratio will behave different when processed with different parameters.
Neither the DICE cell nor the HIT cell is used in the RHbD library.

2 RHbD library definition and design

2.1 Cell amount vs. Synthesis efficiency investigation

The synthesis efficiency with regard to standard-cell library size, in terms of number of different cells in the library, has been investigated objectively, using several different circuits from different application fields as benchmarks.
From these investigations it can be concluded that typically the area and timing overhead are relatively small (about 6%) compared to using a full-blown library. The timing overhead can become higher (up to 30%) for designs that have a critical path close to the delay of a few logical levels in the library. The maximum area overhead is about 25%. Cf. [9].
Note that these figures compare designs made with different sizes (in amount of standard cells available) of a library. The area overhead of the hardening of the cells is not included.

2.2 Library Development

2.2.1 Library cell definition

A limited library was defined taking into account the output of the Cell amount vs. Synthesis efficiency investigation. This library consists of the following 20 core and 5 I/O cells.

Logical cells:	EXOR	2 input exclusive or
	MUX2	2 to 1 non-inverting multiplexer
	NAND2	2 input nand
	NAND3	3 input nand
	NOR2	2 input nand
	NOR3	3 input nor
	BUFD0	buffer drive 0
	BUFD1	buffer drive 1
	BUFD2	buffer drive 2
	BUFD4	buffer drive 4
	BUFD9	buffer drive 9
	INVD0	inverter drive 0
	INVD1	inverter drive 1
	INVD2	inverter drive 2
	INVD4	inverter drive 4
	INVD9	inverter drive 9

Memory cells:	Positive Edge D-flip-flop
	Positive Edge D-flip-flop with asynchronous clear
	Positive Edge D-flip-flop with asynchronous set, clear
	Positive Edge D-flip-flop with asynchronous set
	Latch with active high enable

I/O pads:	Standard CMOS output pad
	Standard CMOS input pad
	VCC pad
	VDD pad
	VSS pad

This limited library is implemented in the UMC 0.18 um CMOS technology, allowing 6 layers of metal interconnect.

The edgeless NMOS transistor has minimum W dimensions of 2.42µm. When a W dimension of a PMOS transistor is used that is twice as big: 4.92 µm, we speak of drive 1 (D1). Higher drives (D2, D4, and D9) are obtained by multiplying the W of the PMOS and the NMOS with the higher drive value (2, 4 or 9). We speak of drive zero (D0) when the PMOS width is equal to the NMOS width (2.42 µm).

2.2.2 Full-custom layout

All cells are made with the Cadence full-custom editor (Composer, version 4.3.4.46).
Together with the layout countermeasures mentioned in 1.3 *Basic Layout Countermeasures* (p.7), some full custom layout techniques were applied.
Figure 1 shows an example of a radiation tolerant design.

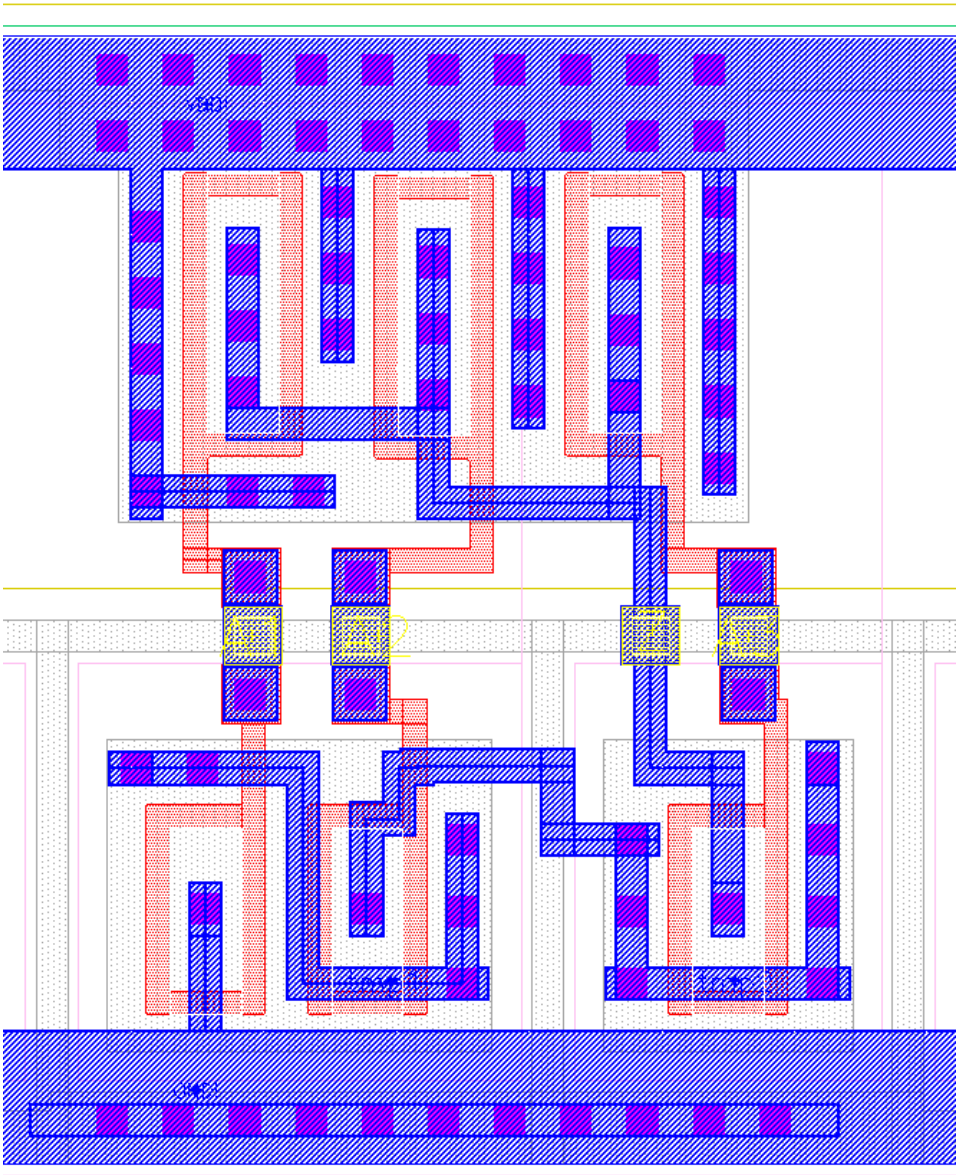


Figure 1: Use of enclosed NMOS transistors to prevent the leakage current along the device edge. Use of guard rings to isolate all n^+ diffusions at different potentials.

By placing equipotential source and/or drain regions next to each other, the number of guard rings to avoid inter-device leakage can be minimised.

Enclosed layout is not necessary for PMOS, as they typically do not have any leakage after irradiation (cf. [3]). The PMOS transistors in the library cells however, are also drawn as enclosed devices because the size of these structures fits perfectly on the edgeless NMOS transistors. The use of enclosed transistors also has some disadvantages:

- waste of area
- increase in parasitic gate and source or drain capacitances

Due to the square shape of the NMOS transistor the minimum W_N=2.42µm and L_N=0.18µm. To reduce the difference in rise- and fall transition time W_P=2xW_N≅4.90µm and L_N=0.18µm. Calculation of the effective W/L of enclosed transistors is described in [6].

The penalty area factor due to Radiation-Tolerant layout is between 2 and 4 in comparison with a commercial standard cell library (cf. the table below). The higher the drive of a cell and the more functionality it has, the bigger the area penalty factor is.

The maximum drive capacitance of the RHbD library is determined by the maximum allowed transition time at the output. This transition time was set to 3ns (0%-100%), a value comparable with other commercial 0.18µm libraries. The corresponding maximum capacitance at 3ns-transition time for the RHbD library is 1070fF. This is about 1.3 times the drive capacitance of a typical commercial library. This means that the real area penalty is lower than the penalty factor in the table because of the higher drive capability of the Rad-Tol standard cells.

Cell Name	Area (µm^2)		Factor
	Rad-Tol Height 8.49µm	UMC18 Height 6.16µm	
BUFD1	28.01	12.20	2.3
BUFD2	39.22	16.26	2.4
BUFD4	67.24	28.46	2.4
INVD1	16.81	8.13	2.1
INVD2	28.01	12.20	2.3
INVD4	50.43	20.33	2.5
EXOR2	84.05	28.46	2.9
MUX21	84.05	28.46	2.9
NAND2	39.22	12.20	3.2
NAND3	61.63	16.26	3.8
NOR2	28.01	12.20	2.3
NOR3	44.82	16.26	2.7
LATCH	190.51	52.85	3.6
DFF	291.37	77.25	3.7
DFFRL	353.01	89.44	3.9
DFFSLRL	403.44	101.64	3.9

Table1: comparison of layout size

2.2.3 Cell extraction

Out of the layout views, a transistor net-list file is extracted including all parasitic capacitance. This extraction is done with the Dracula extraction file from UMC, g-DF-LOGIC18-1.8V-3.3V-1P6M-GENERICII-DRACULA-LPE-1.5-P0.txt (revision 1.5).
For further characterisation of the cells in the library, IMEC will use Calibre software to do the extraction. By comparison with the Dracula extraction file, all parasitic capacitors are a factor 10 times smaller (Calibre extracts more realistic capacitance values). That means that all transition- and delay times are smaller and will be updated in the next release of the library.

2.2.4 Cell characterisation

The cells were characterised using the HSpice circuit-simulation over the full range of technology and power-supply variations and over the allowable temperature range. Simulations have been done for different output loads and for different input slopes. Delays were measured from 50% of the input slope versus 50% of the output slope. Output slopes were measured from 10% to 90% of the supply voltage.
The corners used for the simulation were:
Best Case: Fast-Fast process, 0 degrees Centigrade and 1.92V power supply
Worst Case: Slow-Slow process, 125 degrees Centigrade and 1.62V power supply.

2.2.5 DRC (Design Rule Check)

DRC rules were checked with the UMC DRC rules file.

2.2.6 Front-end view generation

Three Synopsys .lib files have been generated for the library, following the principle of Table Lookup Delay models (Synopsys non-linear tables, 5X5).
The Worst Case simulation results were used in a WC lib, the Best Case results were used in a BC lib. Typical results were used in a TYP lib.
Verilog models were written for functional simulation.

2.2.7 Supported Tools

The “Rad-Hard-by-Design” cell library that was developed in the course of this activity can be used for the following tools:

- Synopsys Design Compiler (including area-dependent wire_load estimation with the same values as the commercial library)
- Synopsys PrimeTime timing analysis
- Verilog simulation (zero-delay (functional) only)
- Avant! Apollo (layout: cell views(GDSII and black box) and timing views)
- Calibre, or any other LVS (Layout versus Schematic) tool using CDL input

There is an obvious gap in the simulation models (VITAL and Verilog timing models). This gap will be filled in follow-up activities together with new additions to the small library (Cf. chapter 5).

2.3 Proof of concept

2.3.1 Implementation of two chips

An existing design (The OZONE an MPEG 4 Wavelet Quantizer, O3 for short) was ported to the newly developed library and to a non-hardened commercial library for the same process: UMC 0.18 CMOS. The latter library will be referred to as the COM library. Devices designed with that library will be called COM1 and COM2.

2.3.2 VHDL adaptation

The O3 was previously designed for an Alcatel Microelectronics 0.5-micron technology. The synthesis to generate net-lists for layout in both the libraries could not start from the original VHDL description of the O3 because in that description technology dependent RAM IP blocks were used. These had to be replaced by either latch of flip-flop banks. Latches were chosen because of area considerations. During this update, timing of the banks was carefully considered, so that post-synthesis timing-analysis would be easy to assess.
The logic that was originally included for the test accessibility of the RAMs has not been removed.
Pre-synthesis simulations were re-run to ensure that the new source VHDL was still functionally correct. The simulation results (output files) were – successfully – compared to the original simulation output.

2.3.3 Synthesis

The directory structure that was used during the original O3 design was kept, because a.o. make scripts supported the design flow. In this structure, all the hierarchical components of the O3 had their own directory and their own individual synthesis script (Synthesis was done bottom-up).

These scripts and the Design Compiler start-up files had to be changed because of the new choice of technology. Because of the smaller technology more care was taken considering timing issues. Because all start-up files were links to a central file, the changes in the start-up files were done in that single file. The changes in the synthesis scripts were done using stream-text-editor (“sed”) scripts to ensure that all changes/improvements were performed in all the synthesis scripts.

The first post-synthesis functional simulations however did not generate the same output as the RTL VHDL simulations. Eventually the error was pinpointed to be a Design Compiler bug. The Synopsys help web-site contained a script that allowed finding out whether a particular bug was haunting the design. It turned out to be that this was the case.
The web site also gave a work-around for the bug. This work-around was built into all the Design Compiler scripts. After doing a re-synthesis the functionality of the net-list was correct.

Scan paths were included with Design Compiler. For the design in the RHbD library, this was done using a “dummy” scan cell, that was afterwards replaced with a flip-flop and a multiplexer from the small library, as no dedicated scan cell existed in the small library. All flip-flops are in scan chains. There are 10 different chains.

For the synthesis to the commercial library, the whole ASIC design flow including post-layout simulation and timing analysis was performed.
For the synthesis to the RHbD library, the post-layout simulations were not performed, because the Verilog simulation library models at the time were only functional views, not including timing.

Due to several setbacks more than one production run was necessary to get working chips. Six different devices can be identified: COM1, COM2, RHbD1, RHbD2, RHbD3 and a TESTCHIP. All chips, except the TESTCHIP have the same O3 functionality.
COM1 and RHbD1 were produced on the same shuttle run. COM2, RHbD2 and TESTCHIP were together on another shuttle run. RHbD3 was on a third, separate run.
All O3 devices (except the TESTCHIP) were packaged in an 84-pin package of which 78 pins are used. Each of those chips has 8 supply pairs. All of the O3 chips are pin compatible.
A history of the several devices follows.

2.3.4 The Commercial devices

2.3.4.1 COM1

2.3.4.1.1 Packaging problem

After finding out that the devices weren't operating as they should some measurements made clear that there were internal shorts between several pins of each chip. Pins that even were situated on opposing sides of a device. There was no apparent method in which pins were connected together.
Flipping the lid off a few of the chips and putting them under a microscope revealed that

- there was a metal 'ring' all around our chip. UMC places such a die seal ring around each circuit. It is in fact a guard ring type structure, made out of all metal and via layers. The ring increases yield during sawing, for it acts as a barriers for the cracks that can occur.
- the bonding was done such that some of the bonding wires were touching this die seal ring and as such were shorted (Cf. figure 3 and figure 4).

This explained the shorts.
To verify these facts some devices bonded were at IMEC to ascertain that this was the problem. Tests revealed that it indeed was the case.
Furthermore 5 device were packaged at a nearby packaging plant to do measurements.

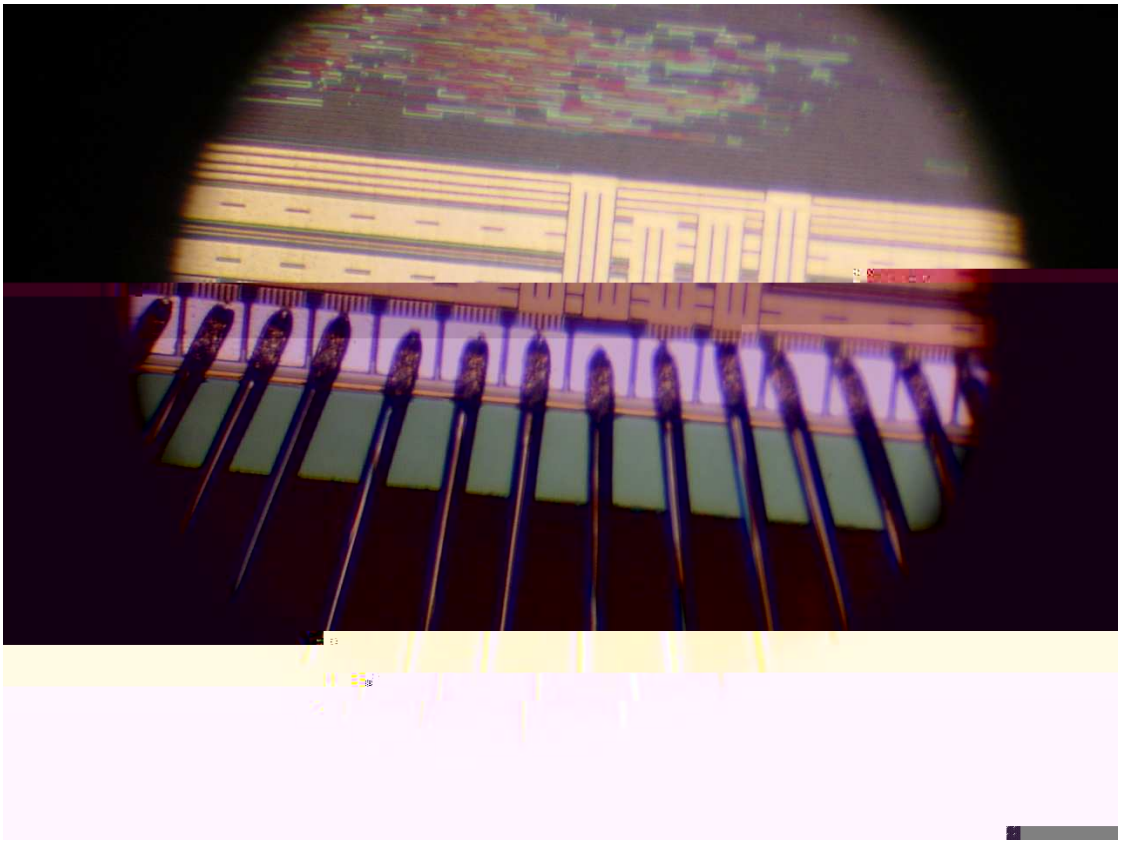


Figure 3: The incorrect bonding, 'large' view

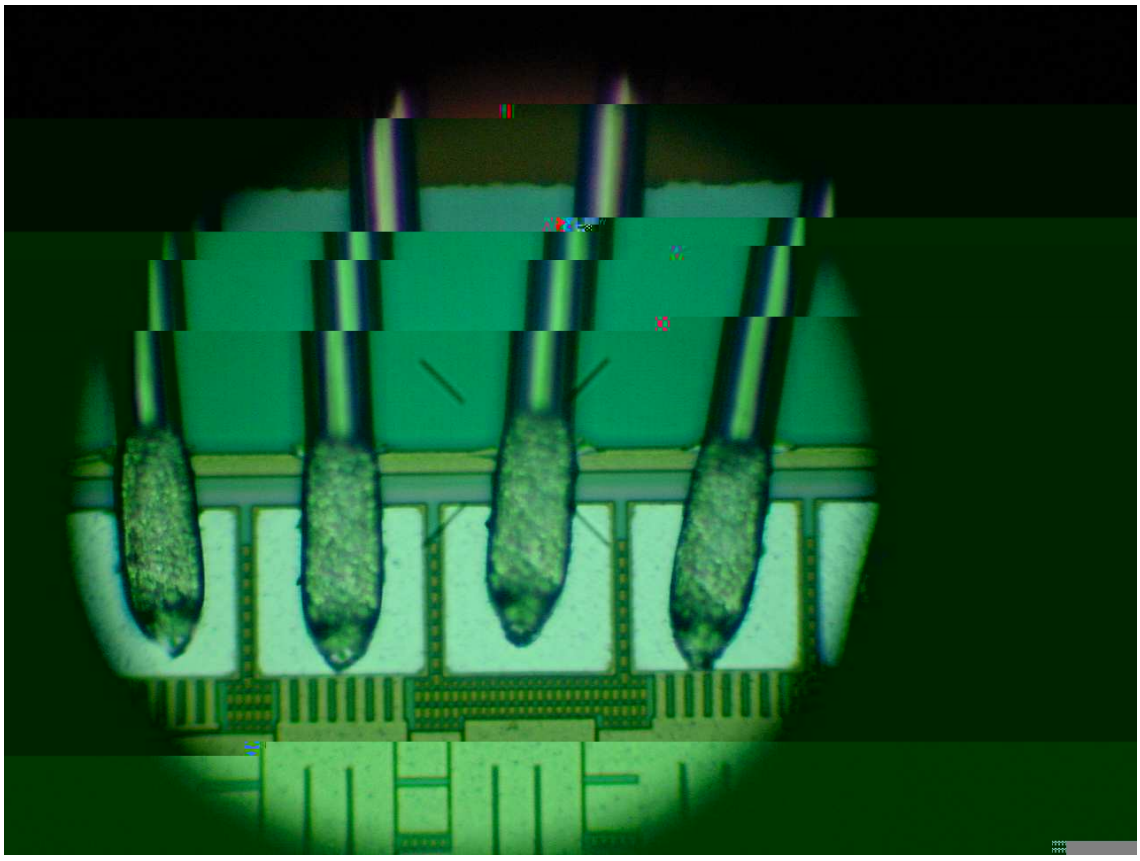


Figure 4: The incorrect bonding, detail

Two actions were taken to lower the risk:
- For the next generations UMC was asked not include a die seal ring around the dies.
- It was decided to use a 3rd packaging firm that could guarantee the bonding.

2.3.4.2 Library problem

The commercial library at that moment did not include a flip-flop with an asynchronous set only. The synthesis tool hence used flip-flops with both asynchronous set and reset for the five instances that needed an asynchronous set only. The synthesis tool decided to connect both the asynchronous pins together because set overruled reset.
The library timing did however not reflect the real timing of the cells and therefore the simulations, nor did the timing analysis spot the fact that connecting the asynchronous set and reset together resulted in a reset, not in a set. The reset became inactive later than the set on a real device.
The real silicon hence had five flip-flops that were reset in a wrong state. A simulation where the flip-flops were altered to give a reset instead of a set was used to find out if this error could cause the erroneous behaviour. The simulated behaviour was identical to the one seen on the real device. Unfortunately the start-up state of these 5 flip-flops had as a consequence that the devices could not be used in any way to perform the tests. Too little activity could be seen on the outputs.

2.3.4.3 COM2

The resets of the five erroneously reset flip-flops were disconnected and connected to VDD instead (inactive). All simulations and analyses were re-run and a new chip was manufactured. The resulting device was fully functional. It has been subjected to TID radiation tests.

Chip Statistics:

pad limited design	
width:	2050 µm
height:	2130 µm
area:	4.3665 mm2
# standard cells:	52850
# of nets:	67687
# of Transistors :	531082
# of flip-flops:	1205
# of latches :	14080
Cell/Row utilisation:	84,03% (pad limited)
# of equivalent gates:	129275
# of equivalent gates/mm2:	60834 (kind of low because pad limited)

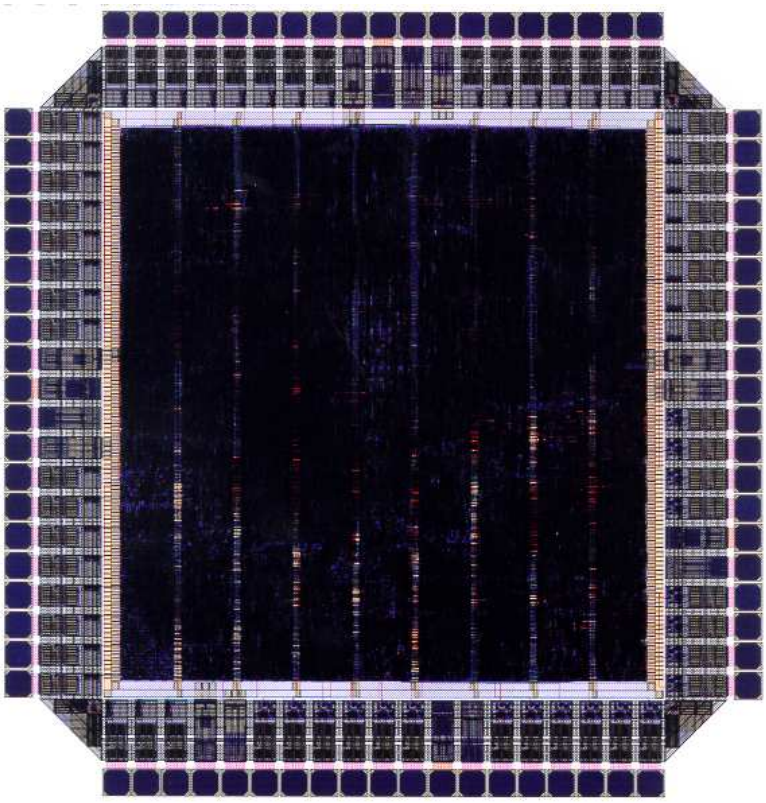


Figure 5: COM2 layout

2.3.5 The RHbD devices

The gate density of the chip in the small "Radiation-Hardened-by-Design" library is 21400 # of equivalent gates/mm2.

2.3.5.1 RHbD1

2.3.5.1.1 Packaging problem

The same packaging problems were seen as with the COM1 devices, as they were packaged at the same time at the same packaging company. The same solution was used to overcome the problem.

2.3.5.1.2 Parameter problem

There was still a problem of power consumption of the chip. Liquid crystal techniques were used to spot the areas where the chip heated up first. Once the temperature is high enough at a particular spot, the crystals on top of that spot turn black. It is at these spots that the most current flows and the most power is dissipated.

It was clear that the heating-up took place in the corner where the flip-flops were situated (Cf. figure 6).

.

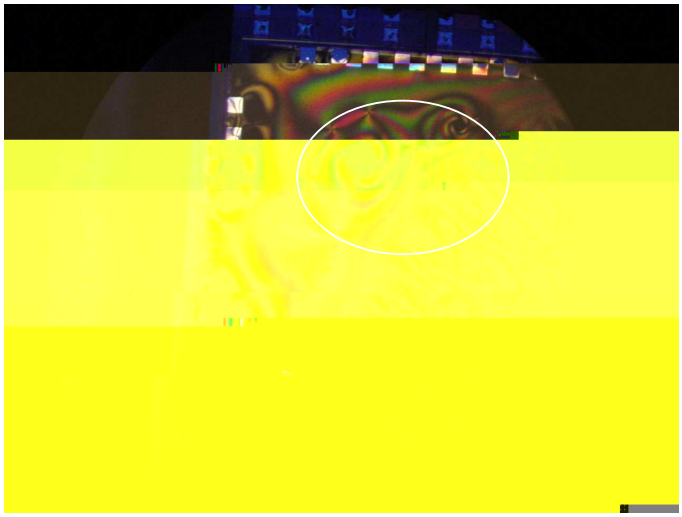


Figure 6: picture of liquid crystal test

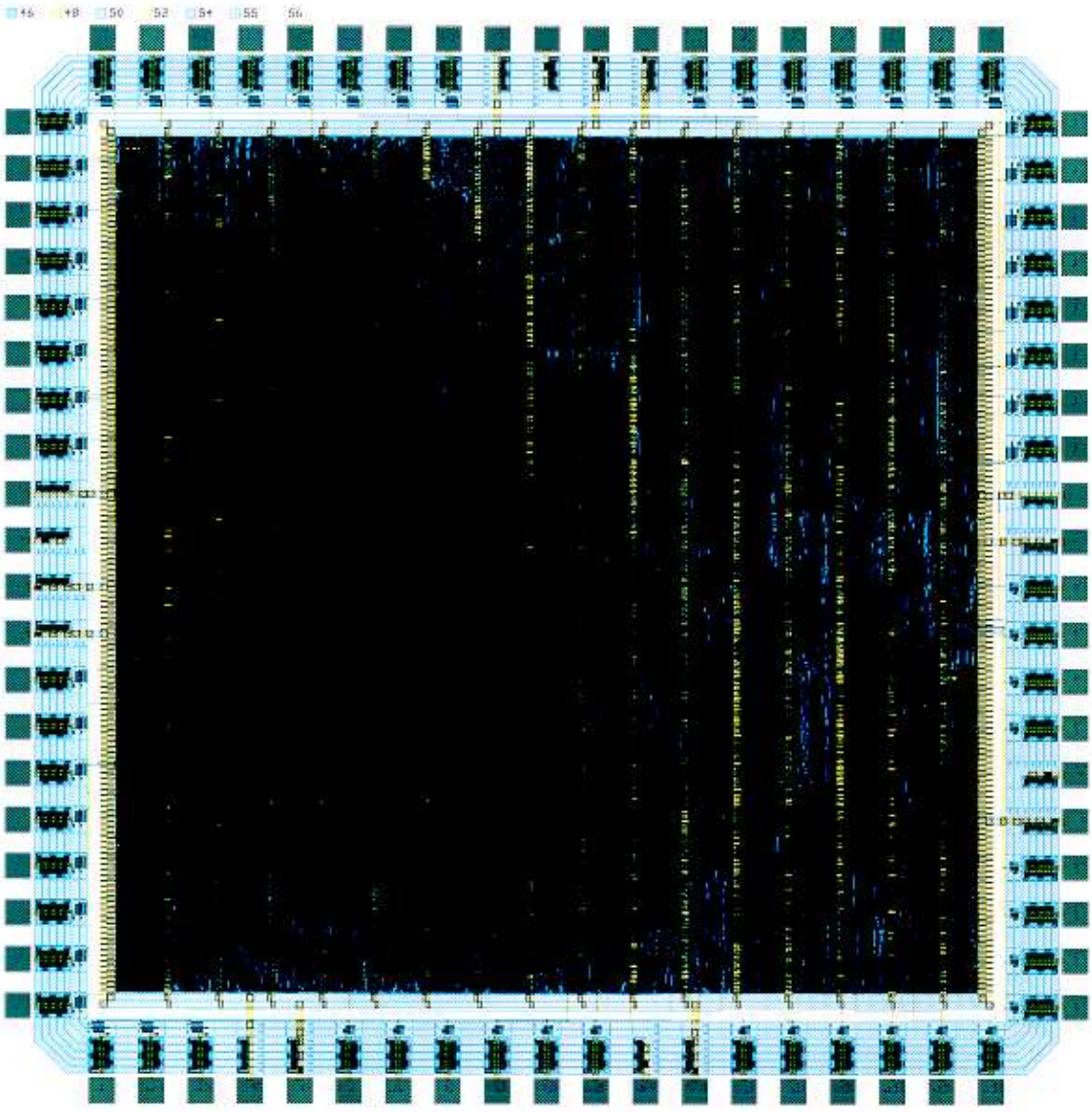


Figure 7: RHbD1 layout

Chip Statistics:

Core limited design	
width:	3219 µm
height	3207 µm
area :	10.324 mm2
# standard cells:	90486
# of nets:	105858
# of Transistors :	647569
# of flip-flops:	1205
# of latches :	14080
Cell/Row utilisation:	96.51% (core limited)
# of equivalent gates:	139000
# of equivalent gates/mm2:	21400

During simulation all memory cells were stable in all corners of the processing. After processing the memory cells did not work and were not stable anymore. The reason for this malfunction was that UMC had tuned the processing parameters. The DICE cells are very sensitive to parameter changes and with the new set of parameters the DICE memory cells had an additional stable point where they were drawing current. To reduce the risk on a second failure due to parameter problems, the Agency decided not to use DICE cells in the new design. New memory cells were developed without redundancy logic (DICE) to guarantee the functionality of these cells after a new processing. At this moment these cells are not SEU hardened (not resistive, capacitive hardened). Drive strength hardening is present due to the use of edgeless tranisistors for TID protection.
Because of the amount of cells involved, the change from DICE to non-DICE structures required the chip to be re-synthesized.

2.3.5.2 RHbD2

These devices were processed using the new non-DICE flip-flops. Because of the sizes of other chips on the MPW and to be able to add TESTCHIP on the MPW, a new aspect ratio was used for the chip. This was necessary to maximise the silicon usage on the MPW.
The power consumption of the devices was within the expected levels. However, the functionality was incorrect. Because of the complicated functionality of the O3, assessing what was wrong was not trivial. Therefore the scan behaviour was investigated. From this investigation it became clear that there was something wrong with the reset of the device. The reset seemed to be constantly active. The problem could be tracked down to a discrepancy between the simulation/synthesis model and the actual layout/spice model of the multiplexer. The simulation/synthesis models were non-inverting, whereas the layout/spice model was inverting.
This discrepancy could not have been found by running a software check (like e.g. LVS). This kind of check compares the layout of the device to its transistor schematic. But checking the functionality of the synthesis library vs. that of the transistor schematic can only be done "by hand" (i.e. it's prone to human error). Post-synthesis simulations can only check the consistency of the synthesis library vs. the simulation models (Cf. figure 8).

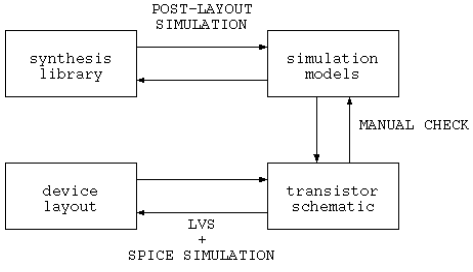


Figure 8: library checks

The inverted multiplexer indeed explains why the device was constantly reset. Figure 9 shows the clocking and reset scheme of the O3. If the multiplexer in the reset path is inverted, an inactive reset signal is inverted to its active state, keeping the device in reset.

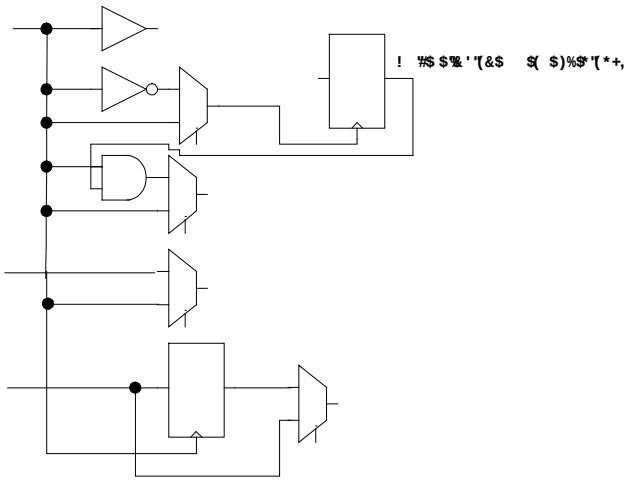


Figure 9: the clocking and reset structure of the O3

Inverting the external reset signal solved the continuous reset problem, but it was impossible to adapt to all the consequences implied by the extra inversion.
The erroneous multiplexer was used in the clocking circuit. Figure 9 shows that there are two external clocks, HW_CLK and SW_CLK. In functional mode (test signal set to '0'), three internal clocks are derived from HW_CLK. Two of them have the multiplexer in their path (Test_Inv_HW_CLK and Buf_GatedHW_CLK). Only these two get inverted. The third one, HW_CLKBuffered, does not pass through the multiplexer, therefore it does not get an extra inversion. SW_CLK is also inverted. The inverted clocks mix up the internal timing requirements of the device, which increases the chance for a malfunction dramatically.
In scan mode however, test is set to '1' and SW_CLK is not used anymore. All internal clocks are derived from HW_CLK. The inversion of some clocks does not matter here since all chains are independent from each other and each of them uses only one clock. Therefore, the device still worked in scan mode.
A third problem was that the multiplexer was also present in the control paths. Reading and writing correct functional parameters, enable/disable data- or control paths the right way became impossible.
Functional simulations indeed proved that the device completely looses its functionality when the inverted multiplexer is used. Tests could still be performed using only scan mode, but the scan chains only cover the flip-flops (¼ of the total area of the device). The latch banks (the remaining area) are not tested in scan mode. For full proof of concept, this is not sufficient.

2.3.5.3 RHbD3

A decision was made to not re-synthesise the chip with an adapted library but to replace the multiplexer cell layout with a non-inverting multiplexer layout and to re-process the chip.
The resulting device was fully functional. It has been subjected to TID radiation tests.

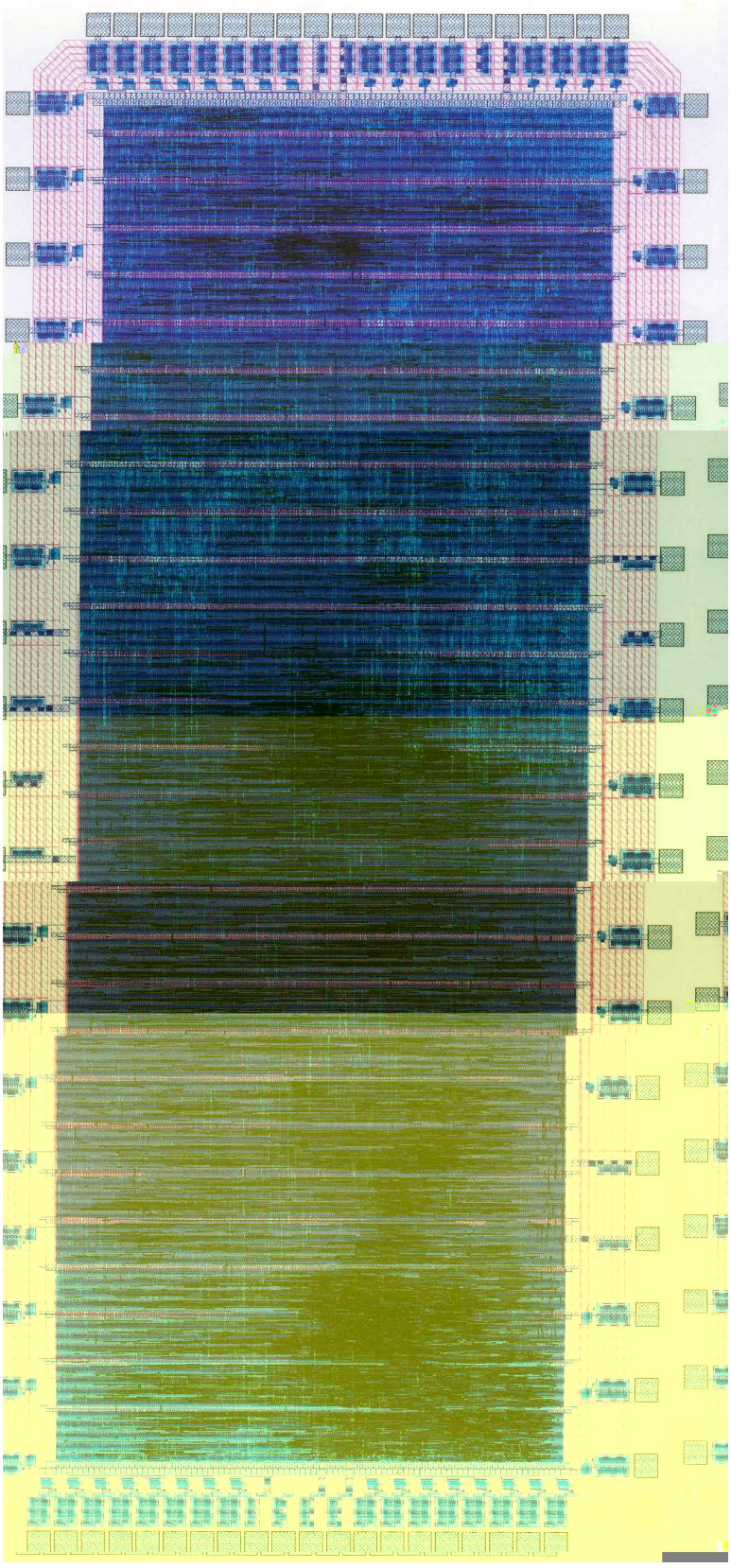


Figure 10: RHbD3 layout

Chip Statistics:

Core limited design

width:	4899.9 µm
height	2196.12 µm
area :	10,761 mm2

#standard cells:	91350
# of nets:	106740
# of Transistors :	617747
# of flip-flops:	1205
# of latches :	14080
Cell/Row utilisation:	94.91% (core limited)
# of equivalent gates:	144.324 kGates
# of equivalent gates/mm:	21000

The 5kGates difference in the number of equivalent gates between RHbD1 and RHbD3 can be explained by different factors. First, redoing the synthesis of the chip before processing RHbD2 resulted in a different mapping of the functionality on to the library. Second, the non-DICE cells are about 13% smaller than the DICE cells. Both facts affect the total area occupied by the standard cells. It is this area that is used to calculate the number of equivalent gates.

2.3.5.4 TESTCHIP

Together with the manufacturing of COM2 and RHbD2 a TESTCHIP was manufactured. This was done as a safety precaution to be able to measure individual cell behaviour when problems would arise. The TESTCHIP also included adapted DICE flip-flops designed using the updated parameter set.
The TESTCHIP has not been used for measurements.

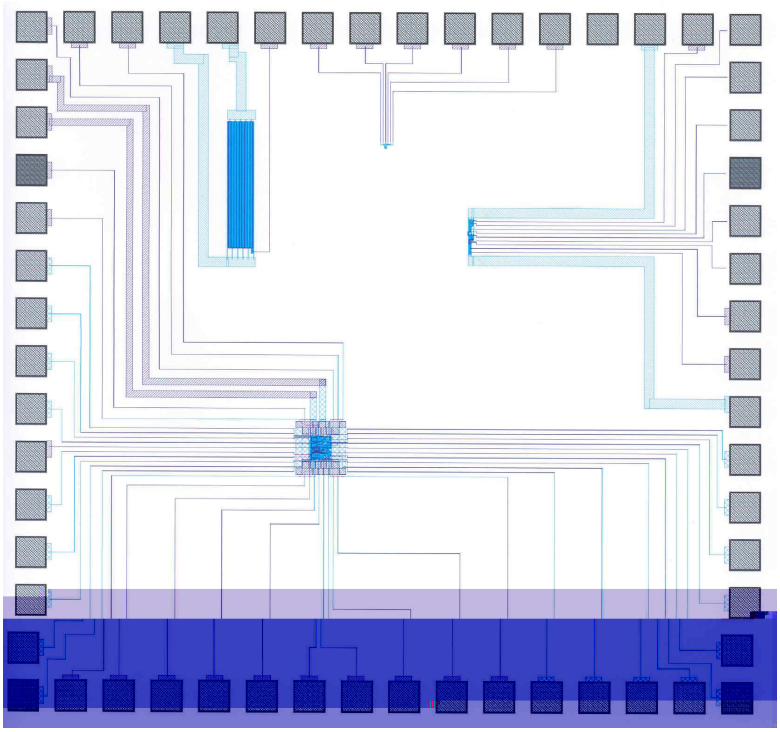


Figure 11: TESTCHIP layout

Chip Statistics:
Pad limited design

width:	2350µm
height:	2200µm
area:	5.170mm^2

3 Radiation test

3.1 Test Set-up

3.1.1 Basic structure

The existing test set-up of the O3 was used as the basis of the test set-up of the radiation test. A PC expansion card carrying an FPGA provides a data communication link between the Device Under Test (DUT) on the test board and the test data on the hard disk of the PC. The interface between the PC and the FPGA is handled by a C-program. Configuration of the FPGA is done using logic synthesis from a VHDL description.

3.1.2 Test set-up as used in the TID tests

The existing functional test strategy needed to be expanded/adapted in order to meet the TID test requirements. A new C-program as well as new VHDL code had to be written. To perform the tests, two new printed circuit boards (PCB) had to be designed. The first one is used to check the functionality of the devices in normal – and in scan mode. Current measurements are also done using this board. The second board holds up to 12 devices while being irradiated. Both boards can be used to test the COM devices and the RHbD devices. However, due to the supply voltage difference between both types of devices, they can not be put on the boards together. A different test cycle is needed for each type of device.

3.2 Irradiation set-up

The Cobalt 60 source at the faculty “Chimie des Matériaux Inorganiques et Organiques (CMAT)” of the University of Louvain La-Neuve was used as radiation source. The source is situated in the centre of a circular chamber (radius 2m). The PCB carrying the devices is placed inside the irradiation chamber. The distance between this PCB and the centre of the Co-60 source depends on the required dose rate (Cf. Figure 12 and Figure 13).
A 15m long power cable connects the PCB to a power source outside the chamber.

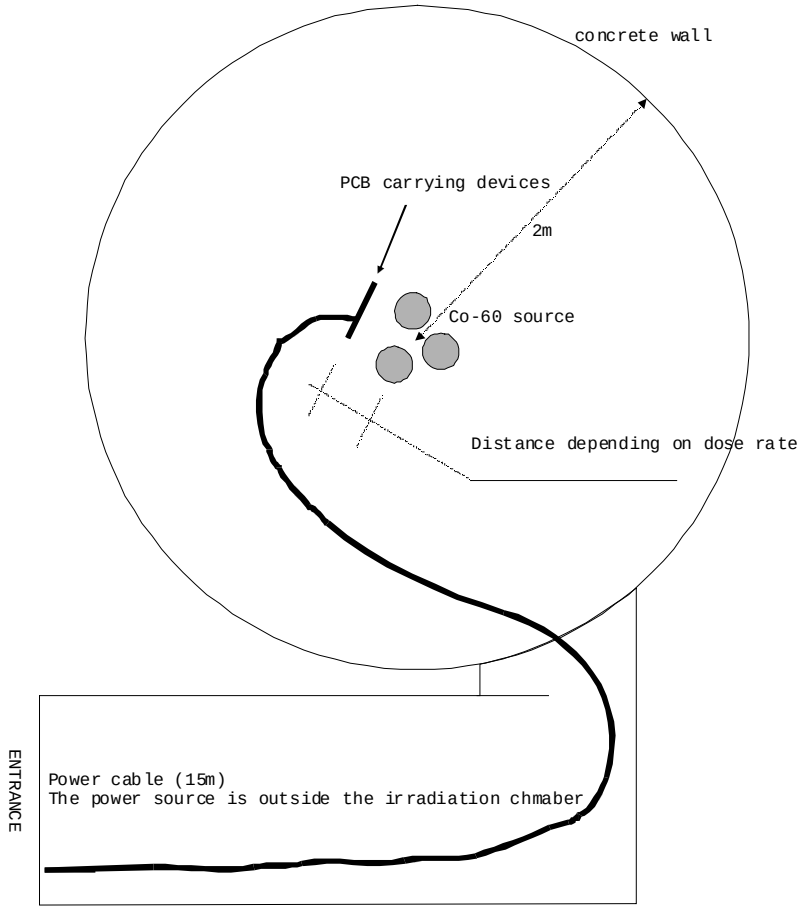


Figure 12: Irradiation chamber

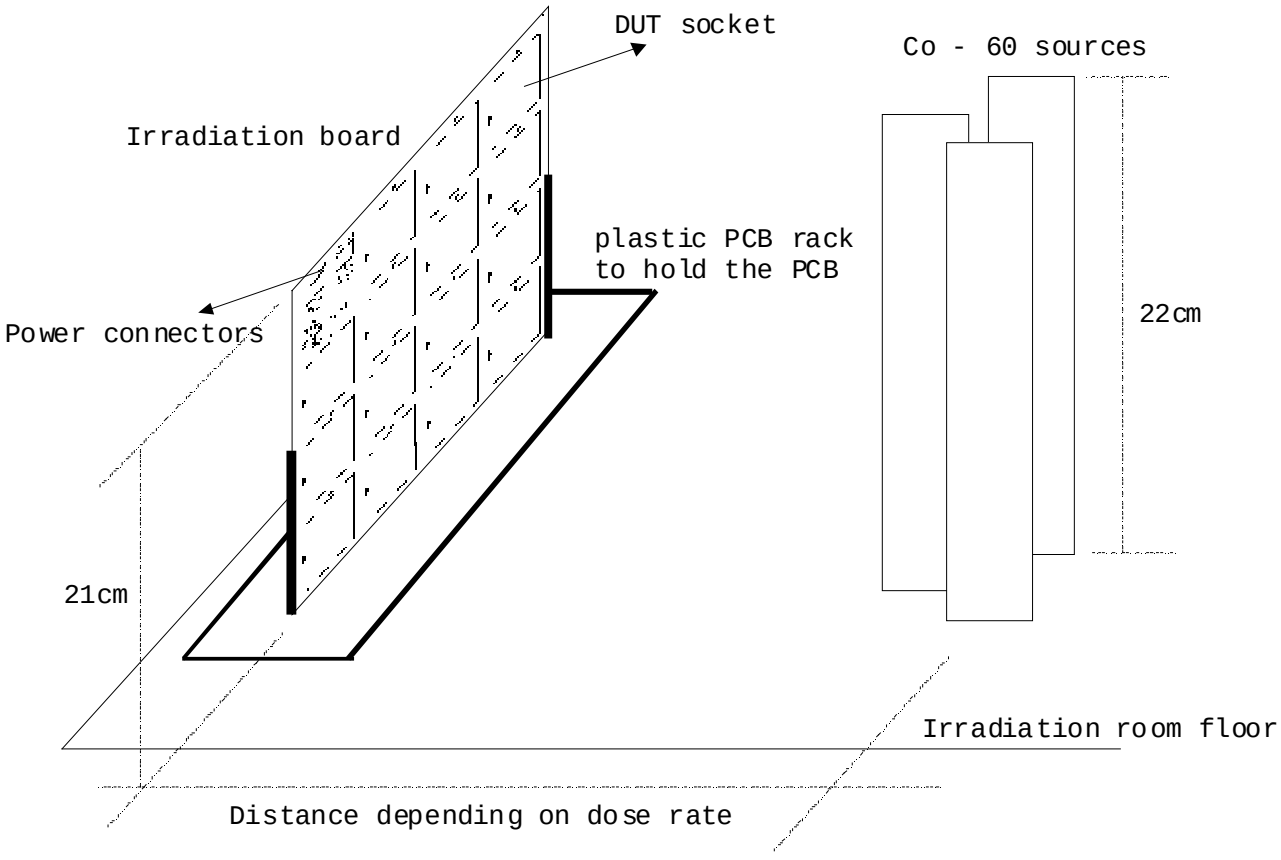


Figure 13: Irradiation set-up

The irradiation board is 20cm high. The dose rate inside the irradiation room has been measured at 8,5cm above ground level. The dose rate at 20cm is 2.5% higher than at 8.5cm, and the dose rate at 0cm is 2.5% lower than at 8.5cm. In other words, the dose rate at 20 cm high is 5% higher than the dose rate at ground level (0cm). This means that the dose rates of the Co-60 source are in accordance with the requirements of ESA/SCC Basic Specification No. 22900. This specification states that the non-uniformity of the radiation field shall be maximum 10%.
Cf. Figure 14: uniformity Co-60 source.

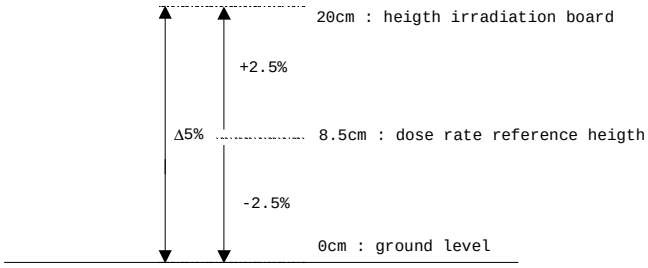


Figure 14 : uniformity Co-60 source

3.3 Test method and results

A TID test was applied to both types of devices (COM and RHbD). Four devices of each kind were tested, each in a different 2-week test cycle.

3.3.1 Test method

The total dose to be reached was set at 1Mrad. This level is reached by applying 9 consecutive irradiation steps. During those steps, the devices are on the irradiation PCB, inside the irradiation room and power is turned on. All power and ground pins are connected to power and ground, respectively. All inputs are set inactive (data inputs connected to ground, active low control inputs connected to power, active high control inputs connected to ground) and all outputs are floating (unconnected). When a step is completed, the devices are taken out of the room and they are tested immediately.
While a device is under test, current is measured three (after power up, after HW_CLK is started, after start of SW_CLK and RESET). The current is not monitored continuously. Cf. Figure 15: current measurement set-up.

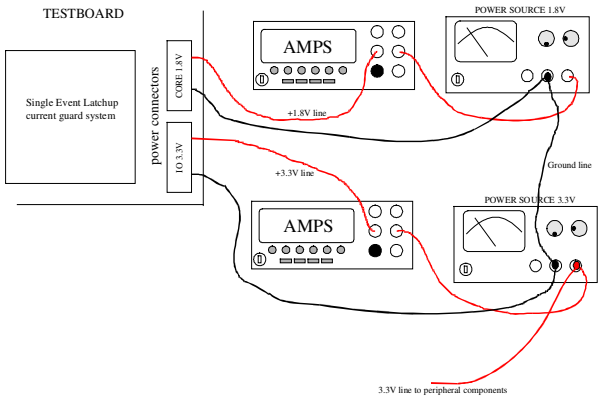


Figure 15: current measurement set-up

The time needed to test all 4 devices is approximately 15 minutes. The measurements done, the devices are put on the irradiation board again. The board is placed back inside the irradiation

room and power is turned on. The devices stay in this condition for about 3.5hrs. before the next irradiation step starts. This was done to set the increase in total dose to 100krad each irradiation step. A constant irradiation time of 20hrs each step and a constant dose rate of 5krad/hr result in 100krad total dose each step. Both types of devices were irradiated in exactly the same way. Cf. Figure 16: flowchart TID test.

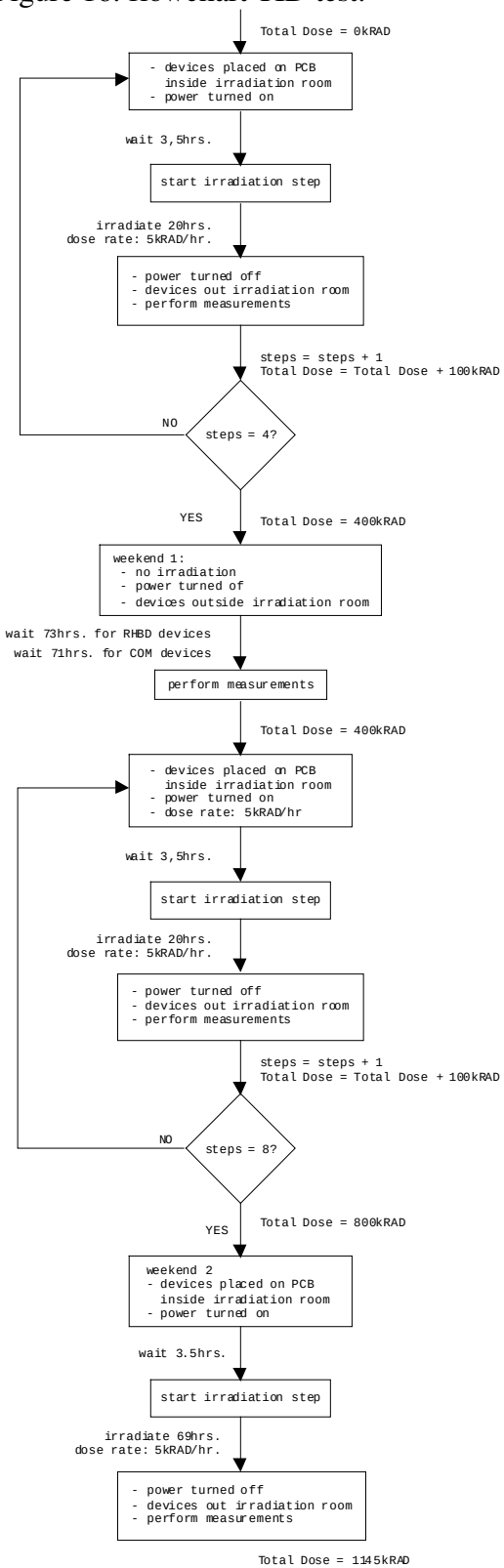
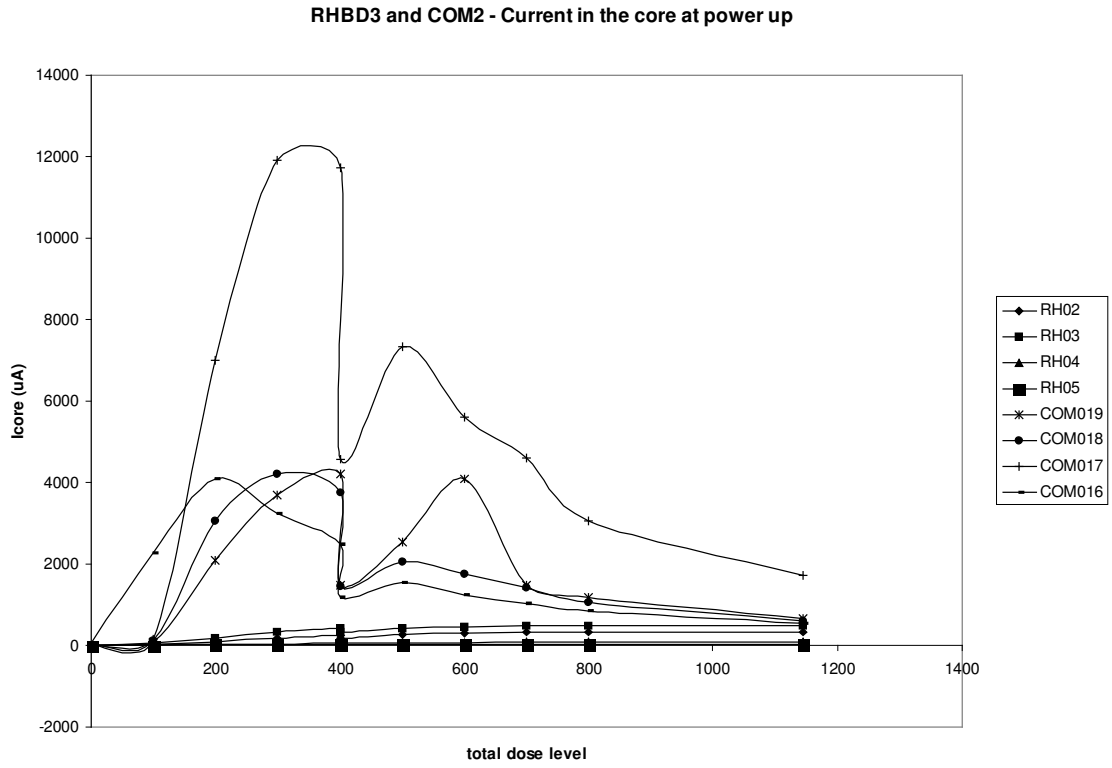


Figure 16: flowchart TID test

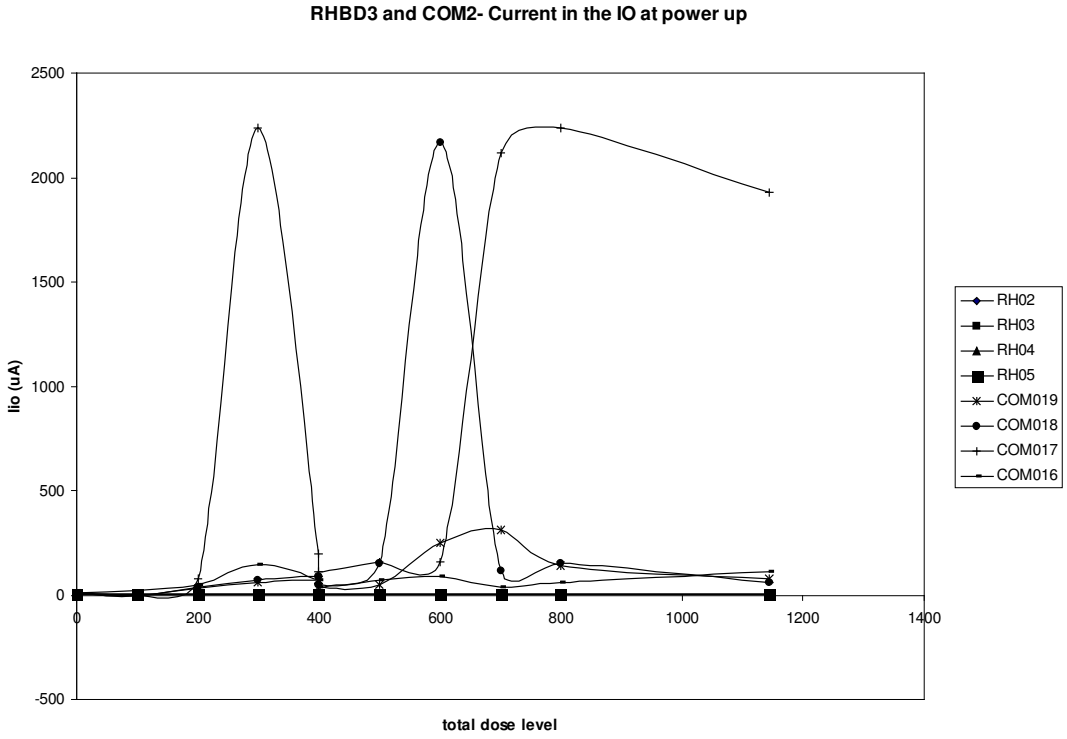
Dose rate: 5krad/hr
Total dose / step: 100krad (20hrs * 5krad/hr)
Time between two steps: 3,5 hrs
Exception: The irradiation cycle lasted 11 workdays, including 2 weekends. The first weekend, no irradiation took place. The devices were inactive and at room temperature. The power supply was turned off. This lasted for a period of 71hrs for the COM devices and 73hrs for the RHbD devices. After this period, the devices were tested again. The outcome of these measurements resulted in the current drop in the graphs (annealing effects). At this moment, the devices were placed back into the irradiation room, power was turned on and the irradiation cycle continued.
The second weekend the devices were continuously irradiated for 69hrs (69hrs * 5krad = 345krad). This way the total dose went well over 1Mrad, to 1145krad.

3.3.2 Results

The results shown in this document are a comparison between the results of measurements on the RHbD and COM devices.



Graph 1 : I_{CORE} at different total dose levels for COM2 and RHBD3 devices



Graph 2 : I_{IO} at different total dose levels for COM2 and RHBD3 devices

4 Conclusions

The result of the investigation of the trade-off between cell amount and synthesis efficiency for the RHbD library was positive. Typically the area and timing overhead are relatively small compared to using a full-blown library. The area and timing overhead depend on the nature of the design and on which kind of cells are used to implement the design.

The penalty area factor due to Radiation-Tolerant layout is between 2 and 4 in comparison with a commercial standard cell library. The higher the drive of a cell and the more functionality it has, the bigger the area penalty factor is. This penalty is reduced because the transistors used in the RHbD cells are bigger than standard transistors. The RHbD cells have a higher drive capability compared to commercial standard cells.

The field of interest for space applications is situated around 200krad to 400krad. In graph 1 (core measurements), the values for the RHbD devices (range 16uA – 193uA at 200krad, range 29uA – 426uA at 400krad) are smaller than the values for the COM devices (range 2097uA – 6987uA at 200krad, range 4197µA – 11717µA at 400krad). At 400krad, the maximum for the RHbD devices is 27.5 times smaller than the maximum for the COM devices.
In graph 2 (IO measurements), the same results can be found. The current for the RHbD devices (range 2µA – 3µA at 200krad and at 400krad) is again smaller than the current for the COM devices (range 30µA – 80µA at 200krad, range 70µA – 200µA at 400krad). At 400krad, the maximum current for the COM devices is even 70 times larger than the maximum current for the RHbD devices.

Why the leakage current is dropping again after about 400krad is not understood yet. The possibility was mentioned that it was caused by a change in the state of the flip-flops (flip-flops that power up ‘0’ at low total dose level, power up ‘1’ at higher levels). Circuit simulations on the DFF data flip-flop were done to investigate the relationship between different start-up modes and static power consumption. Outcome of these simulations shows that the static power apparently depends very little on the start-up mode (even when simulated in the different process corners).
The measurements have shown that the commercial library shows a considerably bigger leakage current after TID irradiation in the dose-rates that are interesting for space applications.

Even though no SEU measurements were done yet, the TID measurements show that the idea of radiation-hardness by design is valid because the leakage current can differ an order of magnitude with the RHbD cells.

5 What the future holds

To improve the area penalty factor due to the limited library, several typical designs will be investigated and a limited amount of much-used core cells will be added to the library. The number of cells in the library will remain limited compared to a commercial library.

The following views will become available for the cells in the library:

- Layout for all the cells in GDSII format
- Layout abstracts for Avant! Apollo
- Timing views for Avant! Apollo, enabling timing driven layout
- VITAL simulation models
- Verilog timing simulation models
- Synopsys Design Compiler (synthesis), Test Compiler (scan insertion and ATPG) and PrimeTime (static timing analysis) and non-compiled (humanly readable) .lib files (with the Wire load estimation identical to the commercial library).
- CDL net-lists for LVS checks (e.g.with Calibre)
- Flextest & Fastscan models

Because many applications use memories, a single-port RHbD RAM compiler will be added to the library.

For the library to be suitable for usage in present-day applications it is also necessary to add more I/O pad options with improved ESD performance.

A more exact figure for the area penalty between the RHbD library and a commercial one will have to be calculated after comparison of layouts of a design mapped to the RHbD library and to a comparable sub-set of a commercial library.

The focus however should not be to compare the RHbD library with a commercial library, but to compare the RHbD library with a radiation-hard technology. That will clearly show the gain in cost, timing and maybe even area the RHbD library brings.

Because the requirement for a space mission is around 200 kRad (Si) parametric, the relative influence on the leakage current of the guard rings with respect to that of the enclosed transistors is also a subject of future investigation. Library density could be improved if the impact of one of the layout techniques would be the major contributor.

The concept of RHbD being portable to future, smaller technologies also gives interesting perspectives. Speed, power, cost and yield gain would add onto the fact that more functionality can be integrated on the same chip-area.