Executive Summary

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CHANGE RECORDS

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1. INTRODUCTION

The present document is generated in the frame of the "Low power, radiation tolerant microelectronics design techniques", a contract awarded by ESA to Alcatel Space and Imec.

This report summarises the activities and results obtained during the course of the study: it is an abstract of all documents generated including papers presented to conferences.

This study contract was initiated by ESA for the following reasons:

- many manufacturers/foundries offering radiation-hard or radiation-tolerant technologies have left the market due to reduced demand from military and aerospace customers and lack of commercially interesting volumes,
- current and future payloads are requiring more and more computing power. These processing capabilities can only be provided by Deep Sub-Micron technologies, offering high performance and low power consumption.

Therefore, the study "Low Power, Radiation tolerant microelectronics design techniques" was initiated by ESA in order to analyze and validate the possibility to use a commercial standard technology of which radiation withstanding could be improved by design, at library level. The objective was to demonstrate the feasibility of developping an ASIC with a specific library (Radiation Hardened by Design), and to measure the radiation behaviour of the chips manufactured with the "commercial" technology in the frame of the multi-project wafer (MPW) approach provided by Europractice. The selected technology is the 0,18μm from UMC (Taiwan).

The study "Low Power, Radiation tolerant microelectronics design techniques" consisted in the following main items:

- the development by IMEC of a library hardened by design (DARE library),
- the development by IMEC of a test vehicle containing all the elementary cells of the library,
- the development of a complex telecom ASIC by Alcatel Space, based upon the DARE library. Associated to that were also foreseen the analyses of DSM design specifities,
- once manufactured, packaged and tested: the characterisation of both test chip and ASIC in terms of functionality, performance and radiation,
- the comparison of DARE performances versus its commercial source
- the elaboration of a report posing the problems of the QA and procurement tasks related to an ASIC developed with a DARE library on a commercial technology.
- the definition of the valuable tasks still to be conducted after the completion of the present study.

The study has been **successfully** completed now, and all results are available. A summary of them is provided in the following pages.

2. ACRONYMS

ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
CTS	Clock Tree Synthesis
CWLM	Custom Wire Load Model
DARE	Design Against Radiation Effects
DRC	Design Rules Check
DSM	Deep Sub-Micron
DW	DesignWare (Synopsys trade mark)
ECO	Engineering Change Order
FF	Flip Flop
HDL	Hardware Description Language
I/O	Input and output
LBO	Location Based Optimisation
P&R	Place & Route
PDEF	Physical Design Exchange Format
RH	Radiation Hardened
RT	Radiation Tolerant
RTL	Register Transfer Level
UMC	United Microelectronic Corporation
VHDL	Very high speed integrated circuits HDL

3. PROJECT ORGANISATION AND TASKS

The project was quite complex, with many various activities and, overall, many entities involved.

The following chart shows all main tasks that have been performed during the project, and who did perform those tasks.

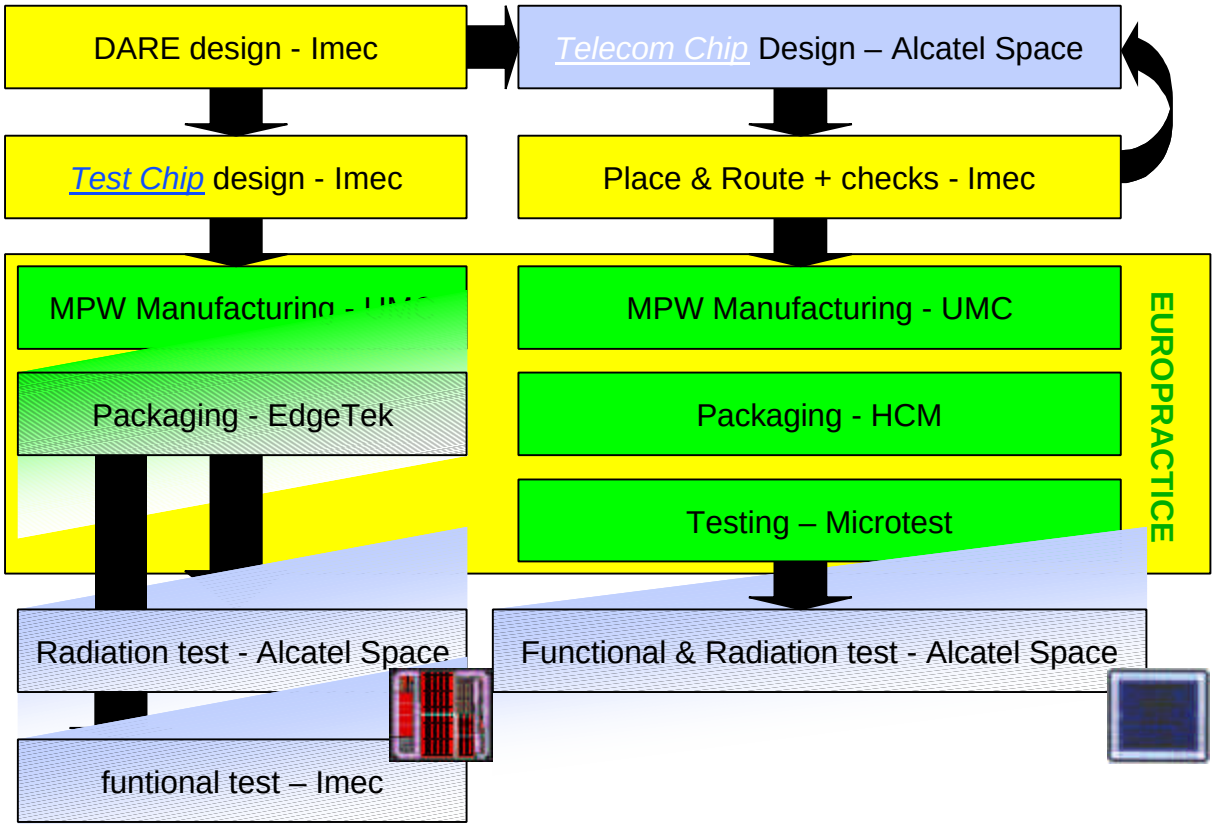

Figure 1: DIE HARD test-chip layout

4. LIBRARY DEVELOPMENT

The DARE library is meant to be used in combination with commercial foundries technology, and seeks foundry-independence while providing competitive, high-performance, low-power, low mass solutions for components to be used in harsh radiation environments.
It was shown in previous studies that the concept of improving radiation performance of components manufactured in commercial deep sub-micron technologies through the application of special layout techniques is valid.

To decrease the area penalty due to the limited amount of cells in the DARE library, typical designs for space were investigated and much-used core cells were identified as valuable additions to the library. With those cells added, the number of cells in the DARE library is still much lower than that of a commercial library.

Many applications needing memories, a single-port SRAM compiler has been added to the design kit. A PLL cell (situated in an IO cell) has also been added. Other I/O pad options with improved ESD performance have been designed including an LVDS driver and an LVDS receiver as well as several pull-up and pull-down options and a few 5 Volt tolerant and Cold Spare I/Os.

Flip-flops resistant to radiation induced bit-flips were also added to the DARE library, but have only been included in the test-chip, and not the DROM (schedule development constraints). More information on the rad-hard flip-flops and the test-chip design and radiation tests can be found in the relevant report.

The maximum achievable gate density with the DARE library for the UMC (United Microelectronics Corporation) 180 nm CMOS 6-layer metal technology is 25 kgates/mm^2

Two ASICs have been developed using the DARE library:

- Test chip: “Die_Hard”
- Telecom application ASIC : “DROM”

5. TEST VEHICLE DEVELOPMENT

Using the final enhanced DARE library a test-chip was designed and manufactured to test and characterize DARE cells individually.

This chip includes:

- 78 core cells, including SEU hardened flip-flops using HIT cells
- 34 I/O (including LVDS related cells, 5V tolerant and Cold Spare I/O)
- 3 Rams
- 1 PLL
- Stand-Alone ESD test structures
- L&W transistor arrays and different field capacitors (not measured)

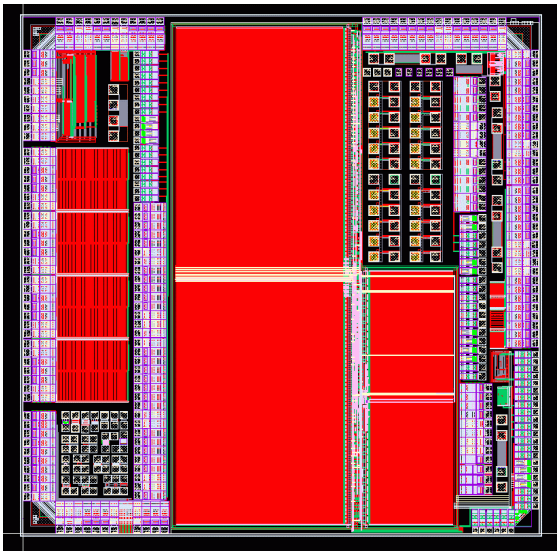

Figure 2 DIE HARD test-chip layout

Test chip validation results.

All measurements have been subdivided into four main parts:

- Functional test: all library cells have been functionally tested. This test has been performed using digital test equipment.
- Timing checks
- Parametrical test
- ESD test

All these tests have given good results, coherent with simulation results, except for a large RAM and the PLL that was not fully functional. The reasons have been understood now and a correction will be possible in the next phase. For the RAM (speed limitation and the big RAM functionality), further investigation is still necessary.

A fifth group of tests has been performed, and is described in a following chapter: Radiation tests.

6. DROM ASIC DEVELOPMENT

Using the final enhanced DARE library, a telecommunication ASIC (Application Specific Integrated Circuit) called DROM (an acronym for Demultiplexer-ROuter-Multiplexer) was designed to validate the functionality, the design methodology and the radiation hardness of the library.

DROM is a telecommunication application ASIC performing a function dedicated to a bent-pipe processor. It has the following main features:

- a system clock frequency of 105 MHz,
- 4 436 000 transistors,
- 263 signal pins,
- a total of 438 pins including power supplies, LVDS inputs and outputs,
- 1.8 V supply for core,
- 3.3 V for I/O.

The ASIC was developed using a classical industrial flow for deep sub-micron chips, using state of the art tools (static timing analysis, formal proof…) with a specific emphasis on physical implementation (Floorplan Manager from Synopsys). In deep sub-micron technologies, the delays due to the wiring become more important than the ones due to the active structures. This is why custom wire-load models must be applied in order to properly meet all timing constraints. Figure 3 shows the layout of DROM. The design flow that has been used is shown in Figure 4.

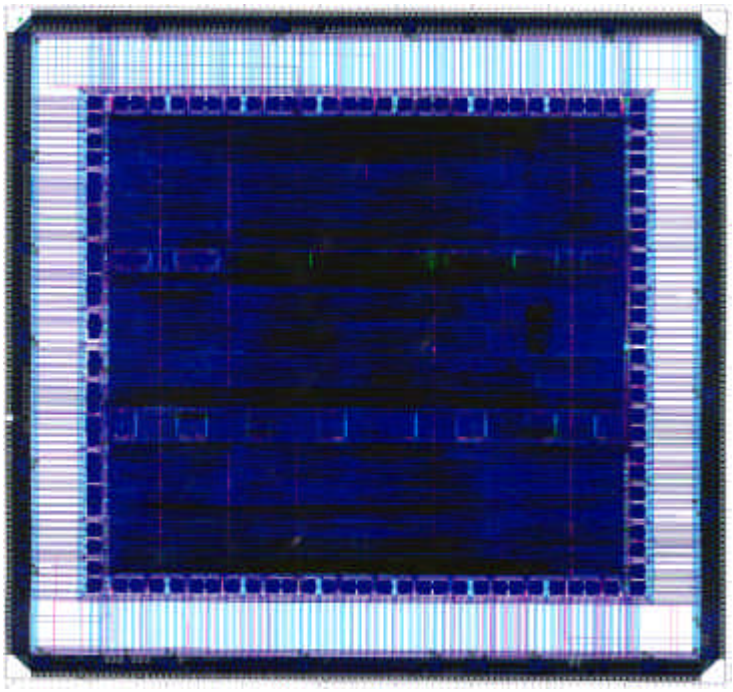

Figure 3: DROM ASIC Layout

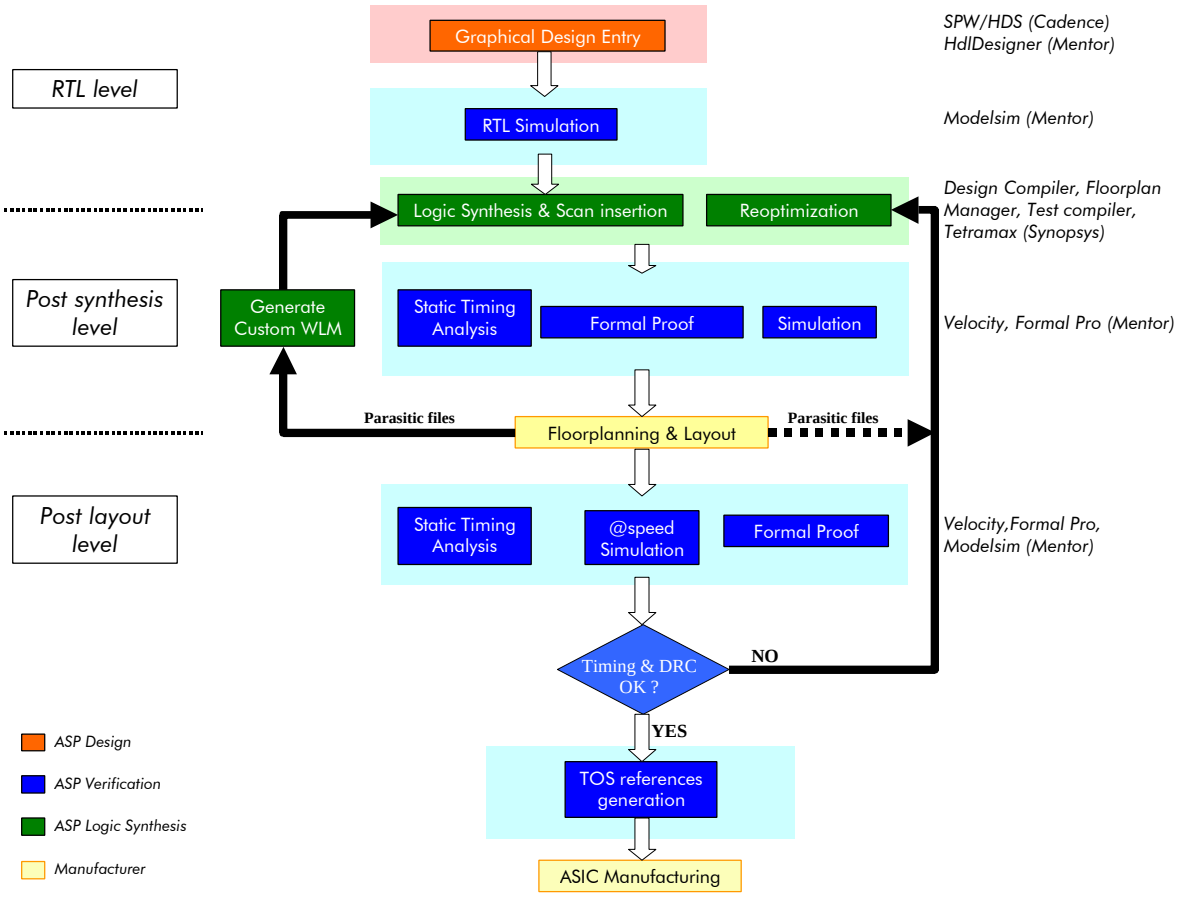

Figure 4: DROM ASIC Design flow

This DSM design flow requires several iterations between layout team and logic design team for timing convergence. In our case, three iterations were necessary to proceed to timing closure, which very reasonable in DSM designs.

DROM functional tests results

The DROM ASIC has been first tested on automatic test equipment, and then, once provided to Alcatel, it has been tested functionally on an operational board, according to test plan.

All tests demonstrated a full spec chip functionality and performance as expected from simulation results.

7. RADIATION TESTS RESULTS

7.1 TEST CHIP RADIATION TEST RESULTS

The radiation tests performed on the test-chip have demonstrated that:

- No SEL occurred
- The Hit cell is not sensitive to SEU
- The sensitivity of non-radiation hardened flip-flops is rather low as shown in the next table.

Type of Registers	Initial Pattern	SEU Rate # / (cell.day)
SDFF	0	$3.8\ 10^{-8}$
	1	$2.4\ 10^{-7}$
LATCH	0	$2\ 10^{-7}$
	1	$8\ 10^{-9}$

Table 1: SEU Rate for Geostationary Orbit on the sensitive Registers

7.2 DROM ASIC RADIATION TESTS RESULTS

The DROM ASIC is highly complex, has a large I/O count, and operates at a high clock frequency: that is why evaluating the radiation effects affecting its performance is challenging.

The full functional and timing evaluation of the complex DROM ASIC at the rated clock frequency necessitates the use of high performance automated test equipment. Such equipment is not available at the irradiation site. Instead an adapted "design for test" approach has been used, during the ASIC architectural study phase. Three test configurations were selected: Functional, RAM BIST (Random Access Memory Built-In Self Test) and SCAN.

7.2.1 Total dose

The test was performed with the samples biased in self-test mode during irradiation.

The ^{60}Co source of the CERT ONERA at Toulouse, France was used. 10 samples plus 1 control sample were used.

The irradiation steps were 0, 50, 70 and 100 krad (Si) at Low Dose Rate (between 36 rad (Si)/h and 360 rad (Si)/h) and 200, 500, 700 and 1 Mrad (Si) at high dose rate. Following the final post irradiation electrical characterisation, two biased annealing steps were applied: the first one at room temperature during 24 hours and the second one at 100°C during 168 hours.

Results:

- At 1 Mrad (Si), all the functional tests passed without any failure.
- No drift on the I_{CC} parameter was reported up to 1 Mrad (Si).

This demonstrates that the design techniques used to harden the cells based on enclosed transistors and guard bands are very efficient.

7.2.2 Single event effects

To characterise the sensitivity of an ASIC to Single Event Effects, it is necessary to have the device working in the nominal conditions, and to detect possible internal state changes during irradiation exposure. More globally, the objective was to detect any effect due to heavy ions exposure such as SEL (Single Event Latch-up), SEFI (Single Event Failure Interrupt), SEU (Single Event Upset).

Results:

- No sensitivity of the ASIC to Single Event Latchup (SEL), Single Event Hard Errors (SHE) and Single Event Functional Interrupt (SEFI).
- Only Single Event Upsets (SEU) were observed on basic cells: on SRAM cells in BIST test, and on D-Flip-Flops in SCAN test.

The results are summarised in Table I and are presented in terms of SEU rates with the number of events per cell and per day.

Type of Program	Total Number of measured cells	SEU Rate 1 / (cell-day)
SCAN0	3075	$6\ 10^{-7}$
SCAN1	3075	$7\ 10^{-7}$
BIST1	18432	$1.2\ 10^{-6}$
BIST2 (with EDAC)	20480	$2\ 10^{-7}$

Table 2: SEU rates for a geostationary orbit

8. DARE PERFORMANCES COMPARISON

The objective of this work was to compare DARE based circuit performances with several other library-technologies. These comparisons have been made for several functions:

- Basic cells (nand/nor/…)
- Complex functions:
  * Operators (various adders, multipliers)
  * Functional block (100 k gates range)
  * DROM Asic,

And at different levels:

- Analogue simulation
- Digital pre-layout
- Digital post-layout
- Prototypes.

We had to consider the variety of parameters that must be taken into account to perform these evaluations, the different levels of available information, the different design steps that were reached and finally the interpolation/extrapolation some times required to get comparable values. All these various constraints require being very careful when comparing results and drawing conclusions.

8.1 BASIC CELL LEVEL COMPARISON

A comparison has been carried out between a set of DARE cells and their counterparts from a commercial library for the same technology.

For the selected set of cells we can say that DARE delay and transition time values approximate those of the commercial library cells rather well, in spite of the (more than) doubled load capacitance for the DARE library. This is largely explained by the DARE output transistor widths being 1.6-2.3 times larger than the transistor widths in the commercial standard cells, which has a compensating effect.

Considering power consumption, it is 2.2-2.3 times higher for the DARE selection.

8.2 COMPLEX FUNCTIONS COMPARISON

The following table will present the relative behaviour of several technologies versus the three main parameters:

- area,
- timing,
- power.

The relative behaviour is obtained by normalisation of the results versus a reference that is a standard cell 0.18μm library/technology, non-European. We have included in this table 2 technologies that have not been evaluated in the frame of the present contract: 0.25 and 0.35μm standard cell. For these technologies, the factors that are in the table are the scaling factors that

are found in the literature and commonly admitted by silicon manufacturers corresponding to technology shrinks.

	Area	Timing	Power
0.18 µm non European, commercial	1	1	1
0.18 µm European, commercial	0,9	1,3	1
0.18 µm UMC DARE	3	1,06	2,3
0.25 µm	2	1,3	3
0.35 µm	4	1,69	9
0.35 µm Radiation Tolerant gate array	7,5	2,58	9,2

Table 3: library & technology comparison

8.3 CONCLUSION

Taking into account the difficulty to perform a true and fair comparison, it was our objective to extract the global tendency and the average figures that will allow making a statement on the performance of the DARE library, with sufficient background to be validated and correlated.
This has been the case, and leads to the following conclusion:

A DARE based design in 0.18µm will be in average:

- 3 times bigger than its equivalent commercial library,
- the same (slightly slower) in terms of speed to its equivalent commercial library,
- 2,3 times more power consuming than its equivalent commercial library.

This situates the 0.18µm DARE library almost one technology generation behind its commercial equivalent, and corresponds to the initial expectations with a rather good surprise for the speed performances.

It is also worth to note (cf. radiation test report) that the DARE library is really hardened, and some improvement could certainly be made to release hardening versus area and power improvement.

9. QA APPROACH

The aim of this work package was to identify critical items to deal with in the frame of flight models procurement from commercial sub-micron technology manufacturing and third part assembly and test.

Items developed in this activity are:

- a summary of quality assurance requirements applied to Asic procurements,
- a description of commercial flow with identification of difficulties, risks and proposition of risk mitigation solutions,
- some 100% and sampling test flows to be applied to FM and test structures,
- a list of open items that can lead to further analysis or studies.

First issue of document was a proposition of criteria to be used for selection of technology, assembly and test houses. Some screening test and lot acceptance tests were proposed. It was decided to update the document in order to be closest to Hirel standard flow and to introduce DROM experience when available.

Economical aspects lead to multi project wafer (MPW) solutions. As in that type of procurement, many entities are involved, it is important to define the responsibility of each site. It is preferable that the entity in charge of MPW is responsible for assembly and test of FM.
Specific care should be applied to prototypes validation in term of yield estimation, assembly and test set-up debug.
Wafer control flow is proposed and alternative solutions are identified if some tests are not performed. As traceability data are not as complete as in Hirel system, Test Structure definition and use is detailed. These Tests Structures can be used to check if there is no major technological evolution and to make some lot-to-lot reliability validation.

Finally, items to be more developed in future studies are listed in order to secure FM procurement from a commercial Silicon manufacturer such as detailed definition of test structures, Assembly & Test House evaluation and management, fixed configurations of die versus package in order to save time and money for new developments.

10. FUTURE ACTIVITIES

Several points have been identified that should be tackled in future contracts. Some of them can be considered as classical follow-on or complementary tasks, and some others are more important since they impact on the viability of the approach.

10.1 FOLLOW-ON TYPE ACTIVITIES:

Library aspects. The library shall be improved with new cells (e.g. Scan HIT cells, Dual Port RAM), correcting the out-of-specification actual cells (e.g. PLL & large SRAM), adding new features such as cold sparing. Analyzing ways to reduce power consumption shall also be an important goal.
Design kit. It will be interesting to build a true design kit with all classical associated tools and documentation (e.g. Design manual).
Radiation aspects. It would be interesting to proceed to some radiation tests at transistor level, aiming at defining the capability for mixed designs (analogue/digital).

10.2 VIABILITY TYPE ACTIVITIES

Library portability. The portability of the library is of utmost importance if we want to be fully independent of a given manufacturer/technology and if we want to follow the commercial technology trends, thereby taking advantage of the most up-to-date performances.
Industrialisation process. In the frame of the present project we have demonstrated both the capability of hardening a technology only by means of the library, and the capability of developing a fully functional ASIC based upon this library. We have also settled the basis for a reflection on packaging, testing, procuring the chips. But providing an ASIC for on board satellite equipment requires a full procurement flow validation, thereby bringing confidence in the new approach.

This point is really critical since it will allow or not the procurement for flight models.

11. CONCLUSION

It has been practically demonstrated during this exercise that a library (DARE) could be developed in order to harden a "normal" commercial library versus radiation behaviour (Total Dose, SEU, and SEL). This has been proven through the validation radiation tests that have been performed on both test chip and complex ASIC.

It has been demonstrated that an entire complex ASIC could be developed using this library and that this ASIC has been fully functional at first run, fulfilling expected performances.

It has been demonstrated that the performances of DARE library are comparable to its a fas orrfor3), which waatioeur (Total
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