

THE DESIGN AGAINST RADIATION EFFECTS (DARE) LIBRARY

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Abstract— This paper describes the first use of a Radiation Hardened by Design (DARE: Design Against Radiation Effects) library for the UMC 180 nm CMOS 6-layer metal technology in a telecom ASIC. An innovative adapted “design for test” approach has been used to allow the evaluation of the behavior of this ASIC under radiation. Radiation tests results and conclusions on future use of this library are also presented.

I. INTRODUCTION

Many foundries with radiation-hard technologies have left the market due to reduced demand by military and aerospace customers and lack of commercially interesting volumes. The DARE development, performed in the framework of an ESA (European Space Agency) Technology and Research Programme contract [2], is aiming at providing an alternative solution to the one offered by the limited number of foundries that can currently manufacture radiation-hard ASICs. The DARE library is meant to be used in combination with commercial foundries’ technology, and seeks foundry-independence while providing competitive, high-performance, low-power, low mass solutions for components to be used in harsh radiation environments. In [1] it was shown that the concept of improving radiation performance of components manufactured in commercial deep sub-micron technologies through the application of special layout techniques [3] [4] is valid.

To decrease the area penalty due to the limited amount of cells in the DARE library, typical designs for space were investigated and much-used core cells were identified as valuable additions to the library. With those cells added, the number of cells in the DARE library is still much lower than that of a commercial library.

Many applications needing memories, a single-port SRAM compiler has been added to the design kit. A PLL cell (situated in an IO cell) has also been added. Other I/O pad options with improved ESD performance have been designed, including an LVDS driver and receiver as well as several pull-up and pull-down options.

Using the final enhanced DARE library, a telecommunication ASIC (Application Specific Integrated Circuit) called DROM (an acronym for Demultiplexer-ROuter-Multiplexer) was designed to validate the functionality, the design methodology and the radiation hardness of the library. A test-chip was also designed and manufactured to test and characterize DARE cells individually. Flip-flops resistant to radiation induced bit-flips were also added to the DARE library, but have only been included in the test-chip, and not the DROM. More

information on the rad-hard flip-flops and the test-chip design and radiation tests can be found in [5].

II. AREA SPEED AND POWER TRADE-OFFS

The maximum achievable gate density with the DARE library for the UMC (United Microelectronics Corporation) 180 nm CMOS 6-layer metal technology is 25 k gates/mm². For example, the NAND2 gate area is 39.45 μm². One bit of RAM takes up 28.98 μm². Several exercises have been carried out to evaluate the DARE library performance versus its functionally equivalent commercial (i.e. not radiation-hardened) 0.18 μm library.

The area penalty factor between commercial non-hardened cells and DARE cells with the same functionality ranges from 2 to 4. For the DROM core, the penalty factor obtained is 3. The area penalty for the full DROM using in-line pads is 2 (Cf. Figure 1).

There is no speed penalty factor with the DARE library. For DROM the speed that has been achieved is indeed equivalent to the one with a commercial 0.18 μm library.

Power consumption of DARE cells is 2.2 times higher than that of comparable cells in a commercial library. This figure takes into account internal and switching power.

III. DROM: FIRST ASIC DONE WITH DARE

DROM is a telecommunication application ASIC performing a function dedicated to a bent-pipe processor. It has the following main features: a complexity of 1,5 million equivalent gates, including RAMs, a system clock frequency of 105 MHz, 263 signal pins, a total of 438 pins including power supplies, LVDS inputs and outputs, 1.8 V supply for core, 3.3 V for I/O.

The ASIC was developed using a classical industrial flow for deep sub-micron chips, using state of the art tools (static timing analysis, formal proof...) with a specific emphasis on physical implementation (Floorplan Manager from Synopsys). In deep sub-micron technologies, the delays due to the wiring become more important than the ones due to the active structures. This is why custom wire-load models must be applied in order to properly meet all timing constraints.

The objective was to demonstrate the capability to design a large, functionally demanding and complex ASIC with the newly developed DARE library, to reach the required technical performance and to perform radiation testing. All these objectives have been successfully reached, since the ASIC is fully functional at the targeted performance.

The radiation test results are presented in the following chapter.

IV. RADIATION TEST APPROACH

As the name implies, application specific integrated circuits (ASICs) are developed to perform a specific function in a system with a great deal of design requirements inputs from the system developer. Because the DROM ASIC is highly complex, has a large I/O count, and operates at a high clock frequency, evaluating the radiation effects affecting its performance is challenging. High performance, a large pin count and automated test equipment is required to store all the test vectors and exercise the ASIC at an operational clock frequency.

A. Total Dose

Total ionizing dose induced failures in ASICs are the result of radiation induced changes in transistor characteristics and the creation of leakage paths. Leakage paths can drastically increase the supply current or alter the information stored as charge on critical nodes, or both. These changes are produced by a combination of mechanisms involving charge trapping and interface state generation in gate and field oxides. Radiation-induced leakage under the field oxide, around the transistor edges and through the transistors themselves will be observable in the supply current. This is why the supply current is measured prior to the irradiation and after each irradiation step.

The full functional and timing evaluation of the complex DROM ASIC at the rated clock frequency necessitates the use of high performance automated test equipment. That equipment was not available at the irradiation site. Instead an adapted “design for test” approach has been used. Three test configurations were selected: Functional, RAM BIST (Random Access Memory Built-In Self Test) and SCAN. SCAN, with its associated ATPG (Automatic Test Pattern Generation) and RAM BIST are the part of the production test strategy selected to validate the correct manufacturing of DROM. These functions have been adapted, as described hereafter, to facilitate the radiation tests.

1) Description of Functional Test

A self-test mode is designed to activate DROM’s functional behaviour without any external intervention, thus simplifying the physical setup of the tests. The self-test internally creates functionally representative input data. A checksum is calculated periodically by accumulation of intermediate data. Data coming from the input interface and main constitutive blocks is used to calculate 8 checksums on a serial bit associated with a synchronisation signal - both primary outputs. Each checksum is compared with the previous frame accumulation and delivers a flag as primary output. The internal data memorised in Read Only Memory (synthesized, not macros from the library), with 1024 words of 12 bits, correspond to a specific carrier waveform (Self-test 1).

2) Description of RAM BIST Test

The integrity of the RAMS is checked with BIST structures based on the Marinescu 11N algorithm that ensures a very high fault coverage on memory blocks. The BIST structures are composed of a test pattern generator that writes predefined data in memories and a data comparator for data read out of each RAM, delivering a ‘test_nok’ signal. This signal is set to 1 when the data read from RAM are not identical to the data written by the BIST generator.

In order to test the RAM sensitivity under radiation, two memory areas representative of the global complexity were selected. The first one (BIST 1) tests:

- 8 SRAMs of 32 words x 48 bits
- 4 SRAMs of 32 words x 40 bits
- 1 SRAM of 64 words x 16 bits

The second one (BIST 2) tests:

- 8 SRAMs of 32 words x 56 bits
- 4 SRAMs of 32 words x 40 bits
- 1 SRAM of 64 words x 16 bits

The SRAMs with 32 words x 56 bits in BIST 2 are equivalent to the SRAMs of 32 words x 48 bits, surrounded by EDAC structures, in BIST 1.

3) Description of SCAN test

When activating the scan mode, all the flip-flops of the design are organized in “parallel load/serial shift” chains of registers. In this mode, RAM access is inhibited by disabling both the clock and chip select signals. The RAMs are bypassed by putting the input data directly onto the RAM outputs. This SCAN implementation enables exhaustive check of all the chip logic ensuring a fault coverage of 97.64%, excluding faults inside RAMs. 91 Scan chains are implemented in the ASIC.

For the radiation tests, a selection of 8 carefully chosen chains is stimulated. After initialisation of the scan chains, the register inputs of all chains are set to a static value, either “0” or “1”. The test performed with input value to 0 is called SCAN0 and the one with input value equal to 1 is called SCAN1. Bit flips caused by radiation would be then very easy to trace once the contents of the scan chains are shifted out.

B. Single Event Effects

To characterise the sensitivity of an ASIC to Single Event Effects, it is necessary to have the device working in the nominal conditions, and to detect possible internal state changes during irradiation exposure. For this aspect we decided to use the same self-tests as described for Total Dose test.

In addition, the following errors can occur on the DROM during the tests.

The DROM can be sensitive to Single Event Latchup (SEL) because it is manufactured with CMOS technology [6]. SEL can be a destructive effect. The SEL is detected and occurrences are counted by a special power control circuitry (delatcher) that prevents the destruction of the device. The high-current condition is detected and maintained for a certain short time, then the delatcher shuts down the power for a preset time interval. The current trigger and the current limit could be programmed separately. After power is shut

down, it must be applied again to the device. A scope records the shape of the current when an increase of bias current is observed.

DROM has many digital cells that are sensitive to Single Event Upsets (SEU) [7]: the flip-flops and memory (RAM) arrays. The tests on Flips Flops and SRAMs are performed by the already described SCAN and RAM BIST tests programs respectively.

This test bed allows to detect also SEFI (Single Event Functional Interrupt) and stuck bits in the SRAMs.

If there is an upset in the control logic of a RAM, the device can show an unusual operation and we can conclude we are observing a SEFI. Among these errors, we can encounter reading or writing to the incorrect address or a functional interrupt. The latter is usually identified when an important part of the memory cells is simultaneously corrupted. By comparing abnormal bias current with its associated normal value, we can often find the initial sign of a SEFI [8] [9]. In some cases, these errors require a power cycle to restore unperturbed conditions. Then it is considered as a permanent SEFI.

Heavy ions can also induce stuck bits, causing the memory cell not to be read out correctly after programming [10] [11]. Stuck bits in memory elements are believed to occur from either single-event gate rupture or microdose [11] [12].

C. Description of Test Bed

The test bed is shown in Figure 2. The same test bed was used for both Total Dose and SEE tests. The control of the different operation cycles inside DROM and the analysis of the collected output data, in comparison with the references, is performed with a data acquisition board using an FPGA.

Daughter boards were specifically designed for the DROM ASIC. The FPGA is initialised by software running on a computer. The goal of the software is to record the errors detected by the acquisition board and perform the acquisition of the scope curves.

D. Radiation Tests Facilities and Setup

1) Total Ionizing Dose tests

The test was performed with the samples biased in self-test mode during irradiation.

The ^{60}Co source of the CERT ONERA at Toulouse, France was used.

10 samples plus 1 control sample were used.

The irradiation steps were 0, 50, 70 and 100 krad(Si) at Low Dose Rate (between 36 rad(Si)/h and 360 rad(Si)/h) and 200, 500, 700 and 1 Mrad(Si) at high dose rate. Following the final post irradiation electrical characterization, two biased annealing steps were applied. The first one at room temperature during 24 hours and the second one at 100°C during 168 hours.

2) SEE tests

The Heavy ions test was performed at the Cyclotron Research Center of the Université Catholique de Louvain-la Neuve, Belgium. Table I describes the characteristics of the available ions.

TABLE I: ION COCKTAIL AT UCL

Ion	Energy (Mev)	LET (Mev.cm ² /mg)	Range (μm)
¹⁰ B	41	1.70	80
¹⁵ N	62	2.97	64
²⁰ Ne	78	5.85	45
⁴⁰ Ar	150	14.1	42
⁸⁴ Kr	316	34	43
¹³² Xe	459	55.9	43

V. RADIATION TEST RESULTS

A. Total Dose

At 1 Mrad(Si), all the functional tests passed without any failure.

No drift on the I_{CC} parameter was reported up to 1 Mrad (Si).

We can conclude that the total dose behavior up to 1 Mrad (Si) is very good.

This demonstrates that the design techniques used to harden the cells based on enclosed transistors and guard bands are very efficient.

B. Single Event Effects

A very important result is that heavy ion tests demonstrated DROM is not sensitive to Single Event Latchup (SEL), Single Event Hard Errors (SHE) and Single Event Functional Interrupt (SEFI).

Only Single Event Upsets (SEU) were observed on basic cells: on SRAM cells in BIST test, and on D-Flip-Flops in SCAN test.

An important factor is the number of events that will occur during a satellite's lifetime. In order to perform the rate calculations, we need the SEU cross section. For this reason, we represent the cross section curves as function of LET (Linear Energy Transfer) for all the tests we performed. For digital parts, the SEU cross section, σ , is defined as

$$\sigma = N / (F \cdot \cos\theta)$$

Where N is the number of upsets, F is the fluence (1/cm²) and $\cos\theta$ is the beam angle factor. The cross section measurement is performed for different values of LET.

First of all, the sensitivity of the flip-flops in the scan chains is the same with the test performed with input values set to 0 (SCAN0) as the test with input values equal to 1 (SCAN1), as presented in Figure 3.

As expected, the device cross-sections measured with BIST 1 and 2 programs (see Figure 4) demonstrate that the SRAM with EDAC (BIST 2) is less sensitive than the other SRAM (BIST 1), because there is a protection due to the automatic internal correction of the errors implemented by the EDAC.

The impact of SEU in flip-flops and the SRAM cells can be observed during the functional Self-test 1 program. The errors reported are transient perturbations from which the ASIC recovers after a few clock cycles. The detailed cross-section curves as function of LET during self-test 1 are presented in Figure 5.

VI. INTERPRETING THE RADIATION TEST RESULTS

The Total Dose results are very good. A radiation hardness level of 1 Mrad(Si) is far beyond the usual space requirements level of 10 – 100 krad for a geostationary orbit. For a better comparison of sensitivity to Single Event Effects during a geostationary mission, we performed the upset rate calculations for each test configuration (SCAN, BIST and self-test).

The parameters used for these calculations are the following. The cosmic ray environment is calculated with CREME (Cosmic Ray Effects on Micro Electronics) in terms of the integral LET spectrum for an interplanetary weather index of M=3. This integral LET spectrum includes all ion species from Hydrogen (Z=1) to Uranium (Z=92). In addition, this LET spectrum does not take into account any “magnetic storms” but includes the earth-shadow effect on the spacecraft. The shielding around the silicon target is assumed to be 1g/cm. The trapped proton environment is described using the differential energy spectrum. The SEU rate calculation is realized using Weibull FIT and PROFIT [13].

The results are summarized in Table II and are presented in terms of SEU rates with the number of events per cell and per day.

TABLE II: SEU RATES FOR A GEOSTATIONARY ORBIT

Type of Program	Total Number of measured cells	SEU Rate 1 / (cell-day)
SCAN0	3075	$6 \cdot 10^{-7}$
SCAN1	3075	$7 \cdot 10^{-7}$
BIST1	18432	$1.2 \cdot 10^{-6}$
BIST2 (with EDAC)	20480	$2 \cdot 10^{-7}$

The SEU rate is lower for BIST2 than for BIST1. This can be explained because in BIST 2 there are 8 SRAM 32 words x 48 bits surrounded by EDAC structures.

The SEU rate observed on D Flip Flops and SRAM cells are low (higher for SRAM cells due to higher level of integration) and are in the same order of magnitude in comparison with other CMOS ASIC technologies.

Finally, this low level of sensitivity on the basic memory cells induces an error rate on the functional test (self-test1) of 0.29 transient errors per day.

VII. CONCLUSIONS

In this paper, we describe the first use of a Radiation Hardened by Design (DARE: Design Against Radiation Effects) library for the UMC 180 nm CMOS 6-layer metal technology in a large telecommunication ASIC. An innovative adapted “design for test” approach has been used to allow the evaluation of the sensitivity of this ASIC to Total Dose and Single Event Effects. The radiation test results demonstrate a level of hardness for the Total Dose aspects higher than 1 Mrad(Si). For Single Event Effects, this ASIC is neither sensitive to Single Event Latch-up, Single Event Hard Errors nor Single Event Functional Interrupt. The Single Event Upset sensitivity observed on D Flip Flops and SRAM cells is low. The SEU sensitivity of this ASIC is compatible with in-orbit use for a geostationary mission. Furthermore, the inclusion and validation by means

of the test-chip tests [5] of SEU-resistant flip-flops enhances the SEU robustness that the use of the DARE library can offer.

The project, initiated by ESA and carried out by IMEC and Alcatel Space, has demonstrated that the DARE library provides very good radiation hardness. It has also been demonstrated that the library is suitable for an ASIC design in a classical deep sub-micron design flow.

This gives interesting perspectives for the European space community. Since the radiation hardness obtained is (for TID) far beyond the space requirements, a better compromise between radiation hardening and DARE performance might be possible, improving the area penalty.

The library could also be enhanced in the future with additional cells, and other memory or I/O options.

VIII. ACKNOWLEDGEMENTS

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IX. REFERENCES

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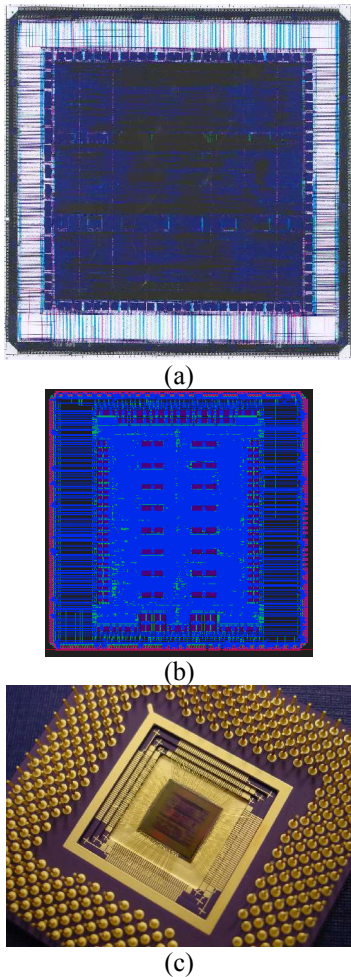


Fig. 1. (a) Layout of the DARE DROM (9.418 x 9.418 mm²) (b) The DROM in a commercial .18 library (6.540 x 6.540 mm²) (c) Picture of the packaged DARE DROM

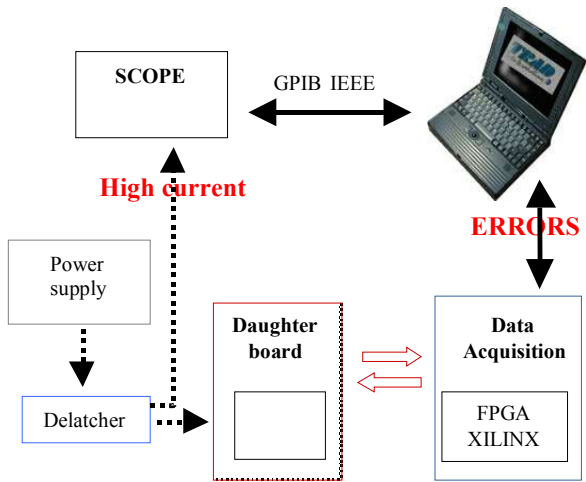


Fig. 2. The DROM test-bed

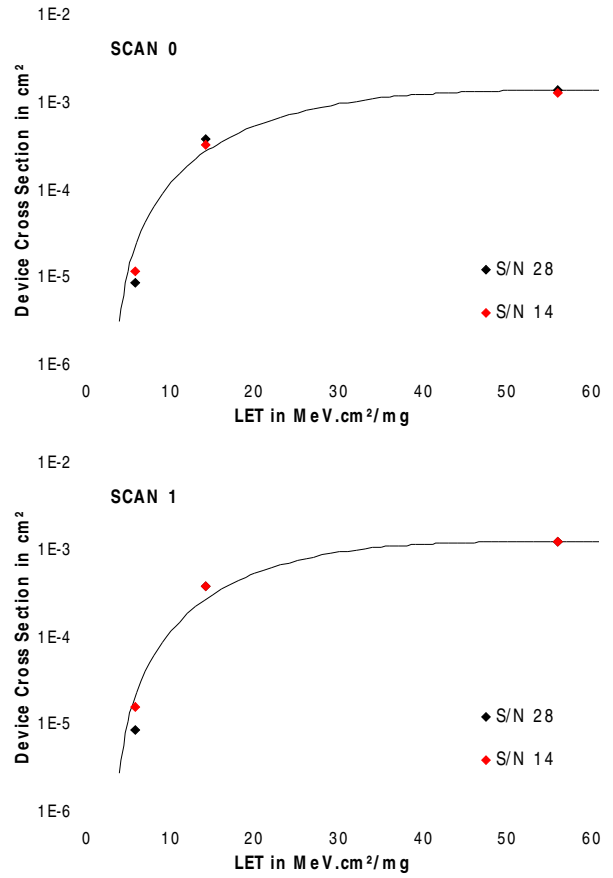


Fig. 3. Device cross section on DROM during SCAN0 and SCAN1 test

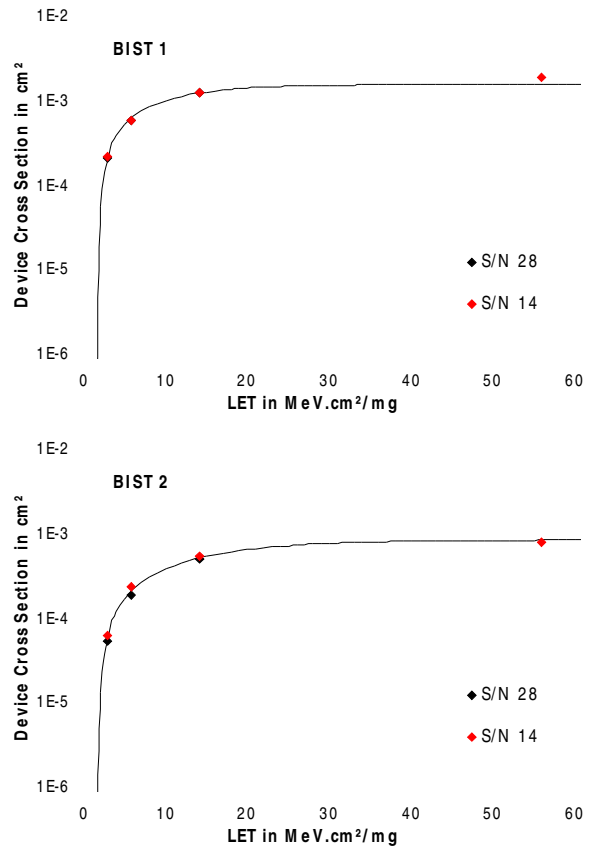


Fig. 4. Device cross section on DROM during BIST1 and BIST2 test

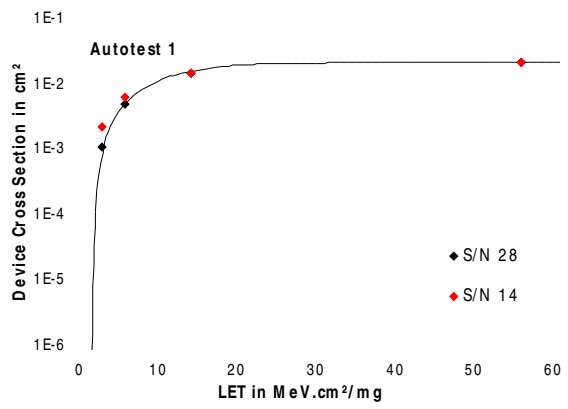


Fig. 5. Device cross section on DROM during functional test