Final Report - GR740 Next Generation Microprocessor Flight Models (NGMP Phase 3)

Final Report

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TABLE OF CONTENTS

1 Introduction 4
1.1 Purpose and Scope 4
1.2 Applicable Documents 4
1.3 Reference Documents 4
2 Abbreviations 4
3 Background and Introduction 5
4 Project Overview 7
4.1 Introduction to the activity 7
4.2 Program of work 8
5 Performed activities 9
5.1 Performed work 9
5.1.1 Overview 9
5.1.2 Task A1 - Wafer Manufacturing and Probing 11
5.1.3 Task A2 - Prototype Assembly and Test 11
5.1.4 Task A3 - Functional and Radiation (Re-)Validation 12
5.1.5 Task A4 - Qualification Preparation 12
5.1.6 Task A5 - Flight Part Assembly and Qualification Test Boards 13
5.1.7 Task B1 - Qualification Testing 13
5.1.8 Task B2 - Certification and Commercialisation 14
5.1.9 Summary 14
5.2 Delivered outputs 14
5.3 External presentations 17
6 Achieved results 18
6.1 Developed product 18
6.2 Test and Performance summary 20
6.3 Power consumption 20

6.4 Radiation Tolerance 20
6.5 Production line 21
6.6 Problems experienced 21
6.6.1 Package development 21
6.6.2 Over Pad metallization 22
6.6.3 Wire bonding 22
6.6.4 Selection of column type for CCGA package 22
6.7 Known anomalies 23
7 Lessons Learned 23
8 Further Evolutions 23
8.1 GR740 PBGA 23
8.2 GR765 24
9 Conclusion 25

1 INTRODUCTION

1.1 Purpose and Scope

This document establishes the Final Report for the activity “GR740 Next Generation Microprocessor Flight Models (NGMP Phase 3)” initiated by the European Space Agency under ESTEC contract 4000122419/17/NL/LF.

The report covers the two subphases 3A and 3B from December 2017 to June 2021.

This document has been developed by Cobham Gaisler AB (Göteborg, Sweden).

1.2 Applicable Documents

The following documents, listed in order of precedence, contain requirements applicable to the contents of the document:

[AD1] MIL-PRF-38535L, December 2018

[AD2] ESCC 2269000 issue 5, February 2016

[AD3] MIL-STD-883L, September 2019

1.3 Reference Documents

The following documents are referred as they contain relevant information:

[RD1] Draft SMD 5962-21204_w2123 submitted to DLA 2021-06-09

[RD2] DM00677476_iss3, NGMPU CLGA625 CCGA625 QMLV and ESCC delta Evaluation qualification plan, September 2020

2 ABBREVIATIONS

CPU	Central Processing Unit
EDAC	Error Detection And Correction
FPU	Floating Point Unit
GRLIB	Cobham Gaisler's IP core Library
I/O	Input/Output
JTAG	Joint Test Action Group (developer of IEEE Standard 1149.1-1990)
kB	Kilobyte, 103 bytes
KiB	Kibibyte, 210 bytes, unit defined in IEEE 1541-2002
Mb, Mbit	Megabit, 106 bits
MB	Megabyte, 106 bytes
MiB	Mebibyte, 220 bytes, unit defined in IEEE 1541-2002
MIPS	Million of Instructions Per Second

NGMP	Next Generation Microprocessor
PCI	Peripheral Component Interconnect
PLL	Phase Locked Loop
PROM	Programmable Read-Only Memory
RAM	Random Access Memory
RMAP	Remote Memory Access Protocol
SDRAM	Synchronous Dynamic Random Access Memory
SEE	Single Event Effects
SEL/SEU/SET	Single Event Latchup/Upset/Transient
SPARC	Scalable Processor ARChitecture
UART	Universal Asynchronous Receiver/Transmitter

3 BACKGROUND AND INTRODUCTION

The design and validation of the GR740 has been performed in an activity completed 2017, the "NGMP engineering models (product code GR740)" activity initiated by the European Space Agency under ESTEC contract 2000113922/15/NL/LF.

The architecture, features, interfaces and layout resulting from the activity are summarized below. This design is used as input for the qualification and development of a flight model in this activity.

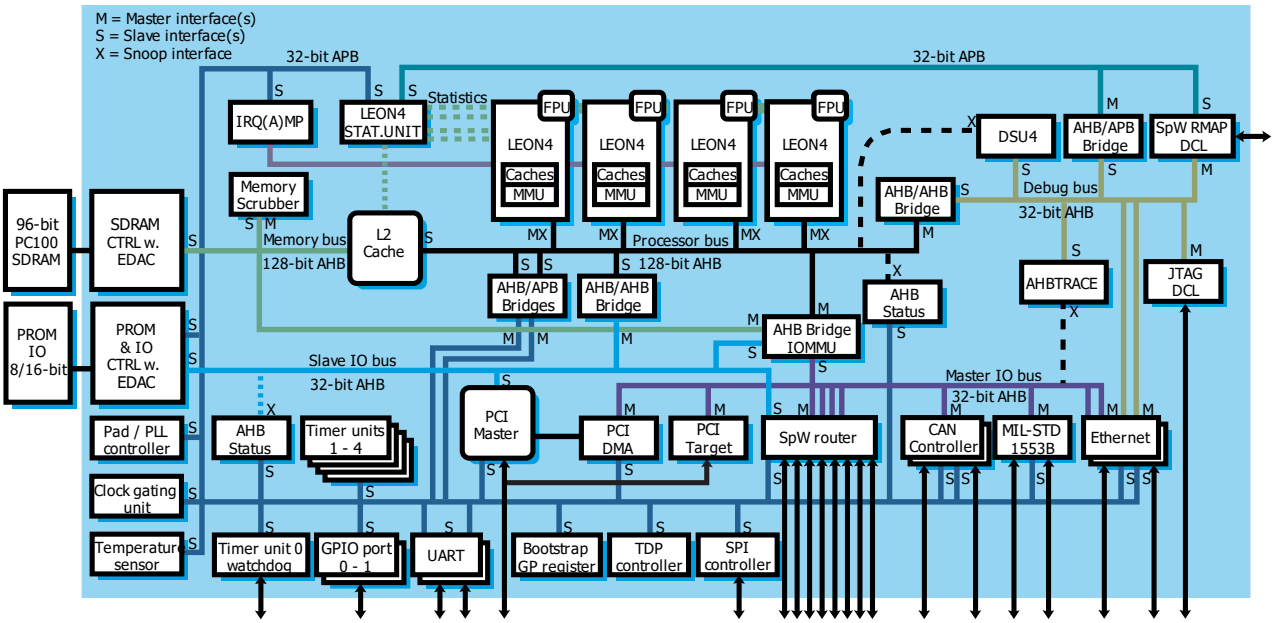


Figure 1 *GR740 architecture*

Features and performance

- Fault-Tolerant Quad-processor SPARC V8 integer unit with 7-stage pipeline, 8 register windows, 4x4 KiB instruction and 4x4 KiB data caches.
- Double-precision IEEE-754 FPU (1 FPU/Core)
- 2 MiB Level-2 cache
- 64-bit PC100 SDRAM memory interface with Reed-Solomon EDAC
- 8/16-bit PROM/IO interface with EDAC
- CPU and I/O memory management units
- Multi-processor interrupt controller with support for asymmetric and symmetric multiprocessing
- SpaceWire TDP controller and support for time synchronisation
- Very low power, < 3 W (core typical)
- Performance 1700 DMIPS

Interfaces

- SpaceWire router with 8 SpaceWire links (200 MHz)
- 2x 10/100/1000 Mbit Ethernet interfaces
- 2x MIL-STD-1553B interface
- 2x CAN 2.0 controller interface
- 2x UART, SPI, Timers and watchdog, 16+22 pin GPIO
- PCI Initiator/Target interface
- JTAG

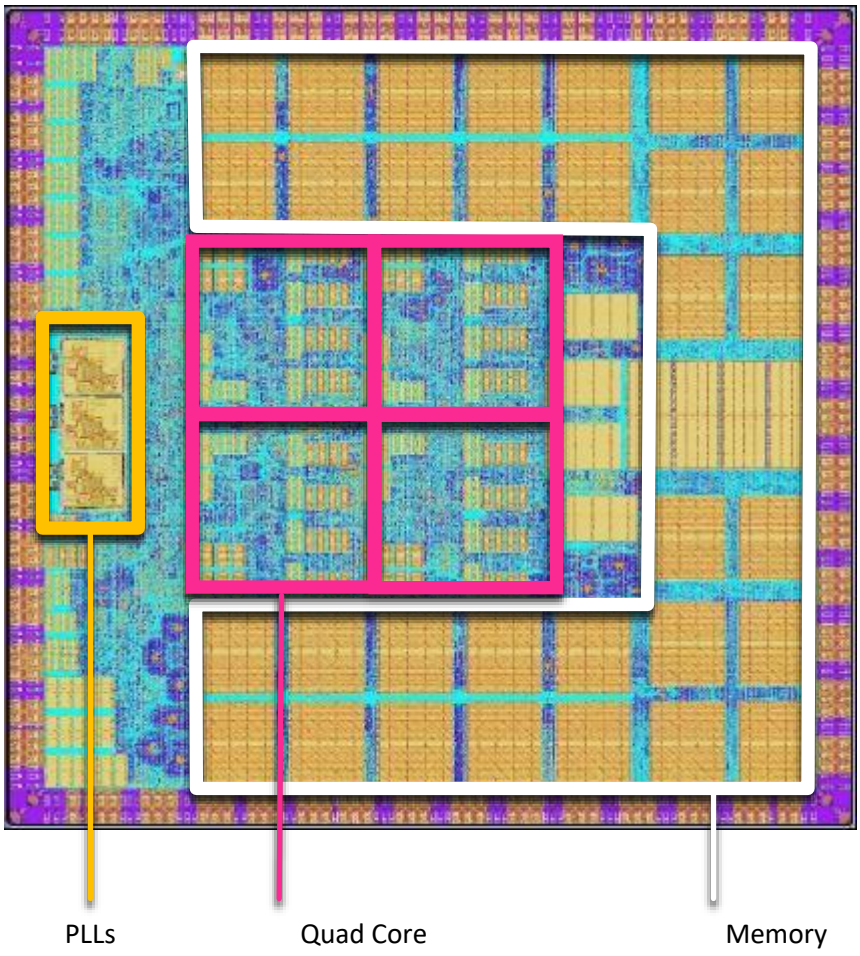


Figure 2 *GR740 layout*

4 PROJECT OVERVIEW

4.1 Introduction to the activity

The aim of Phase 3 of this activity was:

1) To manufacture flight GR740 components (based on the design completed in phase 2)
2) To perform the validation of the flight components (functional and radiation)
3) and to perform the qualification in accordance with QML-V class as per MIL-PRF-38535 [AD1] with a Delta ESCC evaluation based on ESCC2269000 [AD2].

The manufacturing of the flight components was carried out by STMicroelectronics at their Rennes site. This site has already an assembly line that achieved QML-V certification for other products other than GR740.

The screening and qualification plan for the flight components (including the delta ESCC) is described in detail in [RD2]. This plan took advantage of the synergies with other C65SPACE products that ST was qualifying for QML-V.

An overview of the certification process for existing certified suppliers such as ST was given in Deliverable D11 of this project. This process included the submission of:

- A QA plan addressing the new technology,
- A qualification plan for the GR740
- The characterisation data and the qualification test report.
- Results of the reliability assessment
- A standard microcircuit drawing (SMD)

The supply chain setup by ST for the production of the flight components encompasses the following sites and suppliers:

- ST Crolles, responsible for the manufacturing of the GR740 wafers
- ChipBond, responsible for the over pad metallisation of the GR740 dice
- ST Rennes, responsible for the assembly and mechanical screening of the flight parts
- ST Grenoble, responsible for the electrical testing (including wafer sorting), burn-in and HTOL activities.
- Micross Crewe, responsible for the column mounting on CCGA devices.

Some of the qualification tests (RGA , vibrations, salt atmosphere, solderability) were subcontracted by ST to their recognised suppliers. Details are available in Deliverable D11 of this project.

4.2 Program of work

The work was originally scheduled to 27 months, distributed as 9 months for Phase 3A and 18 months for Phase 3B. It was from early in project expected that some overlaps of Phases 3A and 3B would be needed to limit the overall schedule, and as a consequence a kick-off date T1 was defined as the start of phase 3B. There have been no CCNs developed within the activity.

The work related to the two phases 3A and 3B contained seven different tasks:

- Task A1 - Wafer Manufacturing and Probing
- Task A2 - Prototype Assembly and Test
- Task A3 - Functional and Radiation (Re-)Validation
- Task A4 - Qualification Preparation
- Task A5 - Flight Part Assembly and Qualification Test Boards
- Task B1 - Qualification Testing
- Task B2 - Certification and Commercialisation

The activity has included four formal reviews.

Table 1 List of reviews

Event / Delivery	**Related phases and tasks**	**Original date**	**Date**
Kick-Off	N/A	T0	2017-12-08
Validation Readiness Review (VRR)	Phase 3A Tasks A1, A2	T0 + 6 months	2018-06-19
Kick-Off Phase 3B	N/A	T1	2018-06-27
Final Validation Review (FVR)	Phase 3A Tasks A3, A4, A5	T0 + 7 months	2019-04-04
Qualification Readiness Review (QRR)	Phase 3B Task B1	T1 + 8 months (T0 + 15 months)	2021-03-18
Final Acceptance Review (FAR)	Phase 3B Task B2	T1 + 20 months (T0 + 27 months)	2021-06-24

5 PERFORMED ACTIVITIES

5.1 Performed work

5.1.1 Overview

The two phases and their tasks were assigned to work packages shared between Cobham Gaisler and ST as illustrated in the figure below.

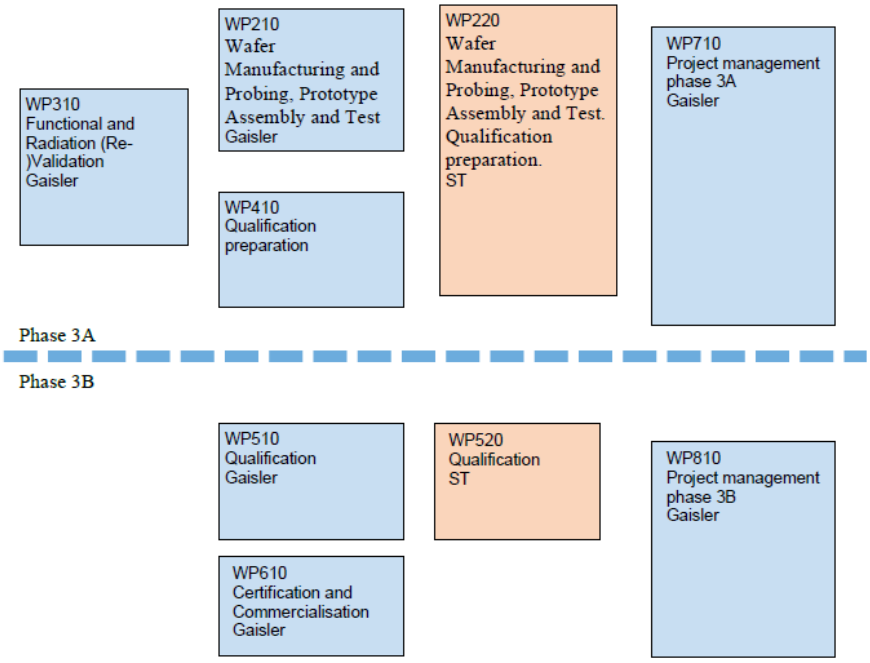


Figure 3 *Work Breakdown Sheet*

There has been a certain overlap of phases, tasks and work packages. The project's progress over time is illustrated as in Figure 4 below. The end date of the activity is assumed, and based on close-out completed within a week after the FAR.

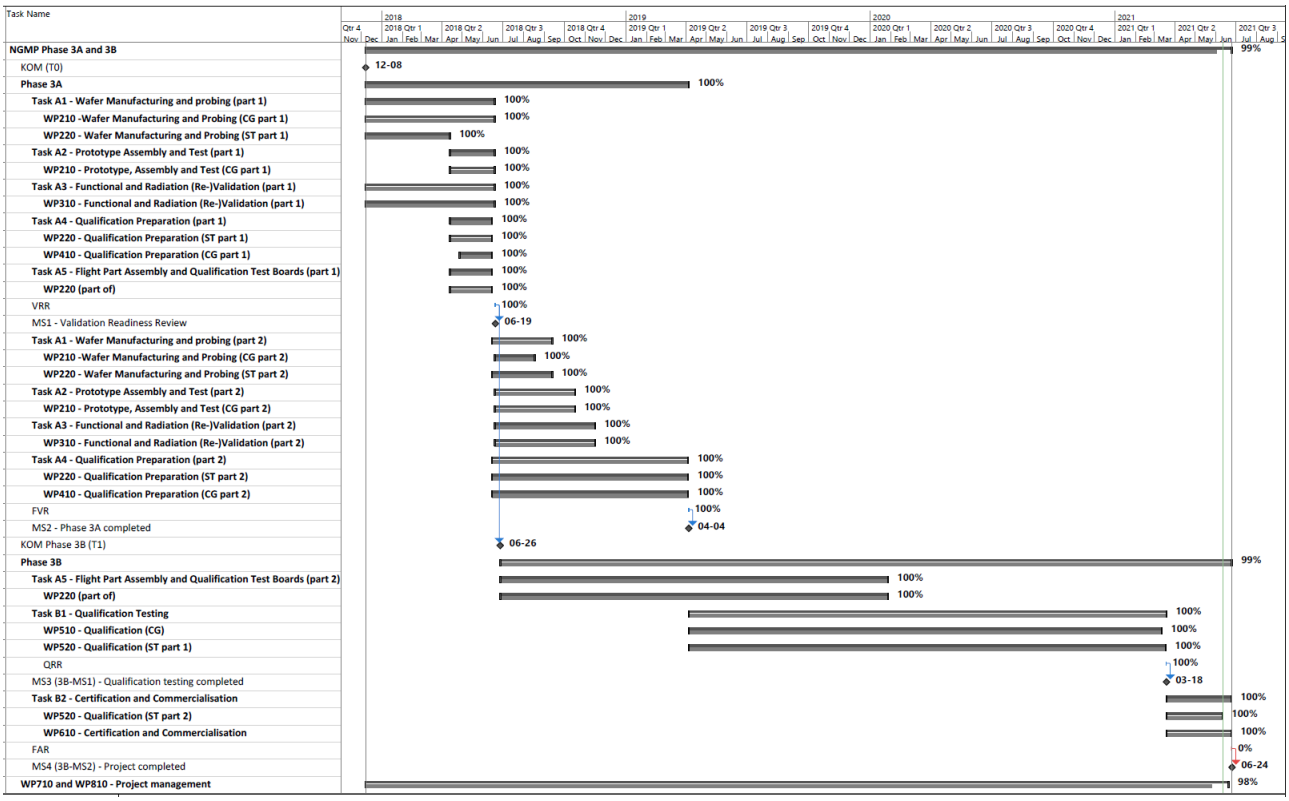


Figure 4 *Activity Overview*

5.1.2 Task A1 - Wafer Manufacturing and Probing

A set of 12 wafers (silicon revision 1), using ST's Rad-Hard 65nm CMOS technology for space applications, were manufactured for the completion of this task by ST Crolles. These wafers successfully completed all WLA (wafer lot acceptance) performed by ST following TM5007 of [AD3]. Over pad metallisation has been applied on all wafers used for the manufacturing of flight components and prototypes samples that require electrical testing over the whole temperature range of the device.

A test program for GR740 wafers (EWS) was developed by STMicroelectronics. All wafers allocated to the production of flight parts were tested with this program and only good dice were allowed into the assembly line (flight components). The details of the content of the EWS program were not released by ST as they consider this part of their 'Know-How'. The impact of EWS on the manufacturing of flight parts was reflected in the yield obtained by ST during the screening of two flight quality batches. Overall, the yield figures were very good.

5.1.3 Task A2 - Prototype Assembly and Test

Numerous assemblies of prototype parts have been completed successfully by ST at the Rennes facilities since 2018. All these samples have used the revised package (revision 1) and cover both the CLGA and CCGA package solutions. All prototype samples have been electrically tested with the

same production test program used for flight parts. The electrical performance of the GR740 has been defined in table IA of the SMD [RD1]. Two fully functional prototype samples were delivered to ESA as part of HW1 (see section 5.2).

In addition to the prototype samples, ST has delivered 'Daisy Chain' samples and mechanical samples, which are used by customers for the qualification of the board mounting process. Daisy chain samples have been delivered to ESA to perform a comparison between IBM type columns and copper wrapped columns from Serma (France).

Electrical testing of the GR740 ceramic product has been mainly performed at the ST site in Grenoble using the load board developed by ST. A second test load board has been manufactured and placed at Synergie CAD facilities in Toulouse. This facility has been used for the electrical testing of irradiated parts (Group E testing). This was necessary due to the time limitations imposed by this type of test (maximum time gap between irradiation and electrical testing of 1 hour).

5.1.4 Task A3 - Functional and Radiation (Re-)Validation

Functional verification of the GR740 (silicon revision 1) were performed on prototype samples with the use of the development boards GR-CPCI-GR740 manufactured by Pender Electronics for this product.

Radiation re-validation focused on the Single Event Effects (SEE) performance of the device under heavy ions. Prototype samples without lid were provided by ST for this task. The complete set of results of the SEE testing were provided in deliverable documents D12 and D13. The data collected demonstrated that the device is Single Event Latch-up immune to an LET of 125 MeV.cm^2/mg (Tj>85ºC and maximum supply voltage). In addition, the overall SEE rate was calculated for the GR740 and shown to be below 0.00001 events per device per day for a standard geosynchronous orbit. The testing performed on the GR740 also showed that the device is immune to functional errors as the result of direct proton ionisation.

Total ionising dose (TID) testing was also completed as part of this task and demonstrated that the GR740 is tolerant to a level of 300 krad(Si). As a result, a radiation assurance level of F has been requested in the SMD for this product.

5.1.5 Task A4 - Qualification Preparation

A first qualification batch was assembled by ST in 2019. However, due to problems during the screening, this batch had to be discarded. However, most of the qualification work planed for the QML-V qualification was completed using samples from this batch. This served as a preparation for the actual qualification work and a validation of the technology. For example, the burn-in boards were validated and used for the screening of the parts. Analysis of the data collected before and after burn-in were analysed and used in the definition of the SMD [RD1]. Mechanical and thermal QCI tests, as defined in groups D3 and D4 of [AD1] were completed without failure (validation of the package solution). A 1000-hour life test, group C, was also completed successfully on 24 samples from this batch (included in the reliability assessment of the technology). Jigs for constant acceleration and vibration testing were also validated.

In addition, ESA performed a constructional analysis on two samples in CLGA package from this batch. No critical issues were identified on these samples.

ESD and electrical latch-up testing of the product was successfully completed as part of task A4. The results of these tests are shown in the table below.

Table 2 ESD and latch-up test results

TEST DESCRIPTION	METHOD	RESULT
ESD HBM	JS-001-2017	2kV
ESD CDM	JS-002-2014	500V
LATCH-UP	JESD78E	PASS

5.1.6 Task A5 - Flight Part Assembly and Qualification Test Boards

A second qualification batch was assembled by ST in 2020. GR740 dice from two wafers, with Over Pad Metallisation (OPM), were used for this assembly. A total of 236 parts were submitted by ST to the external precap inspection performed on the qualification batch.

The screening of this batch, performed as defined in [AD1] for QML-V level, was successful, and the batch was accepted for qualification testing.

5.1.7 Task B1 - Qualification Testing

The following qualification tests were performed on fully screened parts as defined in [RD2]:

- QML-V Qualification Tests:
  - Group A (Electrical Tests in accordance with SCD).
    - Completed on 190 samples (only 116 required)
  - Group B (Mechanical and Environmental Tests).
    - Covered both CLGA and CCGA package solutions.
  - Group C (Life Test).
  - Group D (Package related Tests).
    - Covered both CLGA and CCGA package solutions.
  - Group E (Radiation Hardness Assurance TCI/QCI Test).
    - Total ionising dose
    - Single Event Effects
- Delta ESCC Evaluation will be performed as per ESCC 2269000:
  - Chart I(A) Group 2 – Destructive Tests:
    - Subgroup 2C – Construction Analysis (performed by ESA)
    - Subgroup 2D(iv) – Package Tests.
    - Subgroup 2E – Electrical Tests.

All qualification tests were completed successfully.

5.1.8 Task B2 - Certification and Commercialisation

Based on qualification test results, the data package for DLA was developed. Extensive internal reviews were performed within the team, leading to several iterations in correlating the data with the draft contents of the SMD. This work took considerably longer time than originally planned. Eventually, a data package including the results of the screening and qualification testing has been submitted to the DLA to obtain the QML certification for this product. ESA has also received a copy of the data package.

In parallel, commercialization activities have continued, starting prior to Task B2 with sales of prototypes and engineering models. This has been summarized in the Commercial Evaluation Report D14, developed during this task and provided to ESA.

5.1.9 Summary

The activity has been successfully completed, but the duration extended with more than 50%, from the original 27 months to the final 43 months. As can be seen in the overview and Gantt chart in section 5.1.1 above, the main part of the extension took place after the FVR and start of the qualification testing and was mainly due to the assembly of the second batch described for task A5.

5.2 Delivered outputs

The following table gives an overview of all deliverables of this activity:

Table 3 List of deliverables

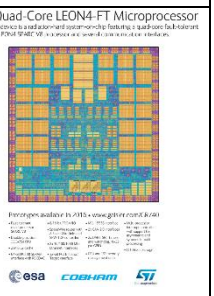
Deliverable	**Name / Title**	**Description**	**Reference**
D02	Production Test Plan	Production test plan	GR740-PTPL-0002 / issue 2.4
D03, part of	GR740 Package Design File Overview	Package design files (drawings, IBIS models etc)	GR740-PKGD-0003 / issue 1.1
D03, part of	IBIS file gr740_fm_ccga625_180612.zip, digital attachment provided with D03	Package design files (drawings, IBIS models etc)	gr740_fm_ccga625_180612.zip
D05	GR-CPCI-GR740_Board_rev1_2_20180219.zip	Validation board design files	GR-CPCI-GR740_Board / rev. 1.2
D06	Validation Plan	Validation plan	GR740-VALP-0006 / issue 2.1

Deliverable	Name / Title	Description	Reference
D07, part of	GR-CPCI-GR740 Development Board User's Manual	Validation board documents (User manual, Schematics, Floorplan, Product Sheet, for public release)	GR-CPCI-GR740-UM / version 2.3
D07, part of	GR-CPCI-GR740 Development Board quick Start Guide	Validation board documents (User manual, Schematics, Floorplan, Product Sheet, for public release)	GR-CPCI-GR740-QSG / issue 1.8
D08	Validation Report, Functional and Electrical part	Validation Report (functional / electrical part)	GR740-VALR-0009 / issue 2.3
D09	GR740 Technical Note on Benchmarking and Validation	Validation / Benchmarking Technical note (public)	GR740-VALT-0010 / issue 3.4
D10	GR740 Quad Core LEON4 SPARC V8 Processor 2020 Data Sheet and User's Manual	GR740 Data Sheet (update) (public)	GR740-UM-DS / version 2.4
D11	Screening and qualification plan for GR740 flight models	Qualification Plan	GR740-QPLN-1 / issue 2.1
D12	GR740 Radiation Report	Validation Report (radiation part)	GR740-RADR-1 / issue 1.4
D13	GR740 Radiation Summary	Radiation Summary (published on ESCIES)	GR740-RADS-1 / issue 1.3
D14	Commercial Evaluation Report	Commercial Evaluation Report	GR740-COME-0014 / issue 2.0
D15, part of	GR740 Qualification Test Report	Qualification Test Report (and logs)	GR740-TRPT-1 / issue 1.0
D15, part of	Qualification test report and logs provided directly by ST	Qualification Test Report (and logs)	Uploads provided to ESA 2021-06-09
D16, part of	GR740 PID Overview	Qualification Package	GR740-PID-1 / issue 1.0
D16, part of	Qualification Package provided directly by ST	Qualification Package	Uploads provided to ESA 2021-06-09

Deliverable	Name / Title	Description	Reference
D17	Executive Summary Report	Executive Summary (for public release)	NGMPFM-ESR-1 / issue
D18	Final Report	Final Report (for public release)	NGMPFM-FR-1 / issue 1.0
CCD	Contract Closure Summary	Contract Closure Documentation	NGMPFM-CCS-1 / issue 1.0 (to be approved with ESA)
HW1, part of	GR740 Prototypes, packaged tested and fully functional	Physical product	2x GR740-CP-CG625 (s/n 9 & 11 (D1819)
HW1, part of	GR740 Prototypes, packaged tested and fully functional	Physical product	1x GR740-CP-CG625 (s/n TBC, not yet delivered 2021-06-10)
HW2, part of	Validation Board(s), fully populated and functional	Physical product	2x GR-CPCI-GR740 (s/n 46 and 55)
HW2, part of	Validation Board(s), fully populated and functional	Physical product	1x GR-CPCI-GR740 (s/n 81)
HW3, part of	Flight Parts (3 parts for construction analysis, extended to 5 parts)	Physical product	2x GR740 in CLGA package from qualification bath #1, SN5 and 7 (D1913A)
HW3, part of	Flight Parts (3 parts for construction analysis, extended to 5 parts)	Physical product	1x GR740 in CLGA package from qualification batch #2, SN11 (D2009A)
HW3, part of	Flight Parts (3 parts for construction analysis, extended to 5 parts)	Physical product	2x GR740 in CCGA package from qualification batch SN13 & SN14 (D2009A)
HW4	Promotional Items	Physical (and digital) products, see note 1) below.	N/A
SW1, part of	Final Design Database (update from RD[14] in the SoW) with latest version of all items, enhanced with test pattern, manufacturing and test logs.	Production test logs for batch of 25 GR740-MP devices, room temperature	NGMP_cut2_GR740_MP_25spl_Ambiant.xlsx
SW1, part of	Final Design Database (update from RD[14] in the SoW) with latest version of all items, enhanced with test pattern,	Production test logs for batch of 25 GR740-MP devices, cold temperature	NGMP_cut2_GR740_MP_25spl_Cold.xlsx

Deliverable	Name / Title	Description	Reference
	manufacturing and test logs.		
SW1, part of	Final Design Database (update from RD[14] in the SoW) with latest version of all items, enhanced with test pattern, manufacturing and test logs.	Production test logs for batch of 25 GR740-MP devices, hot temperature	NGMP_cut2_GR740_MP_25spl_hot.xlsx
SW1, part of	Final Design Database (update from RD[14] in the SoW) with latest version of all items, enhanced with test pattern, manufacturing and test logs.	Test program version tracking spreadsheet delivered with batch of 25 GR740-MP devices	ST_Deliveries_tracking_for_NGMP_cut2_25GR740_MP.xlsx
SW2	Validation Database (update)	Data package with logs and outputs from the software validation tests and benchmarks, re-run on flight silicon.	VALDB-190319.tar.gz

1) Related to HW4, posters were provided for the previous Phase 2 contract. Due to e.g. restrictions in physical meetings the last 15 months, there have been no updates of these kind of posters. Promotional items or activities are instead provided in digital format, such as regular updates on https://www.gaisler.com/index.php/products/components/gr740, notifications on https://twitter.com/cobhamgaisler/status/1199730464874995712?lang=en, and presentations at conferences, see an overview in deliverable D18.



5.3 External presentations

There have been several different external presentations related to GR740 qualification held during the activity:

- DASIA 2016, GR740: Rad-Hard Qua-Core LEON4FT System-on-chip
- SEE-MAPLD 2016, Radiation testing of the GR740 Rad-Hard Quad-Core LEON4FT
- SpW Conference 2016, GR740 SpaceWire router validation methodology and results
- RADECS 2019, Single Event Effect Characterization of the GR740 Rad-Hard Quad-Core LEON4FT System-on-Chip
- GR740 User Day 2019, GR740 development status
- ESCCON 2021, GR740 CLGA CCGA qualification results

6 ACHIEVED RESULTS

6.1 Developed product

The finally developed product is illustrated in the figure below. The variant illustrated is a flight equivalent part (MSEV) manufactured prior to available QML certificate. This part has been screened in accordance with the QML-V flow and the whole batch has completed successfully all the relevant QML-V qualification tests.

Figure 5 *GR740 physical component*

There will be four flight variants available, covered by the same SMD number, the only difference being the package type (CLGA and CCGA) and the quality level QML-Q / QML-V. See table below.

Table 4 Flight variants

Product	Part no.	Processor core	Package	Temp. range	Qualification status
GR740-MSQ-LG625 GR740-MSV-LG625	GR740 SMD: 5962-21204	Quad-Core LEON4FT	625-Pin Ceramic **Land** Grid Array	-40°C / +125°C (junction)	QML-Q/V qualification tests completed in 2020 QML-Q/V approval expected in Q2 2021
GR740-MSQ-CG625 GR740-MSV-CG625	GR740 SMD: 5962-21204	Quad-Core LEON4FT	625-Pin Ceramic **Column** Grid Array	-40°C / +125°C (junction)	QML-Q/V qualification tests completed in 2020 QML-Q/V approval expected in Q2 2021

The main common performance for all flight variants is summarized below.

Table 5 Flight variant performance

Product	Clock freq. (MHz)	Perf. (DMIPS)	TID krad (Si)	SEL LET (MeV-cm^2/mg)	Power cons.
GR740-MSQ-LG625 GR740-MSV-LG625 GR740-MSQ-LG625 GR740-MSV-LG625	250	>1700 [1)]	300	> 125	< 2W at 40 °C [1)]

Notes:

1) For more information, see https://www.gaisler.com/doc/gr740/GR740-VALT-0010.pdf

In addition, there are a number of engineering models and other prototypes available. They are listed in the table below, also including the flight models. Apart from package type, the manufacturing flow and temperature range may differ compared to the flight models.

Table 6 Product variant including prototypes

Product	**Description**
GR740-CP-LG625	Engineering model (prototype)
GR740-CP-CG625	Engineering model (prototype)
GR740-MP-LG625	Electrical Qualification Model
GR740-MP-CG625	Electrical Qualification Model
GR740-MSEQ-LG625	Flight Model, Equivalent to QML-Q
GR740-MSEQ-CG625	Flight Model, Equivalent to QML-Q
GR740-MSEV-LG625	Flight Model, Equivalent to QML-V
GR740-MSEV-CG625	Flight Model, Equivalent to QML-V
GR740-MSQ-LG625	Flight Model, QML-Q
GR740-MSQ-CG625	Flight Model, QML-Q
GR740-MSV-LG625	Flight Model, QML-V
GR740-MSV-CG625	Flight Model, QML-V
GR740-DC-LG625	Daisy-chain. Representative of GR740-YY/CP/MP/MSEQ/MSEV/MSQ/MSV-LG625
GR740-DC-CG625	Daisy-chain. Representative of GR740-YY/CP/MP/MSEQ/MSEV/MSQ/MSV-CG625
GR740-DD-LG625	Dummy package (not electrically functioning) without columns.
GR740-DD-CG625	Dummy package (not electrically functioning) with columns.

Table 7 Ordering legend

Designator	**Option**	**Description**
Product	GR740	Quad-Core LEON4FT System-on-Chip
Temperature range and screening flow	CP	Prototypes, tested at room temperature
	MP	Electrical Qualification Model, tested at cold, room, hot
	MSEQ	Flight model, Equivalent to QML-Q
	MSEV	Flight model, Equivalent to QML-V
	MSQ	Flight model, QML-Q
	MSV	Flight model, QML-V
Package type	CG	Ceramic Column Grid Array (CCGA). Delivered with IBM type (Sn/Pb 10/90) columns.
	LG	Ceramic Land Grid Array (LGA)
Number of pins	625	Number of pins

6.2 Test and Performance summary

The major work of establishing performance figures was performed prior to the Phase 3 activity. Some updates have been provided and the figures are included in https://www.gaisler.com/doc/gr740/GR740-VALT-0010.pdf (2021-06-10). The performance figures are grouped in areas of:

- Single-core performance
- Multi-core performance
- Impact of bus interference between processors
- I/O performance and, in particular, SpaceWire RMAP performance.

6.3 Power consumption

Several power measurements have been carried out with the processor on the default configuration (processor at 250 MHz and memory at 100 MHz) and running at 50 MHz. The measurements are taken reading the available power measurement circuits on the board (via I2C) at room temperature. The results are also provided in https://www.gaisler.com/doc/gr740/GR740-VALT-0010.pdf (2021-06-10), from which the table below is extracted, applicable for the average power consumption for core, LVDS and I/O power for GR740 die revision 1.

Table 8 Power consumption

Scenario	Description	Core Power (mW)	LVDS Power (mW)	I/O Power (mW)
9	CPU2000 (single core/LVDS on) @250 MHz	605.09	440.58	185.29
10	CPU2000 (all cores/LVDS on) @250 MHz	1,189.72	439.23	285.82

6.4 Radiation Tolerance

The Total Ionizing Dose (TID) radiation verification tests of GR740 device to the targeted dose of 300 krad(Si) have been completed successfully. Both normal and cold spare operation modes of the GR740 have been verified in the TID testing. Data collected at library level by ST demonstrated that biased conditions were worst case with respect to unbiased conditions during TID testing.

The Single Event Latch-up (SEL) testing of the GR740 device has confirmed the SEL immunity of the device up to an LET of 125 MeV.cm²/mg (tested with elevated temperature - > 85 ºC - and maximum supply voltages).

The GR740 device has also been tested for Single event effects (SEE) in both static and dynamic modes. In dynamic mode, the tests consisted of several application level tests, ranging from memory tests to a multicore test.

The low functional error rate recorded in the application-level tests under irradiation demonstrates that although an extensive amount of SEUs in the internal memory cells of the GR740 have been recorded, all events were successfully mitigated and corrected. There is no evidence of error build-up in the GR740.

The information above and additional details are also available in https://gaisler.com/doc/gr740/GR740-RADS-1-1-3_GR740_Radiation_Summary.pdf (2021-06-10).

6.5 Production line

In addition to the product itself, a serial-production line has been established and validated. The main manufacturing activities are performed at STMicroelectronics in France, using the facilities in Crolles, Rennes and Grenoble.

For variants equipped with columns, column attachment is performed at Micross Crewe UK.

6.6 Problems experienced

6.6.1 Package development

It was identified already prior to Phase 3, that flip-chip technology would not be available for this project. A new package had to be developed based on a substrate, double pad-rings, and relatively long and crossing bond-wires.

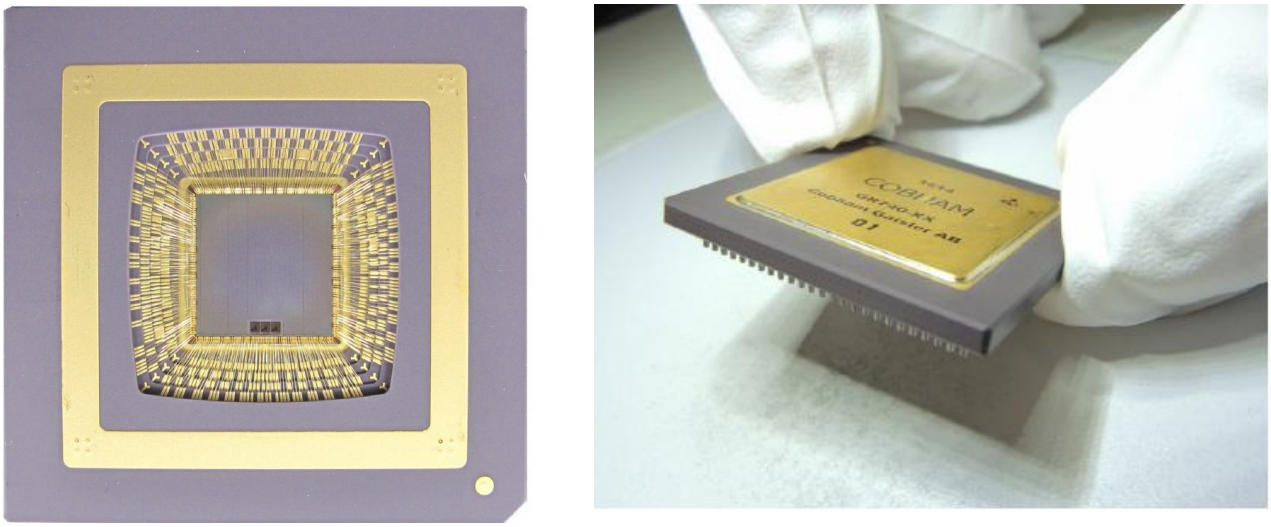


Figure 6 *Illustration of bond-wires*

This led to development of functional prototypes and, in the end, additional design improvements for the final product. Package validation included:

- Vibration, TM 2007 Condition A
- Mechanical Shocks, TM 2002 Condition B
- Constant acceleration, TM 2001 Condition D
- PIND test, TM 2020 Condition A.
- Electrical test & X-ray before and after each test.

6.6.2 Over Pad metallization

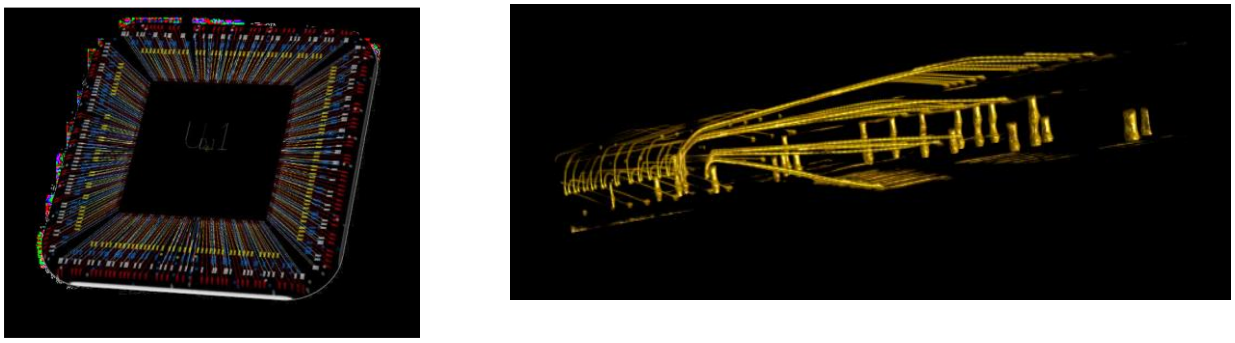
Al wedge bonding was not possible for the C65SPACE library due to pad size compatibility and the complexity of the GR740. Au wire had to be used instead. Because of the Al pad – Au wire metal interface, an OPM layer was implemented.

This required wire bonding validation to be performed after die aging on corner case (500h 150C / 500h 85C/85%RH) with metallization integrity check after aging, followed by constructional analysis.

6.6.3 Wire bonding

Apart from the new package design, the wire bonding itself introduced some challenges.

The C65SPACE library imposed the use of Au ball bonding. At the same time, device complexity imposed the use of thin bond wires, 20µm in diameter. To achieve this, 4 decks were necessary to accommodate all bond wires.



X-ray based 3D reconstruction of the GR740 bonds
Images courtesy of ST Microelectronics

Figure 7 *GR740 Wire-bonding*

6.6.4 Selection of column type for CCGA package

The GR740 package is compatible with various column types:

- Sn/Pb IBM type (Micross Crewe UK)
- Sn/Pb copper wrapped (e.g. Serma, SixSigma)

The QML qualification has been run with Micross IBM type columns, supported by Micross Crewe UK, currently QML-Q/V/Y certified by the DLA. Several of the column related tests were performed by Micross, such as solderability test.

As part of these activities, a board level reliability (BLR) study of the IBM columns was completed by ST & Micross. The report delivered substantiated the Micross column attach process as being consistent and repeatable. Placement accuracy and process controls were measurable and within specifications. The BLR followed the requirements of ECSS-Q-ST-70-38C-Rev.1-corrigendum 1 (2018), which included vibrations, mechanical shock and thermal cycling. As expected, the first failure manifested in the corner columns through the column itself. The results were found to be compliant with the ECSS standard and therefore fit for purpose.

A lesson learnt from this activity is that the corner columns are the most sensitive to degradation due

to mechanical and thermal stress. In the GR740, all corner columns are ground pins. Because of the multiple ground pins available on the device, the loss of all 4 corner columns will have no impact on the functioning of the device. This approach must be repeated in future CCGA developments.

6.7 Known anomalies

Except for the errata described in section 43 of the GR740 Data Sheet and User's Manual, https://www.gaisler.com/doc/gr740/GR740-UM-DS-2-4.pdf (2021-06-10), there are as of today no confirmed known anomalies of the product.

7 LESSONS LEARNED

There are a few areas of lessons to be learned, several of them not unique to this activity:

- In every development obtaining requirements and feedback from users is difficult but very valuable.
- It is important to release prototypes early for:
  - Functional validation
  - Radiation characterisation
  - Allow customers to test and design-in the device.
- Hardware/Software Co-engineering is critical to make sound design decisions. The GR740 has benefited from backward compatibility with earlier generation LEONs and a large software ecosystem for development available at an early stage.

The duration of the activity was extended with approximately 16 months compared to the initial schedule, 43 months instead of 27. The reasons for this and related lessons learned are several, such as:

- Initially in a project with a complex product, it is difficult to imagine all potential technical challenges that may appear, requiring loops in the project cycle. More frequent and comprehensive project risk analyses would not have resolved all delays, but possibly shortened some if potential mitigating actions had been defined in advance.
- Multiple levels of suppliers generate additional challenges. Control of suppliers' resources and priority handling, and vice versa the suppliers' awareness of overall project goals, is reduced for every level. Improved multi-level transparency may reduce such effects.

8 FURTHER EVOLUTIONS

8.1 GR740 PBGA

The GR740 design will be reused for the GR740-PBGA. It uses the same die, but the GR740-PBGA device is the plastic version of the radiation-hard quad-core fault-tolerant LEON4 SPARC V8

processor targeting space constellations.

Figure 8 *GR740 PBGA*

The GR740-PBGA has the same functionality, fault-tolerance and radiation-hardness as the GR740 system-on-chip device. The GR740-PBGA has a Plastic Ball Grid Array (PBGA) with 625 balls, being footprint compatible the GR740 Ceramic Column Grid Array (CCGA), featuring the same pinout and 1mm pitch.

The GR740-PBGA is made available in two quality and temperature ranges:

- GR740-CP-PBGA625 - prototype quality, commercial temperature range
- GR740-AS-PBGA625 - flight quality (ESCC-Q-60-13C class 2), automotive temperature range -40C to +105C

Prototypes are currently undergoing internal evaluation and are planned to be available for sale and delivery in Q2 2021. Flight parts are planned to be available for sale and delivery in Q4 2021.

8.2 GR765

A new contract has been signed to develop the GR765, with the main objectives of developing a radiation-hard multi-core processor based on the LEON5 architecture as the natural evolution from GR740, and to surpass main competitors in computing performance and functionality.

Figure 9 GR765

The first development phase of the GR765 is funded through Element 2: Make of ESA's General Support Technology Programme (GSTP), and co-funded by CAES and the Swedish National Space Agency (SNSA). Element 2 sponsors the design, development and demonstration of activities based on industry proposals. In doing so, GSTP encourages more ideas and partnerships, ultimately leading to the most innovative technologies for the European space industry.

The GR765 Microprocessor builds on the success of the GR740 quad-core LEON4FT Microprocessor and contains eight LEON5FT processor cores, which is the latest and most powerful LEON processor so far. Its architectural improvements and octa-core implementation will provide a four-time increase in computational performance when run at the same frequency as previous generation microprocessors. Work is ongoing to improve the maximum operating frequency, further enhancing the performance. With these significant improvements, new, more advanced and data-demanding computations will be possible for payload and platform applications. The first development phase of GR765 Microprocessor will result in engineering samples expected in 2022, with flight production in 2024.

9 CONCLUSION

The GR740 microprocessor has been developed within ESA's NGMP (Next Generation Micro Processor) initiative in TRP, GSTP and EOP programmes, accompanied also by several activities to consolidate the SW ecosystem.

The Phase 3 contract dedicated to the production of GR740 Flight Models has now been completed. Screening / qualification tests per MIL-PRF-38535L / MIL-STD-883K and delta-evaluation per ESCC-2269000 have been passed successfully.

QML-V & QML-Q equivalent flight parts can now be ordered, and first users have already designed GR740 into their equipment.

QML-V and QML-Q qualified parts will be offered once the certification is granted by the DLA.