COBHAM

Executive Summary

Next Generation Microprocessor (NGMP) Engineering Models
Product code: GR740

Report

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Contract 2000113922/15/NL/LF
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1 INTRODUCTION

1.1 Scope of the Document

This document establishes the executive summary report for the NGMP engineering models (product code GR740) activity initiated by the European Space Agency under ESTEC contract 2000113922/15/NL/LF.

Cobham Gaisler has together with ST Microelectronics manufactured and validated a quad-processor LEON4FT system-on-a-chip device on ST Microelectronics' European Space DSM technology platform C65SPACE. The NGMP, which has been commercialised under product name GR740, provides a significant performance improvement over earlier generations of European space microprocessors and the development is a significant advance in space processor architecture where the NGMP project has been a key driver toward multicore architectures within the European space industry.

1.2 Reference Documents

The following documents are referred as they contain relevant information:

[RD1] “18533/04/NL/JD, COO3: Development of LEON3-FT-MP (GINA)”, http://microelectronics.esa.int/finalreport/SummaryReport-18533-COO3-2006-05-15.pdf

[RD2] “18533/04/NL/JD, COO4: Maintenance and Support of LEON2FT, namely during AT697F development”, http://microelectronics.esa.int/finalreport/SummaryReport-18533-COO4-2007-04-11.pdf

[RD3] “The ESA Next Generation Microprocessor (NGMP)”, ESA Microelectronics section, http://microelectronics.esa.int/ngmp/

[RD4] “GR-CPCI-GR740 Quad-Core LEON4FT Development Board”, Cobham Gaisler, http://www.gaisler.com/gr-cpci-gr740

2 ACRONYMS

AHB	Advanced High-performance Bus, part of AMBA 2.0 Specification
AMBA	Advanced Microcontroller Bus Architecture, bus architecture widely used for on-chip buses in SoC designs.
APB	Advanced Peripheral Bus, part of AMBA 2.0 Specification
ASIC	Application Specific Integrated Circuit
ASMP	Asymmetric Multi-Processing (in the context of this document: each of the CPU cores runs its own OS)
BCH	Bose-Hocquenghem-Chaudhuri, class of error-correcting codes
BIST	Built In Self Test
BSP	Board Support Package
CG	Cobham Gaisler
CPU	Central Processing Unit
DCL	Debug Communication Link
DDR	Double Data Rate
DMA	Direct Memory Access
DSM	Deep-Sub-Micron ASIC technology
DSU	Debug Support Unit
EDAC	Error Detection And Correction
EDCL	Ethernet Debug Communication Link
FIFO	First-In-First-Out, refers to buffer type
FLOPS	Floating Point Operations Per Second
FPU	Floating Point Unit
Gb	Gigabit, 10^9 bits
GB	Gigabyte, 10^9 bytes
Gib	Gibibit, gigabinary bit, 2^{30} bits
GiB	Gibibyte, gigabinary byte, 2^{30} bytes, unit defined in IEEE 1541-2002
GRLIB	Aeroflex Gaisler's IP core Library
HSSL	High-Speed Serial Link
HDL	Hardware Description Language
I/O	Input/Output
IP	Intellectual Property
IPR	Intellectual Property Rights
ISR	Interrupt Service Routine
ITT	Invitation To Tender
JTAG	Joint Test Action Group (developer of IEEE Standard 1149.1-1990)
kB	Kilobyte, 10^3 bytes
KiB	Kibibyte, 2^{10} bytes, unit defined in IEEE 1541-2002
LRU	Least-Recently-Used
MAC	Media Access Controller, when referring to, for instance, an Ethernet MAC

Mb, Mbit	Megabit, 10^6 bits
MB	Megabyte, 10^6 bytes
MiB	Mebibyte, 2^{20} bytes, unit defined in IEEE 1541-2002
MILS	Multiple Independent Levels of Security
MIPS	Million of Instructions Per Second
NGMP	Next Generation Microprocessor
OS	Operating System
PCI	Peripheral Component Interconnect
PED	Pender Electronic Design
PLL	Phase Locked Loop
PROM	Programmable Read-Only Memory
RAM	Random Access Memory
RMAP	Remote Memory Access Protocol
RS232	Recommended Standard 232, standard for serial data signals
RTL	Register Transfer Level
SDRAM	Synchronous Dynamic Random Access Memory
SEE	Single Event Effects
SEL/SEU/SET	Single Event Latchup/Upset/Transient
SMP	Symmetric Multi-Processing
SPARC	Scalable Processor ARChitecture
SOC, SoC	System-On-a-Chip
TMR	Triple Modular Redundancy
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol

3 BACKGROUND

During the past years Cobham Gaisler (previously Aeroflex Gaisler and Gaisler Research) has been one of the main actors in the development of the latest generation of the SPARC architecture-based ESA microprocessor family that is called LEON and in particular the fault-tolerant version for space use.

The pre-development of the NGMP, a quad-core SPARC processor has been performed in 2005/2006 by Cobham Gaisler (then Gaisler Research) under ESA contract 18533/04/NL/JD, COO3 under the code name GINA (Giga Instruction/s New Architecture) [RD1]. The architecture was prototyped on FPGA board, but it became clear that such a design requires an ASIC technology < 100 nm. Due to the non-availability of a suitable space ASIC technology, further development was then suspended for about two years. After the start of a TRP activity to develop a 65 nm space ASIC technology with ST Microelectronics in January 2008, the Architectural Design, RTL coding, Simulations, FPGA prototyping of the NGMP was undertaken under under ESTEC contract 22279/09/NL/JK. Kick-off was in June 2009, and the PDR milestone was achieved in December 2010. Since the access to the ST design kit was blocked, the NGMP development was put on hold again for three years. In the meantime, functional prototypes of the NGMP were developed in 45 nm structured ASIC technology under ESA contract 18533/04/NL/JD, COO3 under the code name NGFP [RD2]. Boards with these chips became commercially available during Q2/2013 allowing user prototyping and the development of the necessary software environment. A design kit for ST 65 nm was finally provided in Q2/2014, and the contract was resumed and extended with a CCN to perform detailed design and layout work up to the level of tape-out (start of manufacturing).

Manufacturing, functional validation, electrical validation and radiation validation has then been undertaken under the current ESA contract 2000113922/15/NL/LF. The current contract has taken the device from tape-out through testing, packaging, development kit design, functional validation and finally radiation validation. Qualification is not covered by the existing contract and is remaining work for the final third phase of the NGMP hardware development activities. In parallel, the NGMP hardware development has been complemented by several activities to validate and benchmark the FPGA and functional prototypes and to provide a suitable SW framework for this multi-core processor, e.g. SMP operating systems and a Hypervisor to handle TSP.

4 OVERVIEW OF THE ACTIVITY

The overall objectives of the NGMP series of activities planned by ESA are to define, develop, manufacture, validate and qualify flight parts of the NGMP within a time frame of 5 years. The NGMP shall, as far as possible, be compatible to main stream multi-core processors, allowing an efficient use/re-use of existing software development tools as compilers, multi-core debuggers and Operating Systems with limited modifications.

The main goal of the present activity was to manufacture, test and validate the device on the European space DSM technology.

The following companies were involved in the development:

- Cobham Gaisler – Cobham Gaisler (Sweden) was the prime contractor and supplied test patterns, specified the validation board and performed functional and radiation validation.
- ST Microelectronics – The ASIC library design support and ASIC backend work has been performed by ST Microelectronics (France, United Kingdom)
  - The business unit handling the space market have headquarters in France and production tests were also performed in France.
  - The backend team involved in this development are located in the United Kingdom. The backend team has supported the project past manufacturing.
- Pender Electronic Design handled detailed design and manufacturing of development boards for the device.
- e2v – e2v in France performed the package design and performed assembly for the first set of prototypes. e2v then stated their unwillingness to continue to support wire-bonded devices and assembly was instead moved to ST.

5 WORK PERFORMED AND MAIN RESULTS

The GR740 design that was taken through back-end design during ESA contract 22279/09/NL/JK has been manufactured, packaged and validated. Figure 1 below shows a block diagram of the system-on-a-chip architecture that was implemented.

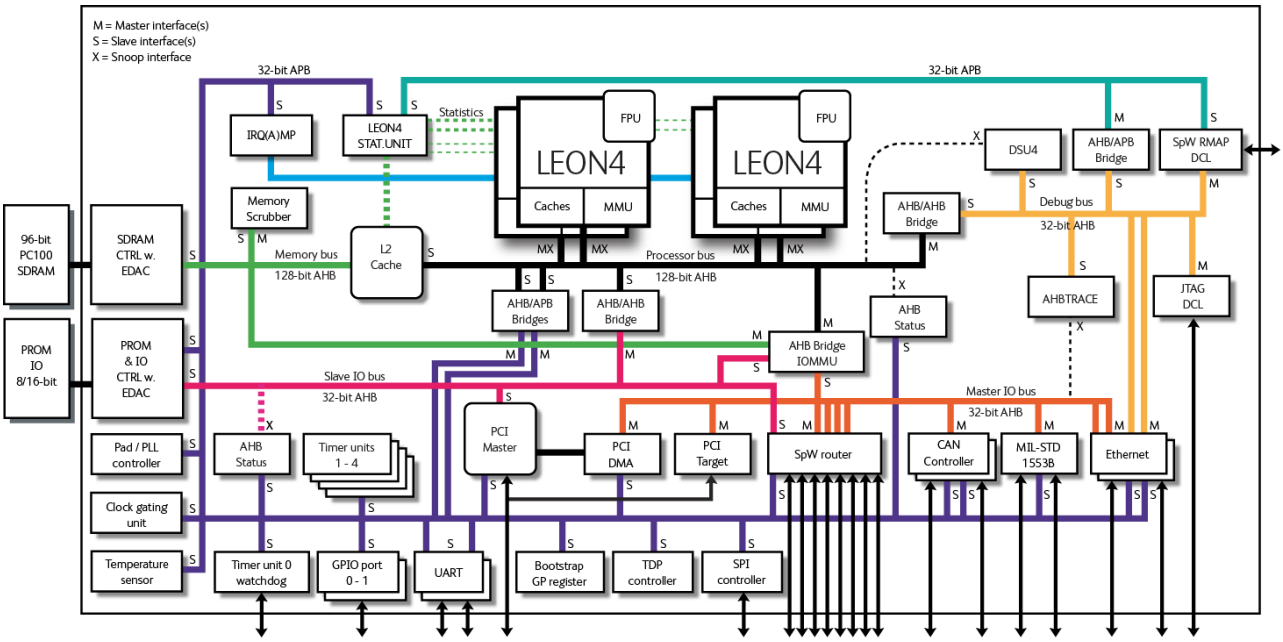

Figure 1. GR740 architecture block diagram

The resulting layout of the silicon device is shown in figure 2. After manufacturing the silicon was tested at ST's facilities in Grenoble and assembly (packaging) was performed at e2v. The first set of devices was delivered to Cobham Gaisler in Sweden in December 2015. In parallel with the production test and assembly activities, a development board was manufactured (see figure 3) and development board bring-up activities and the functional validation effort began in January 2016.

The functional validation effort was a success with device performances exceeding expectations in terms of operating frequency. The worst-case operating frequency for the device from static timing analysis was 250 MHz. Benchmarks and boot of the Linux operating system was possible to perform with the device running at over 400 MHz operating frequency. This correlates well with ATPG test patterns passing at 380 MHz over the full temperature range.

During the functional validation effort, errata were discovered both for the GR740 device and for the development board. All errata found during the functional validation effort was possible to

address using development board changes or minor changes to software initialization routines, except for a nonfunctional on-chip temperature sensor that will require changes to the package or silicon. However, as described below, errata with SEU protection have been discovered during radiation testing, these are not affecting the device without radiation.

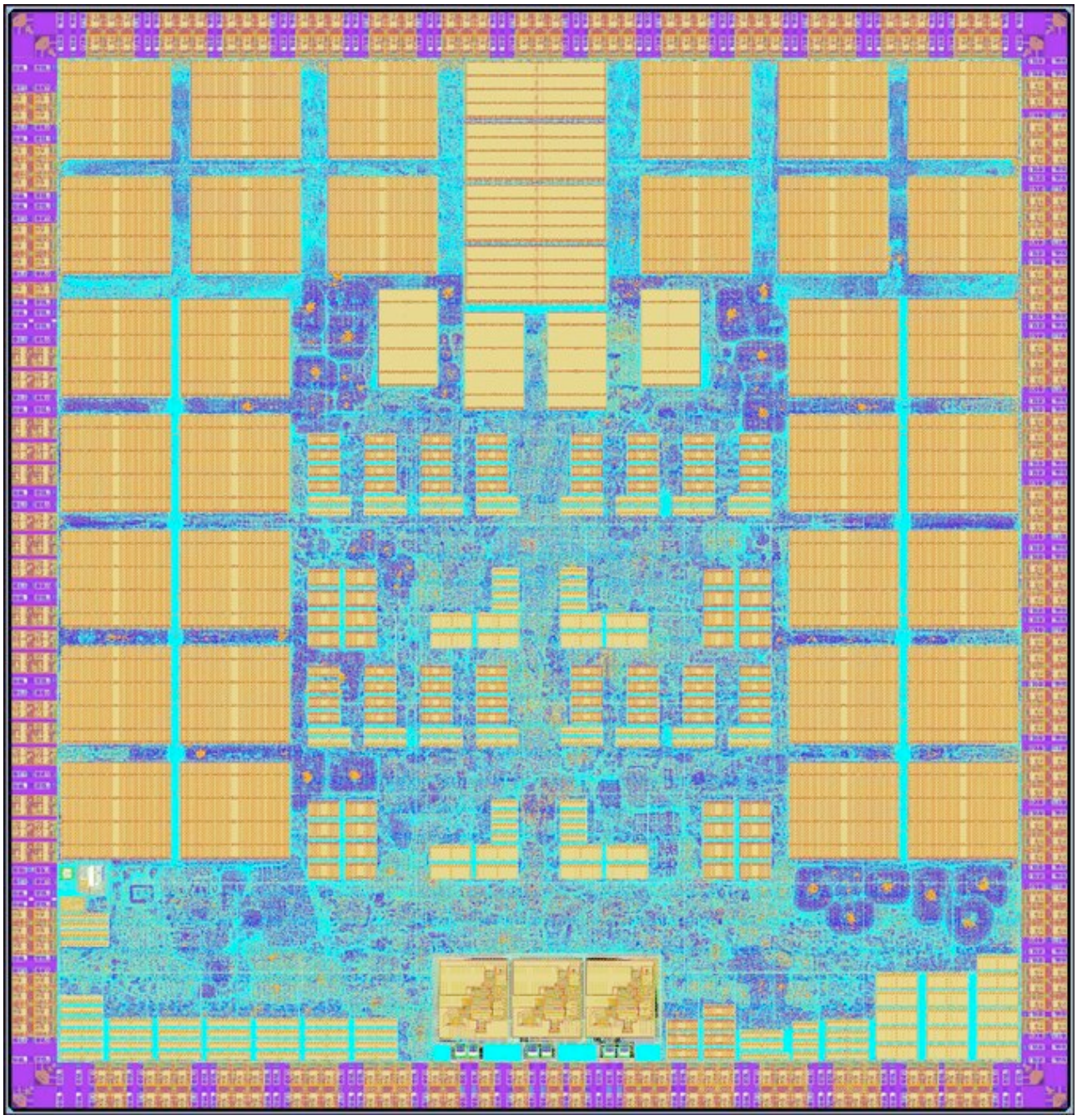

Figure 2. GR740 layout

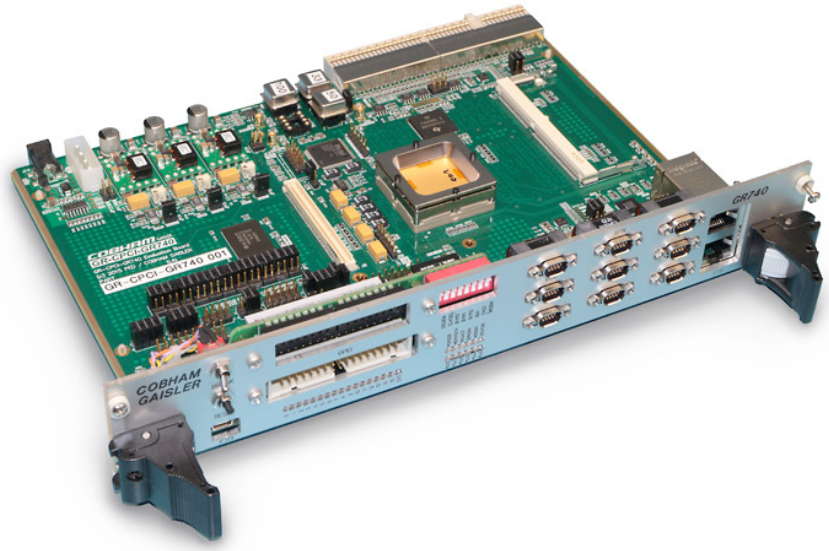

Figure 3. GR-CPCI-GR740 development board

A revision was made to the development board and boards populated with devices have been provided to end users since the first quarter of 2016. End users both in Europe and the USA have also procured devices to build their own board based on the GR740 device.

Several benchmark suites have been run on the processor:

- Each processor provides 459 Dhrystone MIPS (or DMIPS) per core, which gives 1.84 DMIPS/MHz.
- Each processor provides 200.6 Whetstone MIPS (or MWIPS), which gives 0.8 MWIP/MHz.
- The Linpack benchmark reports 22.7 MFLOPS
- The EEMBC CoreMark 1.0 reports 511.7 CoreMarks.
- The EEMBC Autobench 1.1 reports 111.97 AutoMarks
- The EEMBC FPMark 1.3 reports 189.18 FPMarks
- The EEMBC CoreMark-Pro 1.1 reports 73.48 CoreMarks

The final part of the contract was to perform radiation validation of the device. The planning included sessions with SEE testing using heavy-ions and protons as well as total dose testing. As part of the preparations for radiation tests the existing SEU32 test software that has been used for

radiation validation of previous LEON devices (such as AT697 from Atmel, UT699 from Aeroflex Colorado Springs and GR712RC from Cobham Gaisler) was extended to cover new features in the GR740 device. This included adding support for Ethernet controller tests, SpaceWire router tests and multiprocessor tests.

The first radiation test session was performed at RADEF in Finland and the outcome was unexpected. Following analysis of the data from the first session a bug was found in the Level-2 cache. The presence of a bug in the L2 cache EDAC delayed progress in the activity since the software had been developed with the assumption that all radiation mitigation measures would be successful. The Level-2 cache issues was isolated through code inspection and error injection runs at Cobham Gaisler. The source of the problem was that the Level-2 cache was updated late in the project (as part of the phase 2 contract) with functionality to allow hit under miss processing. At the time it was identified that the updates were of high risk, in particular for the fault-tolerance functionality that protects the internal SRAMs in the Level-2 cache. Additional verification effort was put on the Level-2 cache to address this. However, analysis after the bug was found showed that two independent verification engineers has selected to test upsets in the Level-2 cache tag RAMs by only injecting error in the TAG checksums. The erratum manifests when a correctable error occurs in the data value the cache tag. In this case, the L2 cache detects the correctable error but during correction the Level-2 cache will regenerate the checksum but reuse the corrupted data value.

A software workaround has been developed and tested for this Level-2 cache issue and subsequent radiation tests were run with the Level-2 cache disabled. Further radiation testing and error injection tests also revealed problems with LEON4FT branch prediction in connection with parity errors in the Level-1 instruction cache. Also these issues were introduced as late additions before tape-out. In this case with branch prediction, the risk associated with the late changes was also identified and the malfunctions that can be triggered in a radiation environment can be disabled by configuration registers in the processor.

The final heavy-ion tests sessions indicated that with the Level-2 cache disabled and software workarounds for LEON4FT branch prediction there were no more functional issues with fault-tolerance in the design and that the design will meet the radiation hardness requirements given in the activity’s statement of work.

At the time of writing, all errata deemed appropriate to correct for flight models has metal mask changes identified. The corresponding mask changes have also been verified using FPGA validation. Additional analysis of the last radiation test results will continue after the contract closure in collaboration with ST Microelectronics and may affect the fixes implemented for phase 3 flight models.

6 DELIVERABLES

The deliverables in the list below have been produced within this contract. Deliverables marked in bold are or will be made available for public dissemination.

- D01: GR740-PLOT-0001: Layout plot (electronic and 3 printed copies)
- D02: GR740-PTPL-0002: Production Test Plan
- D03: GR740-PKGD-0003: Package Design Files
- D04: GR740-BSPEC-0004: Validation Board Specification
- D05: GR740-VALB-0005: Validation Board Design Files
- D06: GR740-VALP-0006: Validation Plan
- D07: GR740-VBDB-0007: Validation Board documents (**User manual**, schematics, floorplan, **product webpage**)
- D08: GR740-VALR-0009: Validation Report (functional / electrical part)
- **D09: GR740-VALT-0010: Validation / Benchmarking Technical Note**
- **D10 / D11: GR740-UM-DS: Updated GR740 Data Sheet**
- D12: GR740-RADR-0012: Validation Report (Radiation part)
- D14: GR740-COME-0014: Commercial Evaluation Report
- D15: GR740-EXEC-0015: Executive summary (this document)
- **D16: GR740-FRPT-0016: Final Report**
- HW1 GR740 prototypes, packaged tested and fully functional (10 pieces)
- HW2 Validation board(s), fully populated and functional (3 pieces)
- SW1 Final design database
- SW2 Validation database

The following document has been postponed until phase 3: GR740-RADS-0013: Radiation Summary (public and submitted o ESCIES).

7 CONCLUSION

The main outcome of this activity is an extensively validated quad-core LEON4 microprocessor device implemented in ST C65SPACE technology.

The implementation and availability of the NGMP design has pushed the European space industry into considering more complex multi-core systems and this has resulted in additional research activities at both ESA and CNES. Progress for the NGMP development is reported at the ESA NGMP website [RD3]. The validation board product page on Cobham Gaisler's website is available at [RD4].

The NGMP is commercialized under the product name GR740. Final flight models are expected to require a device revision to correct correctable error handling in the Level-2 cache tag RAM.