ABSTRACT AND EXECUTIVE SUMMARY

NEXT GENERATION MICROPROCESSOR (PRODUCT CODE: GR740)

CONTRACT: 22279/09/NL/JK

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1 INTRODUCTION

1.1 Scope of the Document

This document constitutes the Abstract and Executive Summary Report for the Next Generation Microprocessor (NGMP) development.

The NGMP has been defined and implemented as part of an activity initiated by the European Space Agency under ESTEC contract 22279/09/NL/JK.

The work has been performed by Aeroflex Gaisler AB, Göteborg, Sweden.

1.2 Reference Documents

[RD1] “18533/04/NL/JD, COO3: Development of LEON3-FT-MP (GINA)”, http://microelectronics.esa.int/finalreport/SummaryReport-18533-COO3-2006-05-15.pdf

[RD2] “18533/04/NL/JD, COO4: Maintenance and Support of LEON2FT, namely during AT697F development”, http://microelectronics.esa.int/finalreport/SummaryReport-18533-COO4-2007-04-11.pdf

[RD3] “The ESA Next Generation Microprocessor (NGMP)”, ESA Microelectronics section, http://microelectronics.esa.int/ngmp/

[RD4] “GR-CPCI-LEON4-N2X, Quad-Core LEON4 Next Generation Microprocessor Evaluation Board”, Aeroflex Gaisler, http://www.gaisler.com/gr-cpci-leon4-n2x

1.3 Acronyms

AMP	Asymmetric Multi-Processing
ASIC	Application Specific Integrated Circuit
CCN	Contract Change Notification
COO	Call-Off-Order
DDR	Double Data Rate
DSM	Deep-Sub-Micron ASIC technology
DSU	Debug Support Unit
EDAC	Error Detection And Correction
FIFO	First-In-First-Out, refers to buffer type
GINA	Giga Instruction New Architecture
HSSL	High-Speed Serial Link
I/O	Input/Output
IP	Intellectual Property
MAC	Media Access Controller, when referring to, for instance, an Ethernet MAC
Mb, Mbit	Megabit, 10^6 bits
MB	Megabyte, 10^6 bytes
MiB	Mebibyte, 2^{20} bytes, unit defined in IEEE 1541-2002
MIPS	Million of Instructions Per Second
NGMP	Next Generation MicroProcessor
OS	Operating System
PCI	Peripheral Component Interconnect
RAM	Random Access Memory
SDRAM	Synchronous Dynamic Random Access Memory
SMP	Symmetric Multi-Processing
SPARC	Scalable Processor ARChitecture
SOC, SoC	System-On-a-Chip
TSP	Time and Space Partitioning
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

2 ABSTRACT

Under ESTEC contract 22279/09/NL/JK Cobham Gaisler has specified, designed, verified and validated a quad-processor LEON4FT system-on-a-chip design. The design is ready for manufacturing on ST Microelectronics' European Space DSM technology platform C65SPACE. The development effort has also resulted in all major software products from Cobham Gaisler to now support the new architecture. The NGMP, which will be commercialized under the product name GR740, provides a significant performance improvement over earlier generations of European space microprocessors and the development is a significant advance in space processor architecture where the NGMP project has been a key driver for the adoption and acceptance of multicore architectures within the European space industry.

3 BACKGROUND

During the past years Cobham Gaisler (previously Aeroflex Gaisler and Gaisler Research) has been one of the main actors in the development of the latest generation of the SPARC architecture-based ESA microprocessor family that is called LEON and in particular the fault-tolerant version for space use.

The pre-development of the NGMP, a quad-core SPARC processor has been performed in 2005/2006 by Cobham Gaisler (then Gaisler Research) under ESA contract 18533/04/NL/JD, COO3 under the code name GINA (Giga Instruction/s New Architecture) [RD1]. The architecture was prototyped on FPGA board, but it became clear that such a design requires an ASIC technology < 100 nm. Due to the non-availability of a suitable space ASIC technology, further development was then suspended for about two years. After the start of a TRP activity to develop a 65 nm space ASIC technology with ST Microelectronics in January 2008, the Architectural Design, RTL coding, Simulations, FPGA prototyping of the NGMP was undertaken under under the current ESTEC contract 22279/09/NL/JK.

Kick-off was in June 2009, and the PDR milestone was achieved in December 2010. Since the access to the ST design kit was blocked, the NGMP development has been on hold again for three years. In the meantime, functional prototypes of the NGMP have been developed in 45 nm structured ASIC technology under ESA contract 18533/04/NL/JD, COO3 under the code name NGFP [RD2]. Boards with these chips are commercially available since Q2/2013 to allow user prototyping and the development of the necessary software environment. A design kit for ST 65 nm was finally provided in Q2/2014, and the contract was resumed and extended with a CCN2 to perform detailed design and layout work up to the level of tape-out (start of manufacturing); manufacturing itself and any further steps (packaging, testing, validation, qualification) however are not covered. In parallel, the NGMP hardware development has been complemented by several activities to validate and benchmark the FPGA and functional prototypes and to provide a suitable SW framework for this multi-core processor, e.g. SMP operating systems and a Hypervisor to handle TSP.

4 OVERVIEW OF THE ACTIVITY

The overall objectives of the NGMP series of activities planned by ESA are to define, develop, manufacture, validate and qualify flight parts of the NGMP within a time frame of 5 years. The NGMP shall, as far as possible, be compatible to main stream multi-core processors, allowing an efficient use/re-use of existing software development tools as compilers, multi-core debuggers and Operating Systems with limited modifications.

The main goal of the present activity was to define, develop and verify the ASIC design of the NGMP until pre-layout level targeting the European space DSM technology, including validation in an FPGA platform. An appropriate SW environment for the NGMP shall be specified and partly implemented. The NGMP layout, manufacturing and prototype testing, as well as further development of the SW environment was expected to be performed in separate ESA contracts.

The final tasks of the current activity could not be completed on time due to unavailability of design kits for the European space DSM technology. The activity was put on hold and then resumed in Q2/2014 when an agreement was reached between Cobham Gaisler, ESA and ST Microelectronics. A CCN was made to the current contract in order to avoid additional delays in the development. The CCN expanded the development effort within this contract to cover all steps up to start of manufacturing of the device.

The following companies were involved in the development:

- Cobham Gaisler – Cobham Gaisler (Sweden) was the prime contractor and performed implementation of the NGMP VHDL design to the target technology, verification and validation.
- ST Microelectronics – The ASIC library design support and ASIC backend work has been performed by ST Microelectronics (France, United Kingdom)
  - The business unit handling the space market have headquarters in France
  - The backend team involved in this development are located in the United Kingdom
- Airbus Defence and Space – Airbus Defence and Space (then EADS Astrium) (France, Germany) were involved in the activity's specification phase where Airbus Defence and Space reviewed the specification and provided requirements.
- In anticipation of phase two of the NGMP development, Pender Electronic Design (Switzerland) has been involved in reviewing the proposed pinout of the device to be manufactured in phase two.

5 WORK PERFORMED AND MAIN RESULTS

The NGMP architecture has been specified, designed, verified and validated on FPGA prototypes. ASIC synthesis and back-end layout work has been performed for the ST Microelectronics C65SPACE ASIC platform. During the course of the activity several FPGA prototypes have been developed and delivered to end users.

Support for the NGMP architecture has been implemented for all operating systems and toolchains provided for LEON systems by Cobham Gaisler AB.

The target and packaging technology placed constraints on the parts of the NGMP architecture that could be implemented:

- The selected target technology did not allow to implement the high-speed serial links that are part of the NGMP specification, and envisioned to be used to support SpaceFibre.
- Lack of multi-standard I/Os prevented the two main memory interfaces (DDR2 SDRAM and SDRAM) from sharing pins and lack of suitable I/Os also prevented DDR2 SDRAM from being supported. The C65SPACE platform does not have strong bi-directional I/Os. This will limit the performance of the SDRAM interface. Cobham Gaisler has proposed and implemented mitigation measures for the slow I/Os provided by the target technology.
- Available package technology restricted the number of usable pins of the design and led to the implementation of pin sharing between interfaces, which means that all of the included interfaces cannot be active at the same time. Pin constraints also led to the removal of the USB debug link.
- The target technology has been characterised for a mission profile of a maximum operating temperature of 125° C and 20 year lifetime. This derates the timing performances and the target sign-off frequency is now 250 MHz instead of the initially specified 400 MHz.

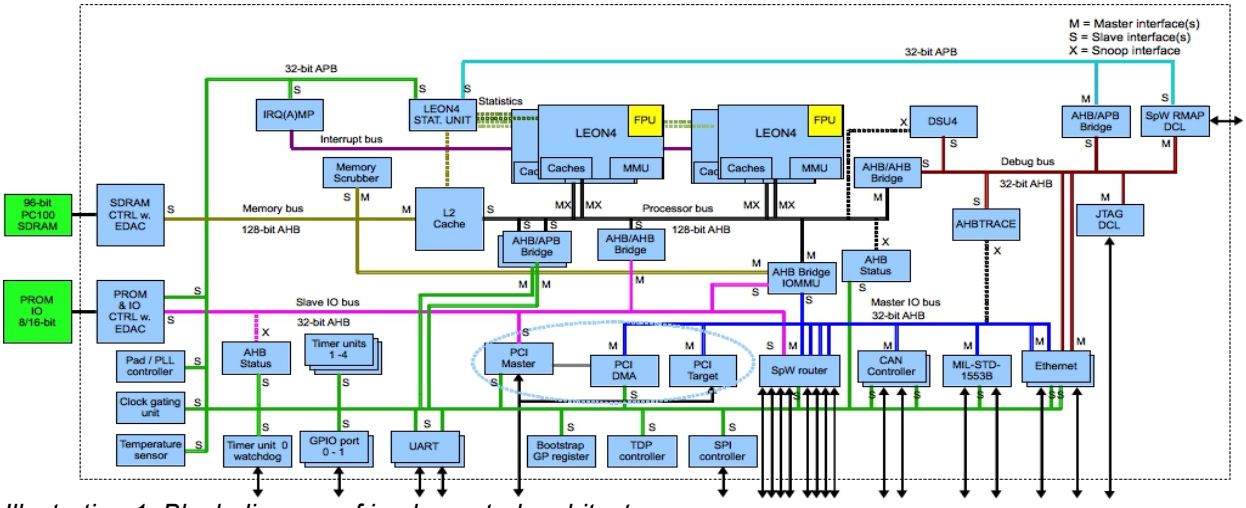

Illustration 1: Block diagram of implemented architecture

The resulting architecture is a multi-processor design with one shared 2 MiB Level-2 cache. Several design adaptions have been made to support both SMP and AMP operation. ESA and Cobham Gaisler has also collaborated with end users and research institutions in order to enable the use of the architecture not only in payload processor but also for platform application by including performance counters that will allow end user to analyse software behaviour and allocate budgets for critical and real time applications.

6 DELIVERABLES

The following deliverables have been produced within this contract:

- Architecture Exploration Report (D1)
- NGMP Specification (D2)
- Development Plan (D3)
- SEE Mitigation Plan (D4)
- Feasibility Report with Spreadsheet (D5)
- Software Requirement Specification (D6)
- Architecture Definition Report (D7)
- Verification Document with Verification Plan and Results (D8)
- Preliminary NGMP Data sheet (D9)
- Documentation of Changes/Configuration of OS, Compiler and the Drivers (D10)
- Technical note on NGMP evaluation (D11)
- Preliminary Radiation Report (D12)
- Technical Data Package (D13)
- Abstract and Executive Summary (D14)
- FPGA Board with FPGA Database (D15)
- High-level simulation models (D16)
- Architectural Design Database (D17)
- Separate databases, per selected OS and compiler, containing source, scripts, makefiles and object code of modified OS versions, specific configuration files (BSP) and drivers for the on-chip peripherals. (D18)
- Test Database with applications in source and compiled format, including all necessary scripts, makefiles and configuration files (D19)
- Detailed Design Database (D20)
- Detailed Design Document (TN-1)
- Layout Design Document Draft (TN-2)
- Preliminary Data Sheet for ST65 Prototype Implementation (TN-3)
- Bitstream for FPGA board – representative of full NGMP with functional enhancements (HW-1)
- Bitstream for FPGA board – representative of NGMP-lite as implemented as part of CCN2 to activity (HW-2)
- Final design database (DB-1)
- Detailed block diagram (added deliverable)
- ST65 ASIC Design Description (added deliverable)
- ST65 DFT Specification (added deliverable)
- GR740 Comparison Document (added deliverable)

7 CONCLUSIONS

The outcomes of this activity allows to start manufacturing of engineering models of the Next Generation Microprocessor architecture. As part of the NGMP activity and parallel activities the space community have been provided access to a quad-core LEON design through FPGA prototypes and the NGMP functional prototype evaluation board (GR-CPCI-LEON4-N2X).

The implementation and availability of the NGMP design has pushed the European space industry into considering more complex multi-core systems and this has resulted in additional research activities at both ESA and CNES. Progress for the NGMP development is reported at the ESA NGMP website [RD3]. The validation board product page on Aeroflex Gaisler's website is available at [RD4].

The NGMP will be commercialized under the product name GR740.