Monolithic Integrated GALILEO/GPS RF Front-End

Feasibility Study – Final Report

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ChipIdea® Microelectrónica, S.A.
Taguspark Edifício Inovação IV, Sala 733,
2780-920 Porto Salvo **Portugal**
Tel.: (+351) 210336300
Fax: (+351) 210336396
http://www.chipidea.com

Prepared by: Alcides Dias
Approved: Carlos A. Leme
Department: ICCE
Tel.: 351210336347
Fax: 351210336396
E-mail: adias@chipidea.com

Version History

Version	Date	Prepared	Description
1.0	2002-Dec-01	Alcides Dias	• Creation
1.1	2002-Dec-26	Nuno Ramalho	• Updated: Addition of simultaneous reception of L1+L2 and L1+E5a/E5b • Updated: Interference requirements
1.2	2002-Jan-09	Alcides Dias	• Updated: Synthesizer's architecture
2.0	2003-Jan-22	Nuno Ramalho	• Review

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1 Introduction

The GPS satellite navigation system consists of 24 satellites in low earth orbit, placed by the U.S. Department of Defense. The satellites continuously broadcast position and time. The terrestrial receiver compares the time difference between 3 satellites and calculates the position of the user. A spread spectrum technique is used in the transmission of the signal. In this approach the data is multiplied by a pseudo-random bit-stream code that runs at a higher rate (chip rate) than the navigation data rate. Using such technique every satellite can broadcast at the same frequency without interfering with each other.

GPS signals are broadcasted into both lower and upper bands, L2 and L5 centered at 1227.6 MHz and 1176.45 MHz respectively and L1 centered at 1575.42 MHz. Two different signals (P code and C/A code) are broadcasted in the L2 band while only P code is present in the L1 band. P code is for military use and the C/A is open for general mass public.

Galileo satellite navigation program is promoted by the European Union and the European Space Agency to reduce the Europe's dependency on the US GPS or Glonass. Four bands exist in Galileo; E5a (1176.45 MHz), E5b (1207.14), E6 (1278.75 MHz) and E2-L1-E1 (1575.42 MHz).

Four different types of data are transmitted in different bands:

- Open Services (OS) data is carried in E5a, E5b and E2-L1-E1.
- Commercial Service (CS) is broadcasted in E5b, E6, and E2-L1-E1.
- Safety-of-life Service (SoL) is present in E5b and E2-L1-E1.
- Public Relation Service is transmitted in E6 and L1.

The objective of this document is to present a feasible study for a low cost, low power solution of a Galileo/GPS RF Front-End Receiver for both terrestrial and space applications.

Description and analysis of the system requirements, architecture design and definition of the system and building blocks specification are presented in this document.

The system proposed will be designed to support simultaneous dual band reception including the following front-end stages:

- 2 re-configurable front-ends for L1 and L2 respectively
- 2 re-configurable front-ends for L1 and E5a or L1 and E5b respectively
- 1 re-configurable front-end for L1 and 1 front-end adapted to the reception of E5a+E5b together.

The report concludes with the proposal of a low risk, low cost and low power fully integrated solution in low cost deep-sub micron CMOS.

2 Technology

The market of portable communications has been rapidly increasing in the last decade. As a result, low-power, low cost and high-integration of both RF Front-Ends and digital circuits is the basic requirement of today communication system.

Most common technology used in RF are: GaAs, Bipolar and CMOS.

GaAs offers very good RF performance and good features such as high quality inductors and capacitors, high cut-off frequency and insulating substrate. But it's often viewed as a high-cost, high-power and low-yield process.

So far the Bipolar technology is the dominant process for commercial RF front-ends. Cost and the level of integration are not as attractive comparing to CMOS technologies. Traditionally, CMOS is confined to digital applications but in recent years the scaling process has offered dramatic improvements in the RF area. Table 2-1 shows some key performance parameters in several technologies and foundries.

Parameter	TSMC 0.35 SiGe	Atmel SiGe1	UMC 0.18 RFCMOS	Unit
Ft	40	30	45	GHz
Fmax	60	50	35	GHz
Q inductor	N/A	20 @ 2GHz	10 @ 2.4GHz	

Table 2-1

Although bipolar technology offers better performance over CMOS, the difference is quite small. For a design at frequencies of 1.6GHz a CMOS technology with an Ft of about 35GHz is adequate. Low cost and high integration make the CMOS option very attractive.

Various CMOS technologies are contenders for this application. Of these, UMC 0.18um CMOS with RF option is one of the most suitable.

UMC 0.18 um RFCMOS Features:

- Ft = 45 GHz
- Fmax = 35GHz
- Noise Figure : 0.6dB @ 2.4GHz
- Integrated Inductor : Q = 10 @ 2.4GHz
- Integrated Varactors : $\Delta C = 45\%/1V$
- Good model's characterization : Very good correlation with existing silicon. Chipidea has experience and very positive silicon results in this technology up to 5GHz transceivers

Figure 2-1 and Figure 2-2 show the gain and noise performance of UMC 0.18 RFCMOS. Figure 2-3 illustrates the quality of the UMC inductors.

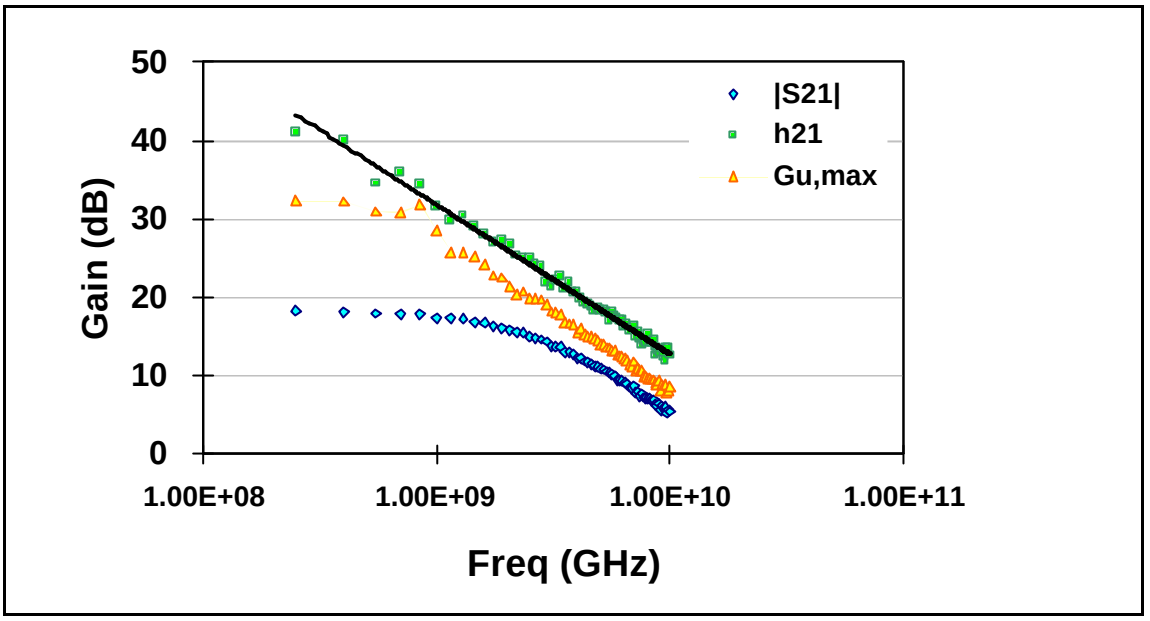

Figure 2-1. Gain vs frequency

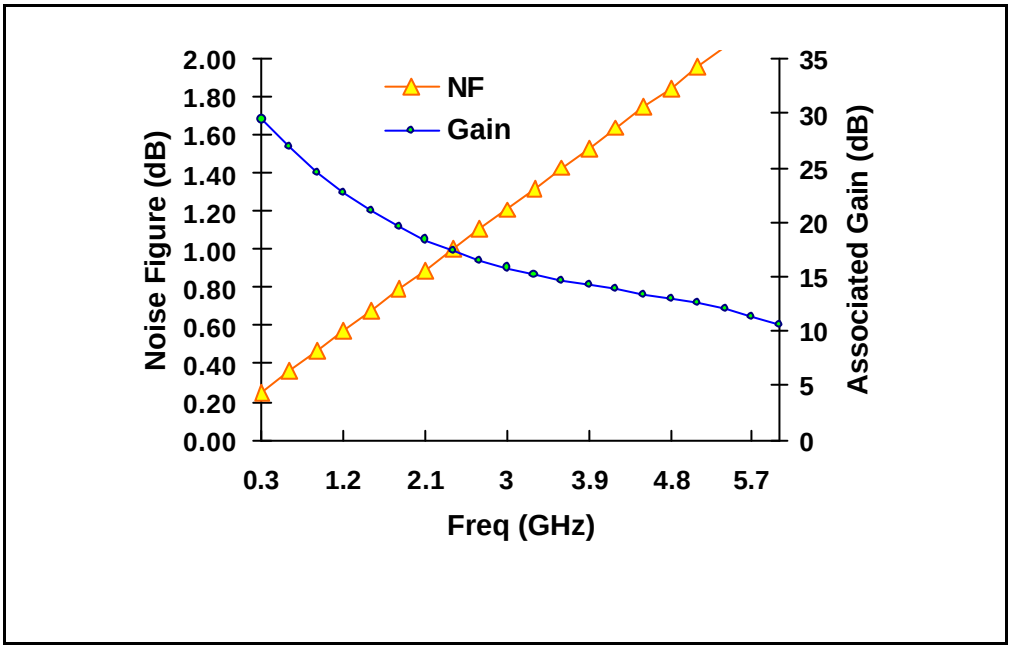

Figure 2-2. Noise vs frequency (UMC 0.18 RFCMOS)

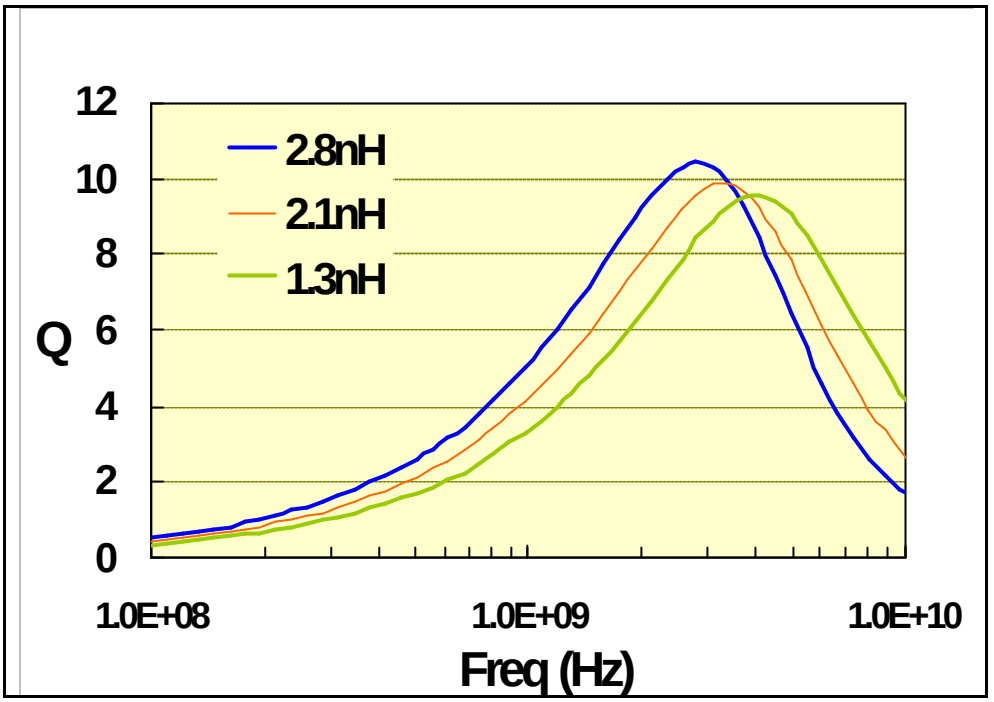

Figure 2-3. Inductor Quality (UMC 0.18 RFCMOS)

These figures illustrate the excellent performance that can be derived from this technology for RF circuits at 1.1 GHz or 1.6 GHz such as those required for Galileo/GPS applications.

CMOS technology has become increasingly popular for RF applications. Below is a list of some of many GPS products and papers in CMOS:

- iTRAX02 from FastraX
- RF8000 from RFMicrodevices
- VS7001 from Valence Semiconductor
- "A 115mW, 0.5um CMOS GPS Receiver with Wide Dynamic-Range Active Filters", Derek K.Shaeffer, IEEE JSSC, vol.33, No12, Dec 1998
- "Implementation of a CMOS LNA Plus Mixer for GPS Applications with No External Components", Francesco Svelto, IEEE Transactions on Very Large Scale (VLSI) Systems, vol. 9, No.1, Feb 2001
- "A 0.8dB NF ESD-Protected 9-mW CMOS LNA Operating at 1.23 GHz", Paul Leroux, Vol. 37, No. 6, Jun 2002

3 Architecture

The architecture widely used in commercial dual-band receivers is the double conversion (Figure 3-1). The two different input bands frequencies are down-converted into a common IF and then each is down-converted again to the base band. The choice of IF is based on the frequency differences between the two input bands. In a dual band system where the input bands are located at around 1.2GHz and 1.6GHz, the LO would be 1.4GHz and thus the IF is 200MHz. The drawbacks with this approach are the complexity, extra IF stages, image rejection and it requires two local oscillators that generally mean two frequency synthesizers. Such approach results in a complex, high cost and high power consumption solution.

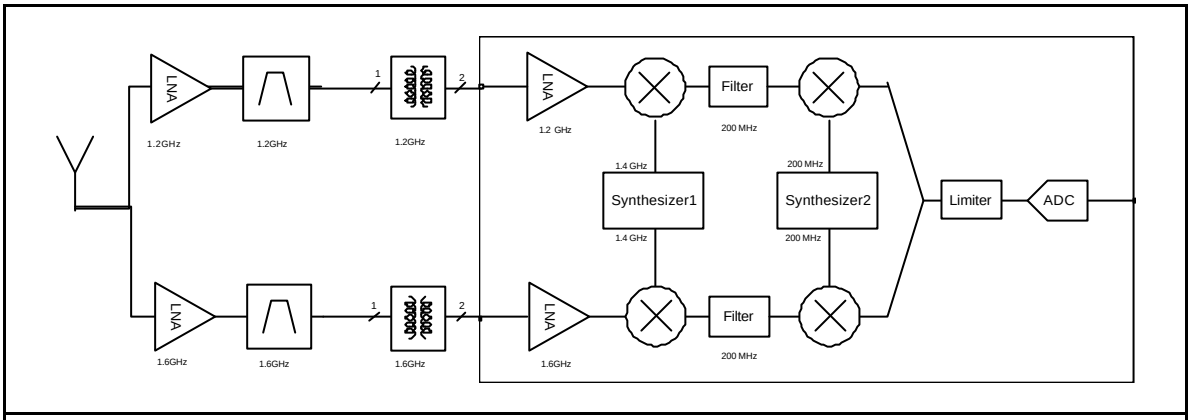

Figure 3-1. Conventional receiver for dual band application. High complexity, hi-power and not cost-effective

Meanwhile homodyne or direct conversion solutions have become very cost-efficient. The proposed architecture diagram for the Galileo/GPS Front-End is represented in Figure 3-2. This architecture is capable of receiving any of the bands by simply reconfiguring the input band of the LNA and the center frequency of the synthesizer. For simultaneous multiple band reception, the front-end can be simply replicated and tuned to a different channel.

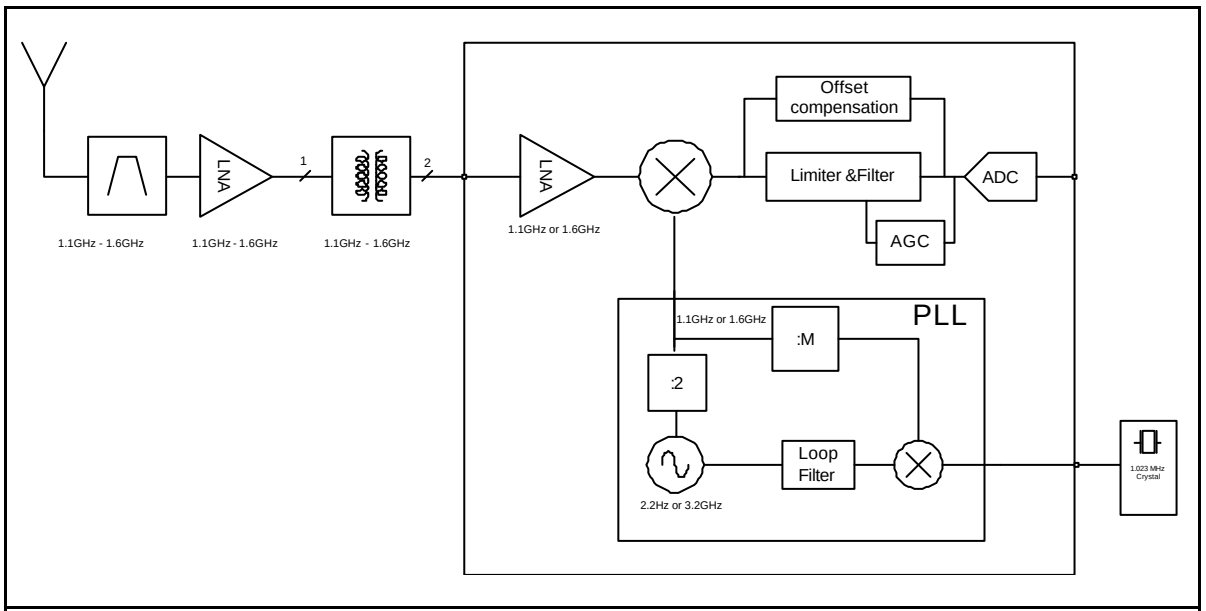

Figure 3-2. Direct conversion architecture with single synthesizer.

The IC consists of an internal LNA, I & Q mixers, frequency synthesizer with I & Q outputs, a limiter and a 2-bit ADC.

One of the major difficulties of the implementation of a direct conversion is to reduce the DC offset as a result of the self-mixing. In this proposed solution, the VCO works at double the output LO frequency. The I/Q signals can be constructed by dividing the VCO. The LO is the output of the div-2 prescaler.

The fact that the VCO is not oscillating at the signal's band has the advantage that the strong VCO's signal can't be self-mixed which would cause DC problems. This is a significant advantage of the proposed solution over many other direct conversion techniques.

Band	VCO's frequency (MHz)	Divider Ration	LO frequency (MHz)
GPS L1	3150.84	2	1575.42
GPS L2	2455.2	2	1227.6
Galileo L1	3150.84	2	1575.42
Galileo Ea5	2352.9	2	1176.45
Galileo Eb5	2414.28	2	1207.14

Table 3-1

3.1 Sensitivity

Although this approach results in an extremely compact, low-cost, low-power and high performance solution, it presents one challenge: the very low noise figure required by the input stages.

The input signal power spectrum is lower than the noise spectrum, which is a characteristic of the spread spectrum. As an example, the signal level power of the GPS L1 band is –128 dBm and the noise power over 24MHz is –100 dBm, thus the input SNR is –28dB. This SNR is improved when an appropriate code is applied to the signal. This gain is called processing gain which is given by:

$$G_p = 10 \cdot \log\left(\frac{fc}{fb}\right) = 43dB$$

Where fc (1.023 Mbps) is the chip rate and fb (50bps) is the bit rate. After processing, the total SNR is equal to 15 dB. Assuming that at least 10 dB of SNR is needed for demodulation, the remaining 5 dB is the target noise figure for the system. This example is in fact the most stringent requirement for all the bands. For the bands E5a and E5b the resulting SNR is 5dB more relaxed (this will be useful later in the proposal of simultaneous reception of E5a and E5b). Table 3-2 shows signal levels of GPS/Galileo in different bands.

	Galileo							GPS		
	L1			E5a		E5b		L1		L2
f (MHz)	1575.42			1176.45		1207.14		1575.42		1227.6
P (dBm)	-122			-125		-125		-128.239		-136
	A	B	C	I	Q	I	Q	I(C/A)	Q(P)	I(P)
BW (MHz)	24	24	24	32.736	32.736	32.736	32.736	24	24	24
CR (Mcps)	5.115	2.046	2.046	10.23	10.23	10.23	10.23	1.023	10.23	10.23
DR (sps)	300	250	0	250	0	250	0	50	50	50
Gp (dB)	42.31724	39.12966		46.11936		46.11936		43.10906	53.10906	53.10906
input SNR	-21.8021	-21.8021		-26.1503		-26.1503		-28.0411	-28.0411	-35.8021
SNR + Gp (dB)	20.51513	17.32754		19.9691		19.9691		15.06794	25.06794	17.30694
NF (dB)	10.51513	7.327544		9.9691		9.9691		5.067944	15.06794	7.306944

Table 3-2

In others words, the system noise figure can be calculated using the following formula.

$$NF = Pin - Pnoise + Gp - SNR$$

Where the Pin is the input signal power, the Pnoise the input noise power, Gp is the processing gain and the SNR is the required SNR for proper demodulation. Substituting the values the system NF is equal to:

NF = -128 – (-100) + 43 – 10 = 5dB

The total noise figure can be calculated using the Friis equation [1] based on the values of the gain and noise figure of each stage. It demonstrates that the most critical bocks are the first few stages. The key of the design is to place a low noise and high gain stage at the input of the receiver.

3.2 Gain Plan

As seen in the previous section, the noise is the bottleneck of the system requirement. In the worst case, band L1, only 5 dB of system noise figure is allowed which is very difficult to achieve using CMOS. To alleviate this difficulty, a low-cost single external LNA is a good solution. Its gain relaxes the noise requirement of the IC. An input RF filter, although not absolutely necessary, improves the overall system performance by suppressing out-of-band interferences.

Table 3-3 shows the receiver gain plan. From the table it is clear that the system noise is dominated by the input filter and by the external LNA.

The total cascaded gain is about 100dB, which is enough to amplify the satellite's signal to a detectable level while the noise does not become too strong to saturate the output.

		Input Filter	External LNA	balun	Internal LNA	Rf to zero mixer	Limiter (3-stage)	Cascaded TOTAL	Units
Gain (df< B/2)	**G**	**-2**	**13**	**-2**	**16**	**12**	**60**	97.0	dB
Noise Figure	**NF**	**2**	**1.8**	**2**	**5**	**20**	**20**	4.8	dB
NF (linear)	NF	1.58	1.51	1.58	3.16	100.00	100.00		
Gain (linear)	G	0.79	4.47	0.79	6.31	3.98	1000.00		
Pre-stage Gain		1.00	0.79	3.55	2.82	17.78	70.79		
Noise Terms		1.58	0.81	0.05	0.27	0.31	0.02	3.05	
Min. Input	Pin(min)	**-136**	-138	-125	-127	-111	-99	-39	dBm
	vin	100.2E-9	79.6E-9	355.7E-9	282.5E-9	1.8E-6	7.1E-6	7.1E-3	V
noise	Pin	**-100**	-102	-89	-86	-70	-58	2	dBm
filter rejection	P	**-20**	0	0	0	-14	-42	-76	dB
blocking @200MHz	P	**-30**	-52	-39	-41	-25	-27	-9	dBm

Table 3-3

3.3 Blocking performance

Galileo specifies that Open Service Performance shall be achieved with any level of external interference power density at the receiver input up to –141.3 dBW in any 1 MHz band. After a gain stage of 100dB, this is equivalent to –41.3dBW or –11.1dBm. Such level of interference is well below the dynamic range of the ADCs and will not saturate any stage in the receiver chain.

Nevertheless, in order to be immune to stronger interferers, some kind of filtering should be present at the receiver. The receiver must be a robust solution against any interferer from others systems, especially in terrestrial applications. A reasonable blocking specification is assumed (Table 3-4).

Frequency	Blocking Input Power	Unit
0 – 900 MHz	-30	dBm
1800 – 5000 MHz	-30	dBm

Table 3-4

After the mixer the out-of-band blocking signals are translated to a few hundred MHz. These signals can saturate the following stage and can interfere with the zero-IF signal due to the aliasing effect at the ADC. The proposed ADC sampling frequency is 65.472 MHz. So the blocking signals must the filtered out before entering the ADC. One of the specifications of the limiter is the filter rejection at 200MHz.

3.4 In phase & quadrature outputs

After the mixer the signal is treated as a complex signal, this means the signal has two components: in-phase (I) and in-quadrature (Q). With the exception of the LNA each block in the receive chain is actually two matched circuits, each one works for one of the signal components (I & Q). Thus, the receiver has two 2-bit ADC outputs.

The two 90º phase shifted LOs are generated by the synthesizer as explained in section 4.10. The image rejection depends mainly on the matching between the I and Q paths. In an integrated solution the rejection achievable is at least 25-30dB.

3.5 Simultaneous reception of two bands

One added advantage of the architecture proposed, is that it is fully reconfigurable to receive any of the channels. Consequently, simultaneous reception of two channels can be easily achieved by simply replicating the receiver and programming each receiver for the bands desired. Figure 3-3 illustrates a solution for a receiver capable of dual reception of upper and lowers band simultaneously. The external narrow band filters and LNA effectively filter and amplify any unwanted out-of-band signals before entering the chip.

This proposal is capable of receiving band E2/L1/E1 on one channel and any of E5a, E5b and L2 on the other channel.

Reception of E5a+E5b simultaneously on a single channel can also be achieved by centering the LO between the two bands (at 1191.795 MHz). After down conversion, both bands will be superimposed between about DC and 25 MHz. Because the signals are uncorrelated, it is possible to detect the individual signals even though they are superimposed. This approach deteriorates the SNR by 3dB. This may be acceptable because, as indicated in table 3-2, the system needs to be dimensioned for the worst case SNR of 15dB in the band L1 whereas the SNR in the bands E5a and E5b is approximately 20dB.

The resulting SNR from the proposal above can be further improved by filtering the bands E5a and E5b separately with poly-phase filters. After down conversion with I & Q to base-band, the band E5a will be located in the negative frequencies and the band E5b will be located in the positive frequencies. Consequently, the two bands can be distinguished via asymmetric band-pass poly-phase filters. Figure 3-4 illustrates this proposal.

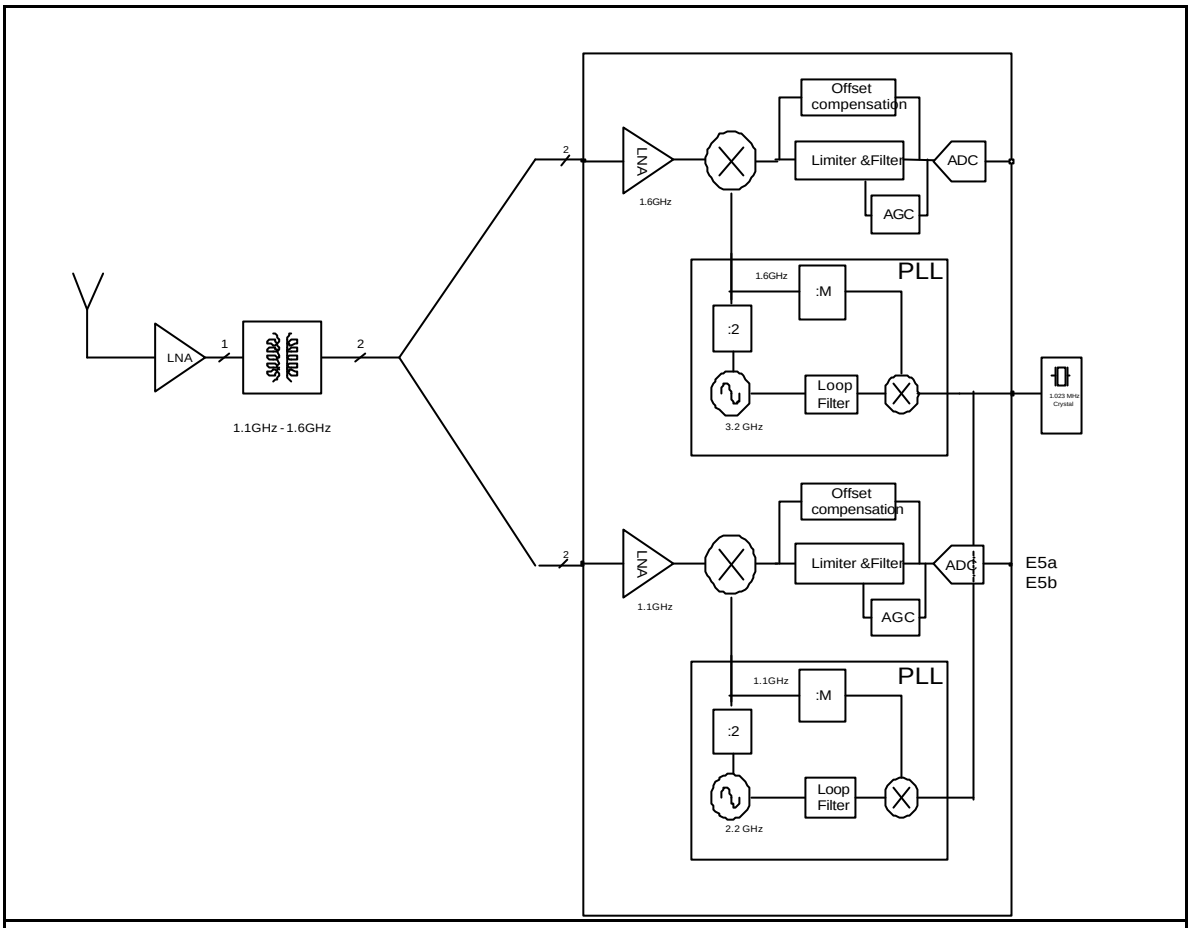

Figure 3-3. High out-of-band rejection for the reception of upper and lower bands simultaneous.

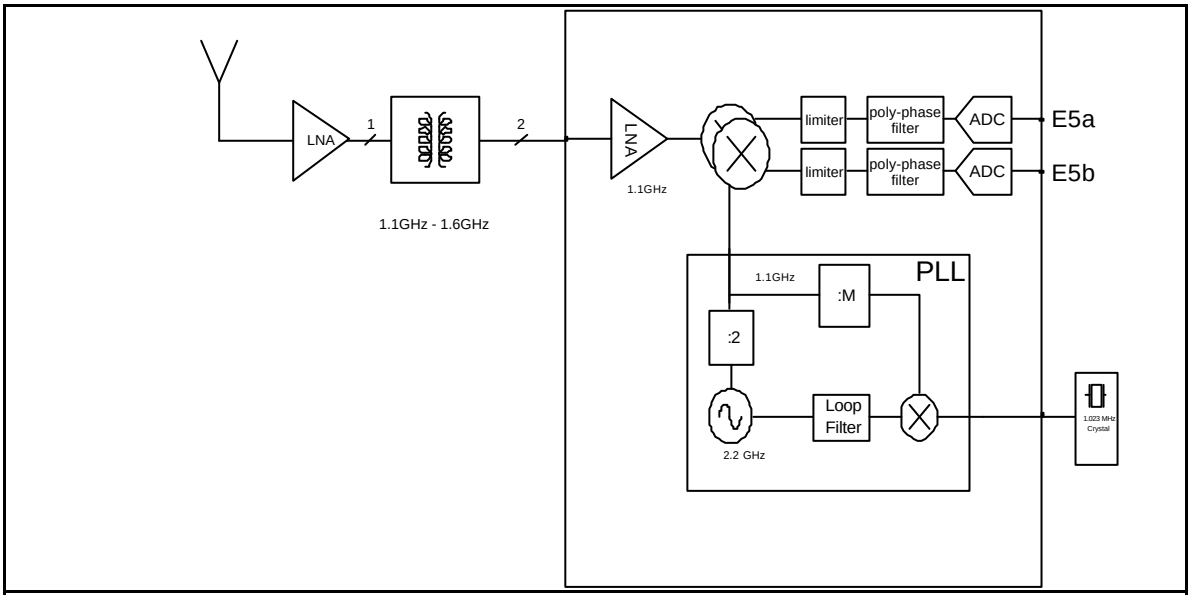

Figure 3-4 Reception of E5a and E5b bands on a single channel with poly-phase filtering and independent ADCs.

4 System & Circuits

4.1 Input Filter

The RF input filter requirement is rather simple. Due to the homodyne architecture no image filtering is required. As mentioned earlier, the filter is only intended to suppress out-of-band interference. The major concern is the insertion loss, since any loss at the input stages of the receiver degrades the total noise figure. Table 4-1 shows the specs and characteristic of the RF filter.

Parameter	Value	Unit
BW (f1 – f2)	1100 – 1600	MHz
Insertion Loss (dB)	2	dB

Table 4-1

4.2 External LNA

The external LNA plays one of the most important roles in the design. It relaxes the noise requirements of the IC. High gain and low noise are the main requirements. Since it's one of the first stages in the architecture it does not require high linearity and interferer immunity. Table 4-2 shows the characteristics of some commercial RF LNAs.

LNA	Band (MHz)	Gain (dB)		Noise (dB)		Current consumption
RFMD RF2371	700-2000	17.0 @ 900MHz	12.5 @ 1950 MHz	1.6 @ 900 MHz	1.6 @ 1900 MHz	2.9mA @ 2.7V
RFMD RF2442	700-2500	20.0 @ 900MHz	12.0 @ 1950 MHz	1.6 @ 900 MHz	1.6 @ 1900 MHz	12 mA@ 3.0 V
Agilent MGA-87563	500-4000	14		2.0		4.5 mA @ 3.0V

Table 4-2

4.3 Internal LNA

The architecture chosen for the LNA is the L-degeneration as shown in Figure 4-1. It has high performance low-risk and is very well known and documented in the scientific community. It is also the most used topology in CMOS LNAs.

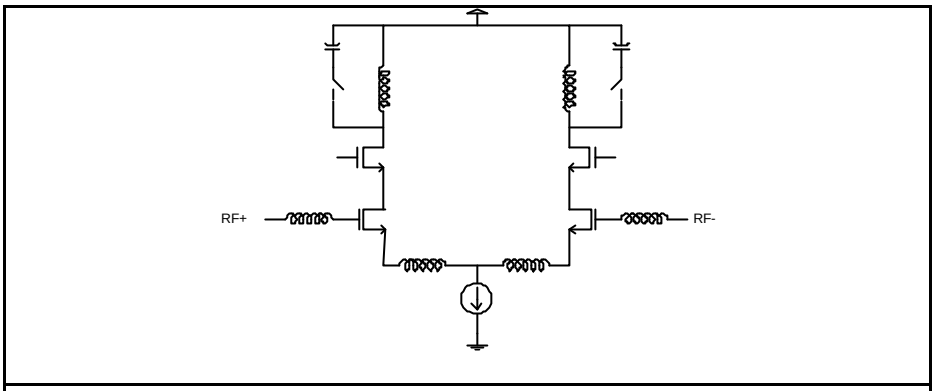

Figure 4-1. L- degeneration topoloty

Preliminary simulations were done to assure the feasibility of the LNA proposed. The plots of the gain and noise figure are shown in Figure 4-2 at both 1.6GHz to 1.2GHz frequencies. The noise plot shows the NF the value is below 3 dB.

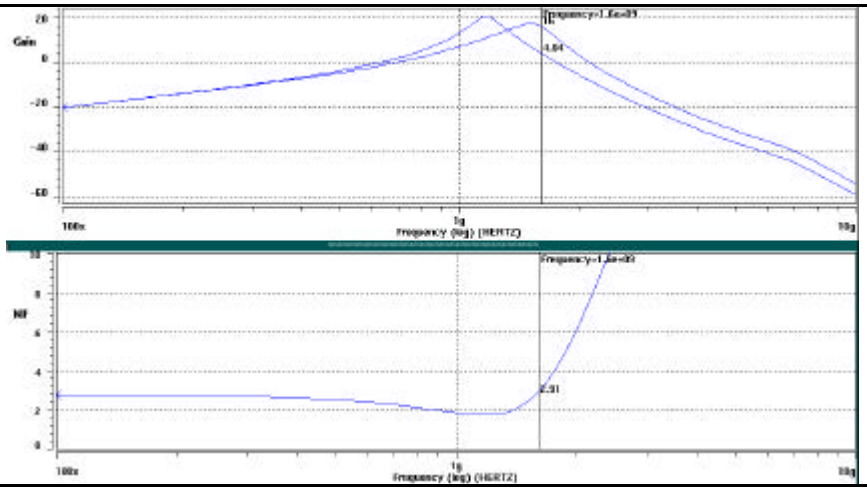

Figure 4-2. LNA's Gain and NF. The NF is independent to the load capacitance.

The specifications for the LNA can be relaxed to the values presented in Table 4-3:

Parameter	Value	Unit
Gain	16	dB
S11	-10	dB
Noise figure	5	dB
1dB input compression point	-32	dBm

Table 4-3

4.4 Mixer

Mixers are responsible for the frequency translation. Mixers can be divided into two groups: passive and active. Passive mixer is not suitable for this application because passive mixers do not have gain and require large LO signal. To avoid the use of extra amplifiers, active mixers are proposed.

The requirements for the mixer are (Table 4-4):

Parameter	Value	Unit
Gain	12	dB
LO to RF isolation	30	dB
Noise figure	20	dB
1dB input compression point	-16	dBm

Table 4-4

The port isolation is very important because one of the problems in zero-IF architectures is self-mixing. If the LO signal is coupled to the input of the mixer, it then mixes itself with the LO it-self to create a static DC signal at the output. As described above, this problem is greatly reduced by placing the VCO frequency much above the RF frequency.

The mixer architecture proposed for the receiver (Figure 4-3) is a Double Balanced Gilbert cell. The output stage forms a pole which helps to filter any spurious or unwanted signals. The output bandwidth can be designed to be 40MHz.

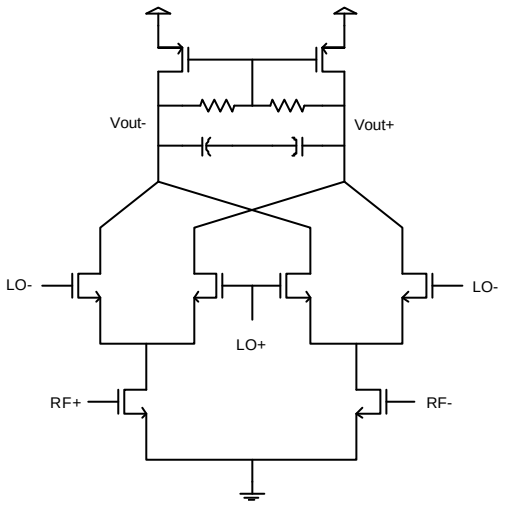

Figure 4-3. A suggested mixer architecture

Preliminary simulation results of the mixer are shown in Table 4-5.

Parameter	Typ
Gain	10 dB
Noise Figure	16 dB
Bandwidth	40 MHz

Table 4-5

4.5 Limiter

The limiter amplifies the small signal at the output of the mixer to a detectable signal at the input of the ADC. It also filters any high frequency blocking signals. The proposed limiter consists of three stages of open-loop amplifiers. Each amplifier has around 20dB of gain and the output stage is a 1st order RC filter, forming a pole around 40MHz.

Parameter	Typ	Unit
BW	0 – 40	MHz
Gain	60	dB
Att @ 200MHz	40	dB
NF	30	dB
Output 1-dB compression point	6	dBm

Table 4-6

A proposed implementation for one limiter stage is illustrated in Figure 4-4. It consists of a transconductor and an output RC load. The input transconductance value is equal to 1/Re. Then it's mirrored to the output stage with a current gain of M. This will relax the consumption requirement for the input stage. The resistor Ro and capacitor Co form the output impedance, where the RC product defines the output bandwidth.

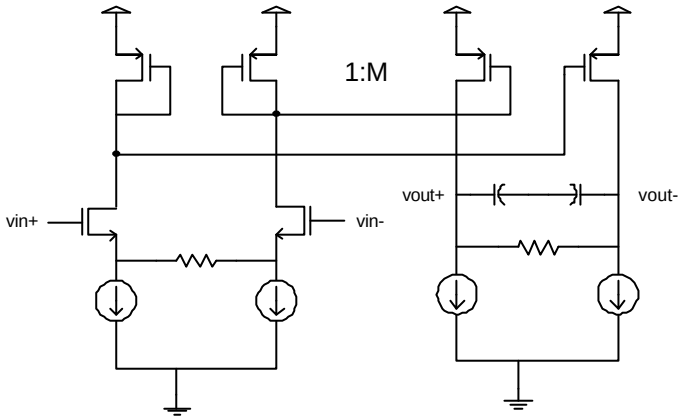

Figure 4-4. The proposed limiter architecture

4.6 Filter

The GPS L1 consists of two signals (P and C/A). The C/A bandwidth is about 2MHz and is 10 times narrower than the P code signal. The equivalent noise bandwidth for the C/A signal can be as low as 2MHz. To maximize the SNR, a filter with 2MHz bandwidth can be applied to the signal. But for a P signal the filter's bandwidth should be 20MHz.

4.7 Offset compensation

Miss-match and LO self-mixing creates a static DC offset which can be amplified by the following stages and may saturate the output stage. A DC offset compensation circuit can be implemented to avoid this situation as Figure 4-5.

The compensation circuit continuously measures the DC offset at the output and then injects or retrieves current at one of the input stages to cancel the error at the output. This is equivalent to a high-pass filter. But in a zero-IF architecture this could be troublesome, because some wanted signal will also be filtered. So the high-pass corner frequency must be sufficiently low.

Alternatively, an offset calibration loop is used, triggered by the baseband processor at the start of reception.

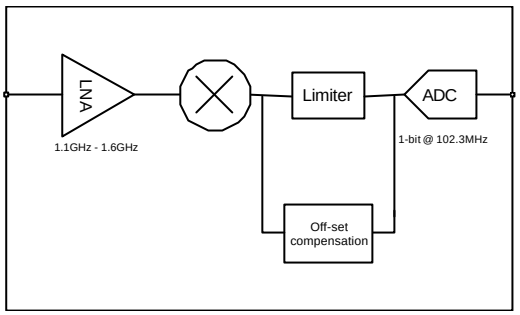

Figure 4-5. DC compensation scheme.

4.8 AGC (Automatic Gain Control)

Due to process variation, the signal level at the ADC's input can suffer variation of a dozen dBs. Too much gain can saturate blocks. On the other extreme, the signal can be too small for proper detection. The purpose of the AGC is to correct the variation of the receiver gain. The AGC measures the input power level of the ADC and then compensates it by changing the gain of the receive path.

The gain of the LNA plus mixer can suffer a variation of +/- 10dB, thus the proposed AGC should be capable to cover this variation. The AGC should detect the signal level at the input of the ADC and then increase or decrease the gain of the limiters depending the signal level. Table 4-9 shows the specification of the AGC.

Parameter	Value	Unit
Minimum detectable signal	200m	V
Maximum detectable signal	2	V
AGC Range	36	dB
AGC step	6	dB

Table 4-7

4.9 ADC

Two bits ADC with over-sampling is proposed. The noise is amplified to the full-scale level and the signal is about 36dB lower. The ADC must have good sensitivity to detect the signal. Assume full-scale is equal to 1V then 36dB lower is 15.8mV. Switched capacitor comparator with DC-offset compensation can achieve an offset error of 1mV up for a sampling frequency to hundred of MHz.

The proposed sampling frequency is 65.472 MHz or 64 X 1.023 MHz

Parameter	Typ	Unit
Sampling frequency	65.472	MHz
Offset	1	mV
Number of bit	2	bit

Table 4-8

4.10 Frequency Synthesizer

The proposed synthesizer architecture is shown in Figure 4-6. The VCO works at double of the LO frequencies.

Band	VCO's frequency (MHz)	Divider Ration	LO frequency (MHz)
GPS L1	3150.84	2	1575.42
GPS L2	2455.2	2	1227.6
Galileo L1	3150.84	2	1575.42
Galileo Ea5	2352.9	2	1176.45
Galileo Eb5	2414.28	2	1207.14

Table 4-9

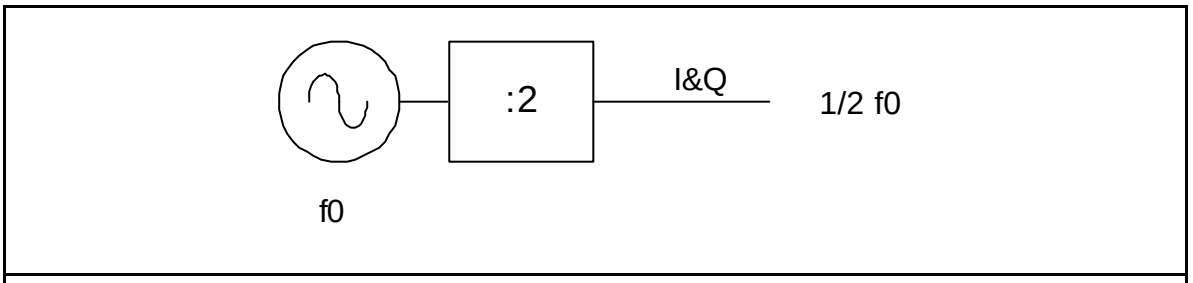

Figure 4-6. The 1.2 GHz and 1.6GHz LOs are the dividers outputs.

The advantage in this design is that quadrature outputs are inherent in any div-2 dividers and therefore, no RC-CR poly phase filter is needed to create the quadrature LOs. Poly phase filters are very power consuming circuits.

Another advantage is that the VCO is not working at the same frequency as the LOs, and therefore, the leakage of the strong VCO signal will not transform in to self-mixing product resulting in large DC offset.

The synthesizer is also responsible to generate the ADC clock. The sampling ratio is 64Xfref = 65.472 MHz.

The key performance parameters of the VCO are summarized below (Table 4-10):

Parameter	Value
Reference frequency	1.023 MHz
LO frequencies	1176.45 MHz 1207.14 MHz 1227.6 MHz 1575.42 MHz
Image rejection	25 dB

Table 4-10

5 Cost Analysis

The cost analysis of the IC presented in this section refers specifically to a single receiver for one band. For simultaneous dual band reception, the receiver and synthesizer must be duplicated.

5.1 Current consumption

The current consumption of various components used by the receiver is shown in Table 5-1. The total consumption is 44mA at 2.5V where 38mA is from the chip. If two LNAs were used for better performance (one LNA at 1.2GHz and the other at 1.6GHz) the total consumption would increase by another 3mA.

block	current (mA)
RX	
LNA	3.5
mixer	1.5
limiter	1.5
ADC	0.5
PLL	
VCO	3.5
Prescaler	6
cp, lf, digital div	1
References	1.5
Total IC (single band)	**19**
Total IC (dual band)	**38**
external LNA	3
Total (mA)	**41**

Table 5-1

5.2 Die Area

Estimated area of each block of the IC is shown in Table 5-2. The total core area estimate is 6.92 mm2, resulting in the chip area (including pads) of about 10.44 mm^2.

block	Area for Single channel(mm2)	Area for dual channel(mm2)
LNA	1	2
Mixer	0.15	0.3
Limiter + ADC	0.8	1.6
VCO	0.4	0.8
presc	0.06	0.12
pll-mixers	0.3	0.6
digital div, cp, lf	0.3	0.6
Ref	0.35	0.7
digital, misc,...	0.2	0.2
core	3.56	6.92
pads	2.62	3.52
total	**6.18**	**10.44**

Table 5-2

5.3 BOM

Typical price of external components is shown in Table 5-3.

	wide band		
Unit	No. Unit	cost/unit	cost
input filter	1	**3.5**	**3.5**
combiner			
ballun	1	0.5	0.5
External LNA	1	0.63	0.63
crystal	1	0.2	0.2
LDO (1)	2	1.1	2.2
capacitor	10	0.06	0.6
inductor	2	0.3	0.6
resistor	6	0.033	0.198

Total (US$)	**8.428**

(1) LDO may not be required if the system already has 1.8V and 2.5V supplies available.

Table 5-3

The estimated cost of the components needed for the Front-End is below 8.5 US dollars.

6 Summary & Conclusion

The most important points for the implementation of the Galileo/GPS RF Front-End receiver were presented in this document. Novel, low risk, techniques were presented to solve or improve existing challenges in the integration of low cost low power receivers in standard digital deep-sub micron CMOS technologies. A fully reconfigurable receiver is proposed which can be programmed to receive any of the Galileo/GPS L1/L2/E5/L5 bands. Reception of multiple bands simultaneously can be achieved by simply replicating the receiver and reprogramming it for a different band. The proposal is summarized below:

- Tecnhonoly : UMC 0.18 um RFCMOS
- Architecture per channel:
  - Direct conversion
  - One frequency synthesizer
  - External LNA and external input filter
- Total Consumption per channel:
  - IC (per band): 19mA @ 2.5V
  - IC (two band simultaneously) with external LNA: 41mA
- Cost:
  - External components: below 8.5 dollars

It's shown that a low cost and low complexity but high performance receiver is achievable when combined with an external LNA. Such approach, when implemented in low-cost standard CMOS, is the lowest cost solution for a combined Galileo/GPS front-end receiver.

7 References

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