

ADV ENGINEERING	Microcontroller for On-Board Data Handling ESTEC Contract N° 12 396/97/NL/FM(SC)	MIC/TP.67.002/En	
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Titre/Title
Final Report Microcontroller for On-Board Data Handling

EUROPEAN SPACE AGENCY CONTRACT REPORT The work described in this report was done under ESA contract Responsibility for the contents resides in the organisation that prepared it	
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1 INTRODUCTION

1.1 Purpose and Scope

The purpose of this document is to presents the lessons learned from the Microcontroller for On-Board Data Handling activity.

The scope of this activity was to assess the 8031/32 microcontroller cores available on the market, to select and validate one and finally to develop, based on this macrocell, a customised microcontroller suitable for space application. Many space projects would benefit from the availability of such low power single-chip microcontroller for low-end applications. Typical applications are antenna pointing controllers or data handling computers for micro-satellites and more generally applications with moderate processing requirements but needing high safety and easy accommodation of equipment interfaces.

Therefore ADV Engineering has proposed to develop a microcontroller based on this well-known Intel 8052 device in the frame of an ESA activity. This project was interesting on 2 aspects. First aspect is the use of an Intellectual Property to design an ASIC which was never performed before by the company and which is a new approach we should be used more and more often in a next future. Second aspect was to deal with microcontroller technology, which will also be more and more, used in future products.

This document focuses on the activities related to the microcontroller core since the customisation phase is quite similar to a normal ASIC development in which the microcontroller is a block as any other sub-block. Recommendations to those buying IP cores are also presented. A general presentation of the product will be found in an annex.

1.2 Background

Very high integration levels of microelectronics will be required to fulfil the ever-increasing demands on performance in terms of processing speed, mass and power. With an increasing number of available gates on an Application Specific Integrated Circuit (ASIC), the functionality being implemented will move away from the use of traditional components to more advanced and complex systems within a single device. To develop such complex the design methodology will have to change from being gate-level oriented to the integration of complex building blocks. The designers will have to rely on existing building blocks with already verified functionality, with documentation and production test vectors being available, which has ultimately been validated on silicon. Today there are many companies offering Intellectual Property (IP) blocks or synthesisable VHDL cores which they have developed for a particular application and which they are now commercialising.

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The justification for developing an 8032 device is based on previous experience with the use of commercial components, especially microprocessors and microcontrollers. The commercially available devices do not always meet the harsh environment experienced in space since not manufactured in a radiation tolerant or radiation hard technology. Traditionally, microcontrollers were bought from the US, resulting in difficulties due to export regulations of radiation hard products. Another problematic aspect of buying parts from the US is that European space industry has little or no influence on the functionality of the devices when specified and designed, which has sometimes led to less than optimal system solutions. Microcontrollers suitable for space usage have been around, but most often in the form of company proprietary items.

The 8032 core purchased in this activity is based on an architecture developed by Intel (US), but the actual synthesisable VHDL core has been developed by R.Watts (UK). By having both a European core and a future radiation tolerant device, the European space industry could fully benefit from both a widely used Intel 8051 microcontroller platform and functions dedicated to space applications.

1.3 Footnote

When discussing an 8051 microcontroller one normally refers to a microcontroller complying with the Intel 8051 architecture and instruction set. When discussing an 8052 one refers to the same type of microcontroller but with additional standard peripherals. For actual implementations, an 8051 or an 8052 normally includes an on-chip Read Only Memory (ROM). If this ROM is not included one normally would use the terms 8032 or 8031, respectively, depending on whether the standard peripherals are included or not.

In this development, a design and an FPGA implementation of an 8032 was performed, i.e. there was no ROM included. In addition, several space specific peripherals and a memory protection function were developed. The final name selected for the design was ADV 80S32, where ADV is obvious and the letter S stands for space. It is believed that in the future the design will be simply referred to as the 80S32.

1.4 Acronyms and abbreviations

ASIC	Application Specific Integrated Circuit
CCSDS	Consultative Committee for Space Data System
DMA	Direct Memory Access
IO	Input/Output
IP	Intellectual Property
OBC	On-Board Controller
RAM	Random Access Memory
ROM	Read Only Memory
RTL	Register Transfer Level
UART	Universal Asynchronous Receiver Transmitter

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USART Universal Synchronous Asynchronous Receiver Transmitter
 T.B.D To Be Defined
 T.B.C To Be Confirmed
 VHDL VHSIC Hardware Description Language,
 VHSIC Very High Speed Integrated Circuit

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2 MICROCONTROLLER CORE SELECTION

The first phase of the project was to assess the different microcontroller cores available on the market. We have first identified seven potential core providers, however four of them provided licenses only for a given technology and were not suitable for this project.

The selection was made between three macrocell providers:

- ?? 3-SOFT (MENTOR);
- ?? R. WATTS;
- ?? SYNOPSYS.

The three candidates have been evaluated on technical, commercial and industrial criteria, which are summarised in the table hereafter:

	SYNOPSYS	3-SOFT/MENTOR	R. WATTS
Licensing conditions			
- Costs first use	65 K\$	60 K\$	40 K\$ +15 K\$
- Cost re-use	25 K\$ (if 3 orders before 30/06/98) otherwise 61500	36 K\$	15 K\$
- Technical support & bug fixing Bug fixing	reasonable effort	within 30 days	Estimation of the modification effort in one day.
Hot-line	10 K\$ for 60 hrs phone support	included in maintenance	included in maintenance
Maintenance	14 K\$ per year	1 st year included, 9K\$ per year	8 K\$ per year
Training	2 days included	TBD	3 k\$ for 2 days
Number of previous designs	Not communicated	9 references identified in volume production	2 references under development + Altera FPGA
Documentation	data book	data sheet + read me file	data book
Verification stimuli	RTL test bench with collection of 8051 programs and set of expected results	VHDL test bench with simulation script and simulation reference file	Test bench with Simulation script and expected results
Compatibility with MCS-51	yes	yes	yes
Processor speed (ref. 8051)	2.5 x	1 x	3 x
Power Consumption	Not communicated	Not communicated	70 mW at 36 MHz
Design complexity	14818 on 0,6 μ gate array 11712 on 0,6 μ standard cell	8000 gates for CBA library from Synopsys	9900 gates on 0,6 μ at 36 MHz and 11500 gates at 70 MHz
Fully synchronous design	Yes	yes	yes
Inclusion of hardware structures	yes	yes	yes
Testability support	Scan insertion	Scan insertion	Test vectors giving

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		95 % fault coverage
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Depending on the macrocell provider it was more or less difficult to obtain all the information needed to assess the macrocells. It is fairly easy to obtain functional information about the macrocell, each provider distributing freely its data sheet. However it is more difficult to have information on the estimated consumption and maximum speed for a reference process. It is also difficult to obtain clear information about how many ASIC/FPGA including the macrocell have been designed and if some of them are in the production phase.

To perform the final choice, the commercial, industrialisation and technical aspects have been classified as presented in the table hereafter.

Criteria	SYNOPTSYS	3 SOFT/MENTOR	R. WATTS
COMMERCIAL	- - high price, long response time of sales people	+ medium price, short response time of sales people	++ low price & short response time of sales people
INDUSTRIALIZATION	+ collection of 8051 assembler program to test all instruction set opcodes, data book - SCAN insertion for testability, only Synopsys script available	+ silicon proven, synthesis scripts available for Mentor, Synopsys - SCAN insertion for testability	+ test vectors for testability, synthesis script available for Synopsys, Compass - Only implemented in ALTERA FPGA
TECHNICAL	+ high performance, Dallas chip compatible	- low performance (Dallas chip compatible under preparation)	+ high performance

By analysing the pros and cons of each macrocell, R. WATTS was chosen because of the best price/performance ratio. The main drawback of the 3-SOFT offer was that its macrocell had an instruction execution time 3 times greater than the R. WATTS macrocell, while for SYNOPTSYS the main drawback was its price and its slow commercial response.

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3 CORE PROCUREMENT, VALIDATION AND RECOMMENDATIONS

3.1 Procurement and licensing

The selected macrocell has been procured by ESTEC, which is the IP owner. The procurement price was 40000\$ including the right to breadboard applications but not to design an ASIC.

Starting from 0.0c -0.- s q 1 0 0 1 -0.24 -0.24 cm 0.75 w 1 j 0 0 0 RG 3.75 -28 and licensin-

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To verify the program execution, we had to identify which are the good observation points. Regarding the 8032 structures and instructions set, the internal and external memory with some internal registers have been identified as the observation points. An observation procedure has been included in the randomly generated program after each sequence of 10 instructions, which calculates a checksum with the value of all the observed points and accumulates the results obtained at each execution of the procedure. At the end of the program the accumulated value represents a test signature.

More than 35 programs representing more than 1 000 000 instructions have been elaborated and executed both on the VHDL model and on the reference device a P87C52EBPN from INTEL. For each signature difference, the program execution has been traced both on the VHDL model and on the emulator, to find the instruction causing the difference.

The result of this activity has demonstrated its efficiency, since it has enabled to detect some bugs. In particular, a bug that was related to the CY bit management would have been difficult to find with other techniques. Furthermore we have also found a new bug in the Keilh 8051 assembler tool, although this tool being used by many users.

3.2.2 Peripheral validation

After the micro sequencer validation, the peripheral validation was the second step to verify that the macrocell is fully compatible with the 8032.

The peripherals to be tested were the followings:

- ?? the 3 timers;
- ?? the UART;
- ?? the interrupt controller;
- ?? the IO ports.

For this validation a more traditional approach was followed. The 8032 Philips Data Sheet has served as a functional specification of the product and some tests programs have been defined covering all the functions described in the data sheet.

These tests enabled to detect that in some modes the timers and the serial lines do not work properly and that the possibility to generate software interrupts was implemented which lead to some macrocell modifications.

3.3

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Recommendations

There are many questions to answer when selecting an IP core. Independently of the cost issue, it is important to address the following issues:

- ?? Concerning model issues: Is the code readable, commented and documented? Is the model easily configurable in terms of bus size, clock speed etc.? Is the model fully synchronous? Is it possible to fully reset the model? What is the fault coverage of the production test vectors?
- ?? Concerning credibility: Has the IP core been implemented in an ASIC? Is there already any commercial device using the IP core? Are there any existing customers with whom you can talk to?
- ?? Concerning extra services: What is included in the support? Do you have direct access to a support engineer? Is it possible to have training? What is the bug fixing policy? Does this policy include the notification to all users of all bugs reported?
- ?? Concerning verification: How has the model been verified? Is there a test plan and a test suite delivered with the IP core? Was the test suite defined by the IP provider or a device manufacturer or in a standard? Can I easily reproduce the test in my environment?
- ?? Licensing conditions shall also be carefully checked. Is there restrictions in using the core? Right for FPGA prototyping included? Commitments asked from licensee? NDA handling for source code?

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4 MICROCONTROLLER DEVELOPMENT PHASE

In the development phase, new functions have been added around the macrocell. As far as possible these functions have been added without macrocell modifications. However, one modification was necessary to extend the interrupt controller capabilities to support 13 interrupt sources instead of 6. For safety reasons, the modification has been verified by R.WATTS and regression tests have been performed on the macrocell.

Before implementing the new functions, all macrocell interface signals have been verified by simulation against the R. WATTS data sheet description. This allowed detecting a non-compliance, which had some impact on our design.

The understanding of the product was quite easy but required some knowledge about the 8051 device. The VHDL structure was well documented and the VHDL was easily readable even if it was poorly commented. However, we did not take the risk to perform ourselves the modifications on the macrocell. R. WATTS has performed all modifications, except one, which has been performed by ADV but has been verified by R.WATTS.

The IP provider support was not as efficient as expected due to staff changes in the design team. As a result, the macrocell procured in November 1997 could only be completely validated in July 1998 due to several iteration. The expected benefits in the development time by using an IP have been lost due to these problems in the IP provider company.

However, the development effort reduction is quite significant and can be estimated between 9 and 12 man months.

The rest of the development is similar to an ASIC development and will not be addressed in this document.

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5 BREADBOARDING

In the last phase, a microcontroller breadboard was developed as well as an application which demonstrate the major added functions.

The first problem to solve was that the design did not fit in one ACTEL FPGA, which was the goal. All of the ADV80S32 features could not be implemented and we chose not to implement the power-down functions which are technology dependant, to implement only one extra USART and only the 128 lower bytes of the additional on-chip memory which is sufficient to validate the microcontroller design.

The resulting design has been broken down in two blocks, which have been implemented in two FPGAs. The first FPGA contains the microcontroller core and the extra USART, while the second FPGA contains all the peripherals and the memory. The two FPGAs have been validated by simulation, first separately then together, before being placed and routed and mounted onto a breadboard with memories and an event generator unit.

The maximum functioning frequency of the two FPGAs is around 4 MHz, which is below what, was expected considering the macrocell documentation. However this difference is mainly due to the use of ACTEL 1280-A which are not very performant in terms of speed, and is not due to the design itself.

The breadboarded application simulates a particle counter equipment which is commanded and controlled by means of CCSDS packets transiting on an RS232 serial line. It is made of:

- ?? the two FPGAs breadboarding the ADV80S32 microcontroller;
- ?? one FPGA implementing a pseudo-random event generator;
- ?? a 16 Kbytes ROM device which contain the bootstrap program;
- ?? a 128 Kbytes RAM device to store both application program and data;
- ?? two RS232 line transceivers and two DB-9 connectors;
- ?? a 64-pin connector which provides the microcontroller input/output ports.

After reset the microcontroller executes the program from the ROM and wait for the reception of the application program on the first RS232 line. The program is downloaded into the RAM and at the end of the reception it is executed by the microcontroller from this memory.

The bootstrap program is an adaptation of a freeware assembler program developed by Philips and which has been found on the Internet. Its counterpart on the PC has been developed by ADV and can be used with any program described in the INTEL HEX format.

The application program is a permanent loop which:

- ?? waits for the reception of a CCSDS packet on the second RS232 line;
- ?? verifies and disassembles the packet to extract the TC command;
- ?? executes the TC command (counters resetting, counting start and stop, report generation);
- ?? assembles for the response a TM CCSDS packet and sends it on the second RS232 line.

The application program has been developed in C and uses some of the specific features of the ADV80S32 devices as the CRC calculator, the extra USART and its associated interruption, the external memory management and the event counting interface. It has been compiled and linked with the Keilh software development tools without difficulties proving the compatibility of the device with standard development tools.

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The breadboard has been used to test some more important sequences, which complement the simulations. It has enabled to detect an interface problem between the macrocell and the memory management logic, which was resulting in spurious write accesses to the additional on-chip memory.

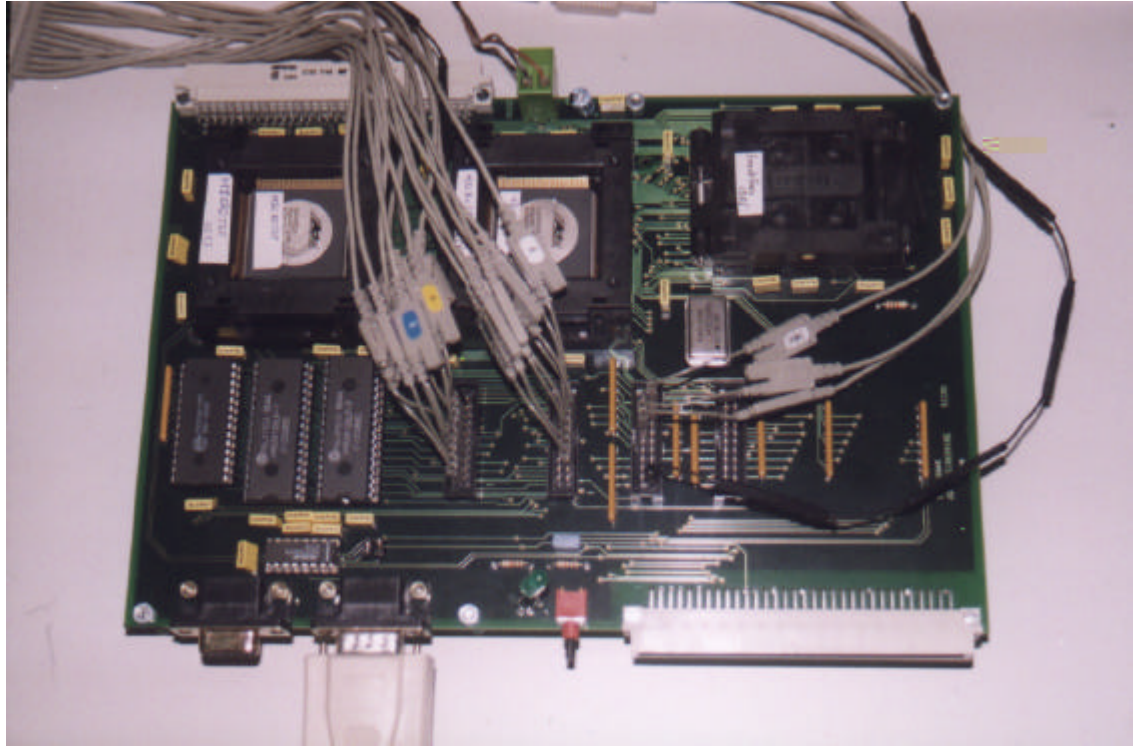


Figure 5-1 : Microcontroller breadboard

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6 INDUSTRIALIZATION

The industrialization has been performed under a continuation of the initial contract. It has consisted in the following phases :

- ?? Data sheet review,
- ?? Design update,
- ?? Detailed Design,
- ?? Layout,
- ?? Prototype manufacturing.

6.1 Data Sheet review

At the beginning of this phase, the Data Sheet has been distributed to potential users including MMS, Alcatel Space Industries, Laben, Saab Ericsson Space, DASA, CRISA, Contraves and university of Surrey. We have received a few comments from MMS-UK and Alcatel Space in order to add one more USARTs and to add wait states insertion capabilities during memory accesses. In addition we have not found a strong interest in the event counter capability that was provided by the chip. Finally the general feedback for this device was quite good that is interesting for the future.

The review of the data sheet by the industrial has been continued with ESTEC in order to finalize the chip functionality. As a result it has been decided to :

- ?? Remove event counters feature,
- ?? Remove power-down mode for the USARTs and CRC calculation,
- ?? modify the EDAC function to detect and correct byte single/double error instead of detect and correct single error on a quartet basis,
- ?? add an additional Extra Usart and its interrupt,
- ?? add one additional external interrupt,
- ?? extend external memory access capabilities up to 8 Mbytes for code and 16 Mbytes for data by page of 32 Kbytes for the code and 64 Kbytes for the data,
- ?? add two 64-bytes Fifo, to be used with the extra Usarts and that can be used as reception or transmission buffer,
- ?? add an on chip bootstrap program that enable to download a program into an external RAM via PacketWire transfers.

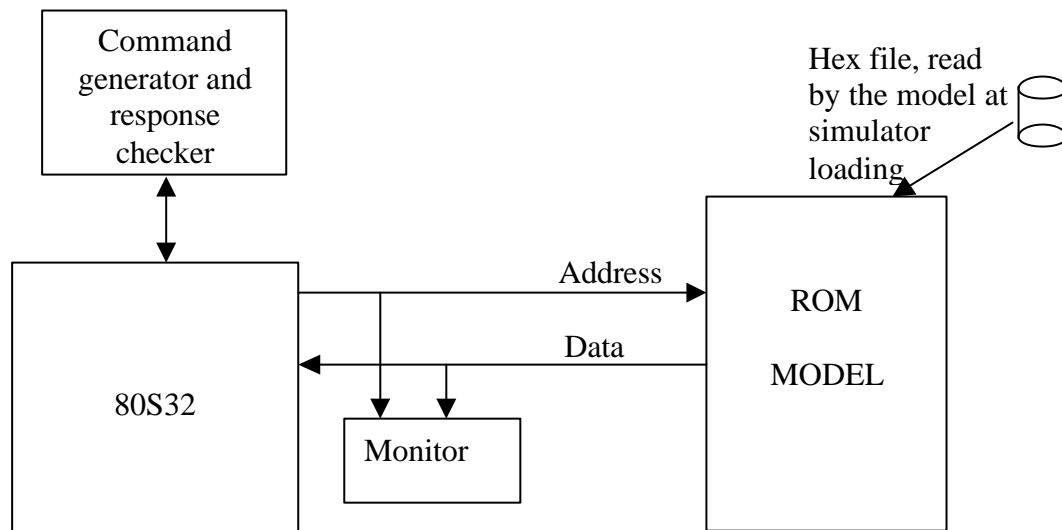
All design modifications have then been performed and regression tests have been performed. An important work has consisted in defining, developing and testing the on-chip boot program.

6.2 On chip boot program

The bootstrap program shall receive telecommand packets from one USART, process the packet and send its response also via an USART. It has been agreed, that transmission on the serial interfaces will be performed by using the PacketWire protocol and that the packet structure shall be CCSDS compliant.

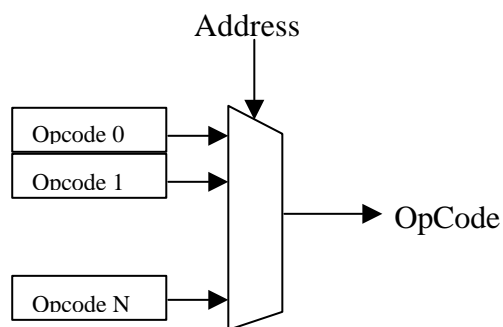
The defined bootstrap program has been coded in assembler, transformed in hex format and verified in simulation.

Verification of the program has been performed in two steps. In a first step, the program has been implemented into a VHDL ROM model connected to the microcontroller VHDL model. A monitor block is inserted on the busses between the ROM and the microcontroller. This block disassembles the program that is executed to give some visibility on the program execution. A command generator and response checker is used to send the command and to verify the response.



In a second phase, the program has been integrated into the 80S32.

The bootstrap program is defined as an 8-bit values array that contain all the bootstrap program op-codes. This array is defined as a constant and a combinatorial function performs the selection of the opcode in use, depending on the internal address bus value, and provides it onto its data bus.



After integration, regression tests have been performed on the model and no differences have been detected.

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6.3 Memories implementation

The chip embeds two 128*16 bits single RAM memory and two 64*8 bits FIFO. The single RAM is a macro block that was provided by ATMEL and that has been integrated in the design during layout. For the FIFOs, we have preferred to develop our own block because the macro blocks proposed by ATMEL has a known bug if a certain access configuration occur.

Test in production of the memory blocks is performed by a program that is executed by the microcontroller. This program implements the Marinescu II algorithm that is the one recommended by ATMEL. In order to limit the amount of vectors needed to test the memory, the program has been embedded into the device and is executed after reset when the test memory configuration is selected with the device configuration pins.

6.4 Detailed design

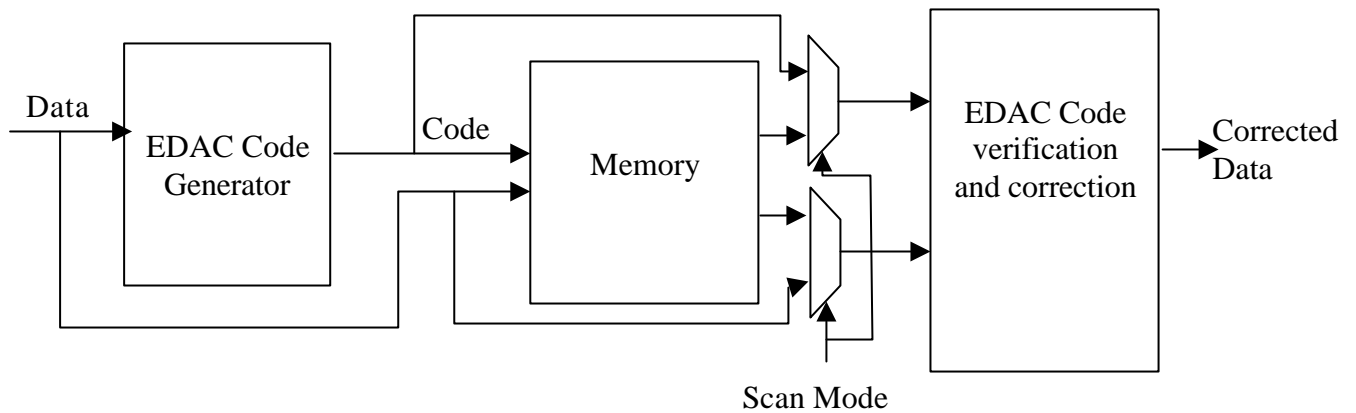
In order to facilitate the synthesis of the chip, the design has been modified in order to use only one clock instead of two in the previous design. However the design uses the two clock edges and the main constraints come from this.

Our target was to run the device at 20 MHz e.g. with a period of 50 ns. As the device uses the 2 clock edge we need at least to accept a duty cycle of 40/60 on the clock. This mean the distance between the two clock edges can be comprised between 22 and 58 ns. So to achieve the 20 MHz speed we have performed a synthesis by defining a clock with a duty cycle of 50% and a period of 40 ns that is a bit more that we need but give margin for routing.

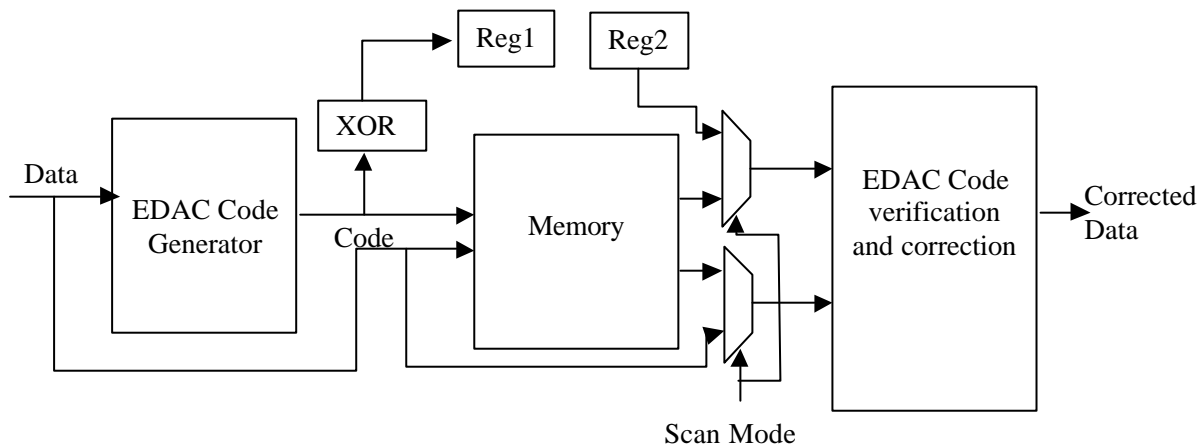
Flip-flop hardening should also be performed during synthesis. The signals that have been hardened are all signals relative to the instruction fetching and execution (program counter, instruction storing registers, ...) and all configuration registers (memory bank, UART configuration, ...)

Hardening was performed block by block by replacing selected flip-flops with their hardened version in the ATMEL library. However, during the merge process of the different blocks the synthesizer has performed an optimization that has resulted in removing all the hardened Flip-Flops that where inserted in the previous step. This has been discovered only at the Design Review and has needed to perform an additional routing to reinsert hardened flip-flops in the design.

The testability of the device was achieved by using a program for RAM testing (cf. 6.3) and with a full-scan technique for the logic itself. After a first vector generation try, we have detected a problem for the test of the EDAC. Problem comes that in Scan mode, the memory are bypassed and then the EDAC code generator block is directly connected to the EDAC code verification and correction block. In this case a stuck at fault in the EDAC code generator is always corrected by the EDAC code verification and correction block and cannot be detected



We are then obliged to modify the architecture in scan mode to have a better fault coverage. In scan mode, the 8 bits of the EDAC code generator output are xored and the result is stored into an internal register and the 8-bit code input of the EDAC Code verification and correction blocks is connected to an internal register.



6.5 Layout

The layout activity has been performed by ATMEL. Three layouts were necessary before to obtain the final netlist.

The first iteration comes from the need to harden some of the flip-flops of the design (cf. 6.4). The flip-flop replacement had degraded the device performances such that we were at a limit to operate the device at 20 MHz.

A second iteration has then been performed by reordering the scan chain according to the flip-flops placement. The routing enable to gain around 2 ns that is enough to operate the device at the speed we target.

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6.6 Product distribution

The ADV80S32 will be made available for all European Space Industries at a fair and reasonable price.

For this ATMEL-WM and ADV Engineering have elaborated during this project an agreement for the product. The ADV 80S32 distribution will be performed by ATMEL-WM while the technical support will be provided by ADV.

In addition the Data Sheet has been transferred from ADV to ATMEL-WM in order to be aligned with the ATMEL format.

However, before to be supported as a standard ASIC, the prototypes shall first be functionally tested. The test activity is not covered by this contract and is mandatory to establish the device as a standard ASIC.

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7. CONCLUSION

Due to the increasing complexity of ASICs, the use of IP blocks in ASIC designs will become more and more frequent. Today there are a lot of company proposing VHDL blocks that they have developed for a particular application and which they want to commercialise. However, some precautions have to be taken in order to verify the macrocell behaviour and interfaces. It is of importance to define a macrocell validation plan and either to perform the tests that you have defined or to verify that the macrocell provider has performed these tests. The cost of this validation phase can be as large as the cost of the macrocell itself and cannot be neglected in the development cost. In addition, in case of bug detection, some iteration with the macrocell provider can be necessary to correct the macrocell, which can impact the project schedule. Once the macrocell is validated, the development phase is not very different from other ASIC developments.

However, it has to be noted that the testability has generally to be included with scan insertion techniques (scan flip-flop insertion in the netlist + ATPG) since fault coverage vectors are generally not provided with the macrocell and that it is difficult to self define tests vectors which will ensure 95% fault coverage

The results of this activity can be used in several ways:

- ?? the **8032 core** and the several peripherals developed within the activity are available to European space industry for their own ASIC developments,
- ?? the availability of the microcontroller as a **STANDARD ASIC** in a rad-tolerant technology, will solve the problem for those applications which require limited processing capabilities at reasonable cost, and will give access to space-dedicated microcontroller to small companies that do not have ASIC development capabilities.

There are several space specific application types where the 8032 core can be used:

- ?? telecommunication and constellations:
 - ?? antenna pointing controllers
 - ?? synchronisation loop and base band processing in transponders
 - ?? Mil-Std-1553 bus couplers
 - ?? general housekeeping and other low level tasks
- ?? manned space applications such as glove boxes etc.
- ?? science instruments such as:
 - ?? new particle detector systems
 - ?? replacement of commercial and obsolete devices in various equipment
 - ?? next generation radiation environment monitors
- ?? main processor on small satellites (e.g. student developments)

The **first prototypes** of the ADV80S32 have been successfully manufactured by ATMEL and the device will be included into the **ATMEL brochure** in the following weeks.

For the near future we are testing a **Mil-Std-1553 intelligent bus coupler**, which includes the 8032 core. This coupler is currently implemented into a XILINX technology and should be ported in the ATMEL-WM technology next year.

ANNEX: ADV80S32 standard ASIC presentation.

The 80S32 is a high performance microcontroller. It is fully compatible with the well-known 80C32/80C52 device and the technology combines high execution speed with high level of integration. Some features have been added to the 80C32 device and the performance has been increased by a factor of 3 that means a processing power of about 2.3 MIPS at 15 MHz. This device is powerful enough to handle the requirements of embedded on board applications.

Specific Features

- ?? 512 bytes on-chip memory ;
- ?? Full 64 Kbytes addressing range for program and data, with expansion up to 16 Mbytes for data and 8 Mbytes for program;
- ?? De-multiplexed Address/Data bus ;
- ?? Memory protection for both internal and external memory;
- ?? Program downloading and program execution from RAM capabilities;
- ?? Fives serial interfaces:
 - * One RS232 UART;
 - * Four extra configurable USARTs (RS232, PacketWire and TTC-B-01 compatible);
 - * two 64 bytes FIFO that can be associated to one of the extra USART and used as emission or reception buffer;
- ?? Three 16-bit counters/timers with extended time count duration;
- ?? Five external interrupts with two priority levels;
- ?? A CRC calculation acceleration unit compatible with CCSDS TM and TC packets;
- ?? Latch-up immune. Total dose > 50Krad. SEU > 20Mev.

