Functional and Performance Validation of the 80S32 µC

Executive Summary

Deliverable D5.2 - Report

Workpackage 5 – Evaluation Kit

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1 Introduction

The aim of this activity has been to validate functionally and performance wise the engineering devices of the ADV80S32 µC. This 8-bit µC has been developed under an ESA contract by ADV engineering. This component is based on a commercial 3rd party IP core, originally from Richard Watts Associates, later commercialized and maintained by Dolphin Integration.

The IP has been enhanced by extended timers, additional USART interfaces, interrupt inputs, de-multiplexed address/data bus and extended addressing range. In addition it is equipped with space specific features, memory SEU protection for internal and external memories and a hardware CRC calculation engine compliant to CCSDS TM/TC standard. The device has been fabricated in Temic/Atmel 0.5 µm radiation tolerant gate array technology (MG2RT).

In order to allow the establishment of the 80S32 as standard space component (ASSP), an evaluation board and a suitable test-suite have been developed.

The test-suite comprises of functional and performance tests. Additionally, tests under varying operating conditions (supply voltage) as well as SEU testing at ESTEC Californium (Cf-252) facilities have been performed.

1.1 Reference Documents

RD-1 ADV80S32 Datasheet v2.5, ADV Engineering, 22-05-2001

RD-2 “80S32 Validation Plan”, D2.3/ISD/80S32 v1.2, ISD S.A., 09-02-2009

RD-3 “Validation Board Specification”, D2.2/ISD/80S32 v1.0, ISD S.A., 30-06-2008

RD-4 “80S32 Validation Board User Manual”, v1.0, ISD S.A., 24-02-2009.

RD-5 “80S32 Validation Report”, D4.1/ISD/80S32 v1.2, ISD S.A., 29-04-2009

RD-6 “SEU Radiation Test Report:”, v1.3, ISD S.A., 29-04-2009

RD-7 “Datasheet Update/Errata Sheet”, ERRATA/ISD/80S32 v1.0, ISD S.A., 29-04-2009

1.2 Glossary

CCSDS	Consultative Committee for Space Data System
CRC	Cyclic Redundancy Code
DUT	Device Under Test
EDAC	Error Detection And Correction
FPGA	Field Programmable Gate Array
I/O	Input/Output
SEU	Single Event Upset
TC	Telecommand
TM	Telemetry
USART	Universal Synchronous Asynchronous Receiver Transmitter

2 Validation Board

The 80S32 validation board is a versatile and user friendly development platform, enabling performance testing and validation of the 80S32 µC and was developed to meet the particular needs of the project.

Users may evaluate the 80S32 performance and features under various test conditions of operating voltage, temperature and operating frequency. Jumpers and test points provide additional flexibility in the evaluation and development process. Specific HW based on FPGA design has been implemented to support the system, which is fully described in the corresponding Digital Design Specification documentation [RD-3]. Additionally, a comprehensive guide of how the whole system works, is included in the system's user manual [RD-4.

The system consists of two distinct boards, a motherboard and a daughterboard [Figure 1]. Motherboard contains a programmable logic device (FPGA) with adequate number of I/O pins interfacing all functional pins of both the µC and its peripherals. The FPGA serves as a traffic handler between the µC and its peripherals for supervision purposes. In some cases (tests) it also interacts and/or provides stimuli to the µC.

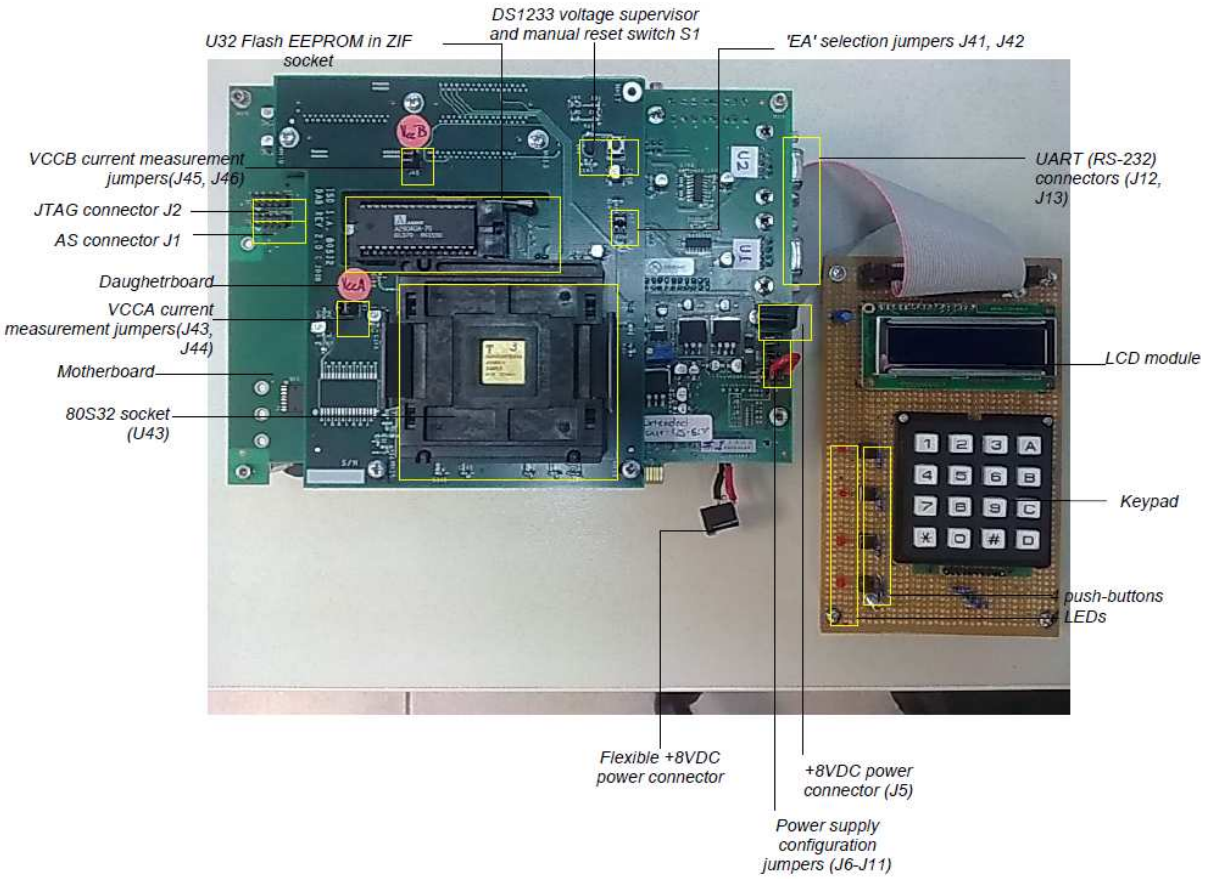

Figure 1 - 80S32 validation board with remote keypad unit.

3 Validation Results

Detailed validation results are contained in RD-5 and RD-6, a summary is given on the following pages. The errors detected have been documented in the Errata Sheet RD-7.

3.1 Functional & Performance tests

Functional tests focus on verifying backward compatibility with the standard Intel 8032 core as well as correct operation of the additional features such as the CRC engine, extended internal memory, external memory, interrupt management, timers and serial interfaces.

Performance tests cover both distinct typical tasks involving matrix arithmetic, signal processing and sorting/searching algorithms among others as well as Dhrystone and Whetstone synthetic workloads.

Table 1 shows the results categorized in terms of tested components or features.

Category	Passed	Problematic	Failed
Internal Memory	4	1	-
External Memory	1	-	-
Timers/Counters	17	-	-
Serial Ports	8	-	-
Interrupt Controller	-	1	-
CRC Accelerator	1	-	-
Boot PROM	-	-	1
Instruction Set	28	-	-
Performance	24	-	-
Overall	96.51%	2.33%	1.16%

Table 1 - Validation results

3.2 Power Measurements

The objective of performing power measurements is to characterize the 80S32 uC in terms of power consumption, under specific activity and operating conditions. The power measurement include the characterization of the part along a two-dimensional voltage and clock frequency range, by simultaneous monitoring of case temperature.

Table 2 below show the evaluated min-max power consumption figures at the maximum clock frequency of 22MHz and through the specified voltage supply range (4.5V – 5.5V), when the uC is running a special test routine (running state).

f_{clk}(max) = 22MHz	
Vs (V)	P (mW)
4.5 (min)	266
5.0 (typ.)	339.2
5.5 (max)	427

Table 2 - Power consumption at f_{clk}(max) = 22MHz

Figure 2 shows the family of power consumption curves at spot clock frequencies and for various supply voltages.

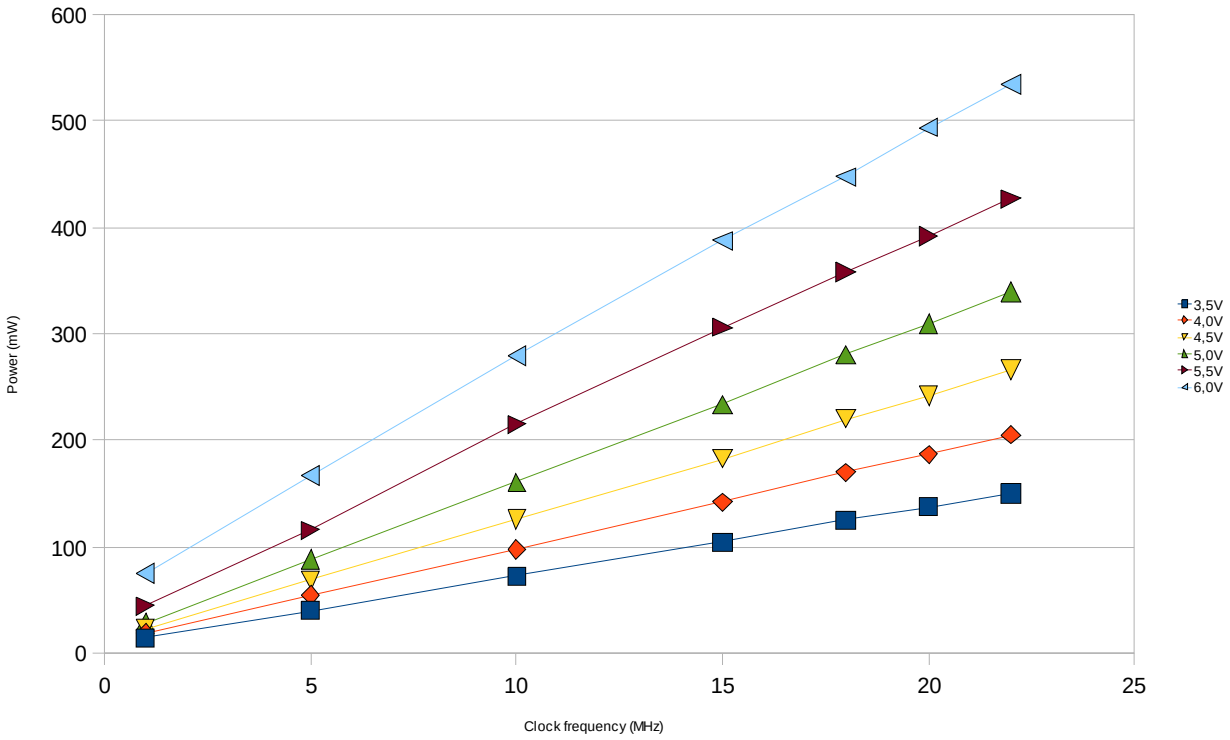

Figure 2 - Power consumption curves for various supply voltages (running state)

3.3 Bugs & Problems

- Difficulty to run compiled C code in EDAC mode.
- Parallel port P0 cannot be configured for general purpose I/O.
- Interrupts IE2, IE3 & IE4 once triggered by software, they cannot be cleared.
- USART Interrupts are raised prematurely.
- Default values (power-up or reset) of some registers are different from those described in the datasheet [RD-1].
- A number of output pins are defined in RD-1 as floating, though they should be connected directly to VSS.
- Reset pin is defined in RD-1 as active low, whereas it should be active high.

4 Radiation Results

The µC was tested for SEU sensitivity to radiation effects at the CASE Cf-252 facility at ESA-ESTEC, The Netherlands. During the three-day testing period, a number of recoverable errors were detected at the internal memory of the device. The tests were conducted under vacuum conditions inside a suitable bell-jar chamber [Figure 3].

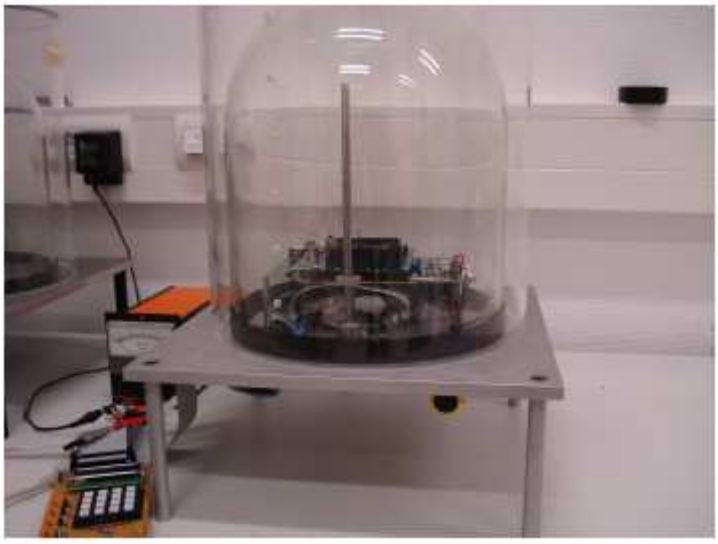

Figure 3- Validation board inside the vacuum bell-jar.

In both test runs, only correctable memory errors have been detected [Table 3]. In general, the cross-section measured during these tests is 1-2 orders of magnitude better (i.e. lower) than figures reported by Atmel for the MG2RT technology which were obtained at a particle accelerator. There are several uncertainty factors which may explain this relatively large discrepancy, namely the uncertainty on the activity of the Californium radiation source, general differences between the radiation profiles from Californium and from the accelerator, and differences in the test vehicle and test conditions.

Metrics	1st RUN	2nd RUN
Total duration (t)	12h	19h 31m
Corrected RAM errors (e)	7	42
Uncorrected RAM errors	0	0
Possible flip-flop SEU events	1	1
Upset rate er (upsets/ sec)	1.62×10^{-4}	5.98×10^{-4}
Test cross-section X (cm^2)	3.90×10^{-6}	1.43×10^{-5}
Cross-section per bit Xb (cm^2/bit)	4.31×10^{-9}	9.40×10^{-9}

Table 3 - Radiation test results

A future version of the test software should strive to maximize the SW cross-section by exercising as many SEU sensitive bits as possible.

To improve the robustness of the test strategy, all error counting and logging should be performed outside the DUT. Additionally, a watchdog could be implemented, allowing automatic reboot of the DUT.

Given the amount of time it is required for the vacuum in the radiation chamber to reach the appropriate level, it would have been more practical if the test software could be changed without opening the chamber.

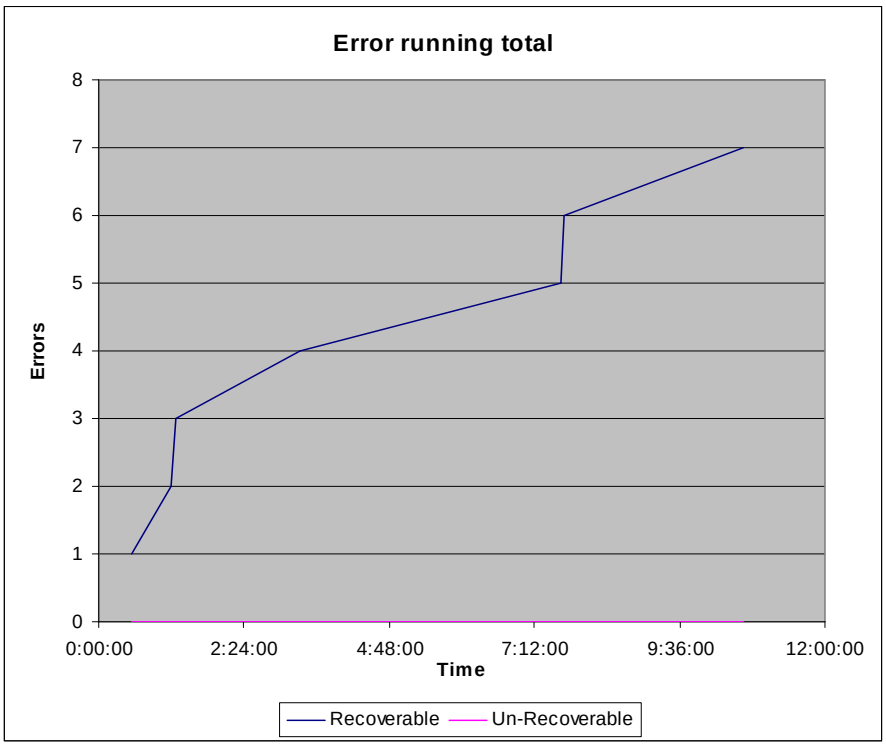

Figure 4 – Errors Running Total for first test

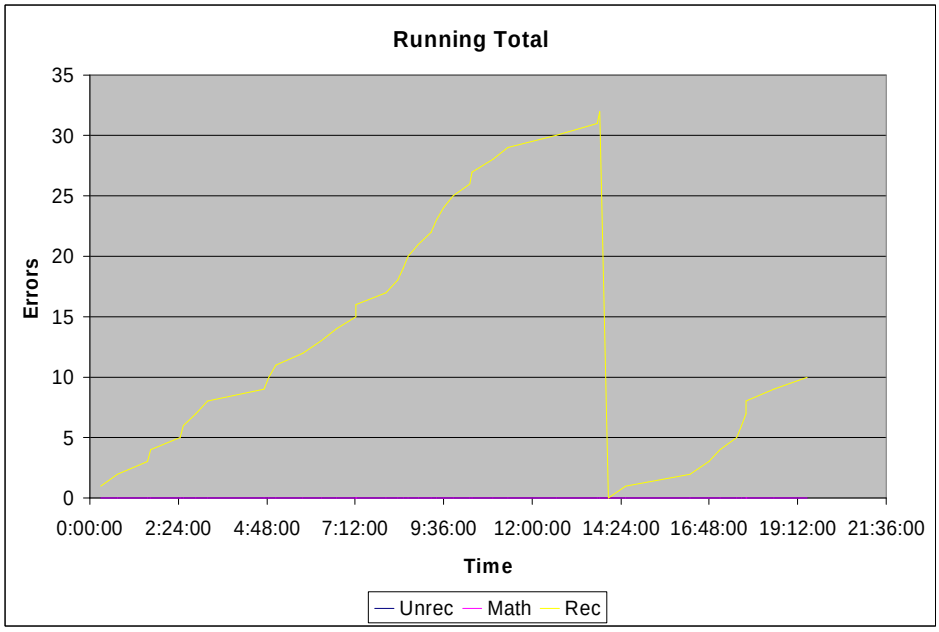

Figure 5 –Detected errors running total for the second test

5 Conclusions

A flexible validation and evaluation board has been designed for the 80S32 microcontroller. The 80S32 has been validated in terms of functionality, performance, power consumption

and single event radiation tolerance. The flexible concept chosen for the validation platform enables the re-use of the validation board design also for other devices.

Functional Validation

- Most parts of the 80S32 have been found to work properly.
- A few mistakes to the pin description have been found requiring an update to the datasheet.
- A few functional problems have been found requiring description in an errata section of the data sheet and definition of possible workarounds.
- The most serious issue is the impossibility to generate valid executables featuring EDAC support when complied from C-sources. This requires further investigation and definition of workaround, possibly a patch to the compilation tools to be defined in cooperation with the tool vendor.

Performance Validation

The performance tests have shown that the 80S32 operates at a clock frequency of up to 22MHz, measured at a maximum case temperature of 41,5 ℃ degrees in the range of [4.5V to 5.5V] supply voltage. This is in-line with the specified value of 20 MHz.

Power Consumption

As expected for a given supply voltage Vs, consumed power exhibits a linear relation to the operation frequency both in idle and running state. Likewise, for a given operating frequency, consumed power µC exhibits a slightly sub linear relation to the power supply voltage. This is attributed to the leakage current dependence on the bias voltage. The maximum power consumption (5.5V) at 10MHz was measured 215mW. This result is comparable with the theoretical value of 235mW reported during the design phase, for the same clock frequency.

The power consumption at 5.0 V supply voltage is about 16 mW/MHz.

Radiation Tolerance

Given the test conditions (vacuum, radiation source) and DUT technology (0.5µm), the number and type of detected errors were considered both logical and expected.

The two interrupts on software's normal execution (crashes on both test runs) may be assumed to be SEU events in flip-flops due to irradiation, as only a subset of the flip-flops is SEU hardened.

In summary, SEU error rates stay far below the SEU cross-sections provided by Atmel for the MG2RT technology, and the 80S32 microcontroller has been shown to have very good radiation tolerance.