A System-on-a-Chip for Small Satellite Data Processing and Control ("ChipSat")

Abstract

This document summarises the work carried out within the ESA funded activity *"ChipSat: A System-on-a-Chip for Small Satellite Data Processing and Control"* at the Surrey Space Centre in Guildford, UK.

All of the objectives of the contract were fully met as follows:

- A Requirement Specification for a single chip data processing and control system targeting small satellites was derived.
- The feasibility of a software implementation of a CCSDS based telemetry and telecommand on-board communication system was assessed.
- Potential usage of highly reliable parts, developed under ESA funding, for small and medium size, low cost satellite missions was evaluated.
- A single chip data processing and control system for a small satellite was designed, implemented on a high-density FPGA and verified.
- Usage of ESA developed VHDL cores in FPGA developments was evaluated.

SoC Specification and Feasibility Experiment

The system-on-a-chip (SoC) for small satellite data processing and control, codenamed "ChipSat", aims to implement an on-board data handling (OBDH) system of a small satellite with enhanced remote sensing and data gathering capabilities on a single mixed-mode application specific integrated circuit (ASIC) chip. The specification of the system-on-a-chip is based on requirements derived for future satellite missions of Surrey Satellite Technology Ltd. (SSTL), who have designed and manufactured micro- and mini- satellites for more than 20 years. The SoC consists of four subsystems – a 32-bit RISC processor core modified for space use; an image handling subsystem capable of capturing and compressing still or video-rate images; a communication subsystem for the satellite uplink and downlink connection; and a supporting peripheral subsystem.

A single chip solution of an entire OBDH system in the form of a mixed-mode ASIC is well beyond the funding of the contract. Financially viable option in the circumstances are high-density field-programmable gate arrays (FPGAs). FPGAs offer a number of advantages that are very relevant to the specifics of small satellite design: flexibility of design, shorter time-to-market, lower cost, remote reconfigurability, etc. So far high-density FPGAs have mostly been used in payload systems of small satellites, however introduction of radiation hardened versions of such devices by leading manufacturers as XILINX and Actel paves the way for their use in main on-board electronic systems.

A feasibility study into the implementation of an on-board computer (OBC) on a single programmable chip was carried out. The aim was to scale down an existing OBC, implemented as a printed circuit board (PCB), to a SoC implemented on a high-density XILINX Virtex FPGA. A primary OBC, developed by SSTL and flown on several small satellite missions, was used as a reference design. Figure 1 shows the block-diagram of the system-on-a-chip OBC (SoC-OBC). Two of the modules - the LEON microprocessor core and the HurriCANe CAN core - are developed by the European Space Agency (ESA). The LEON processor core includes support for

the Advanced Microcontroller Bus Architecture (AMBA) protocol, and therefore the AMBA bus is selected as an on-chip bus of the SoC.

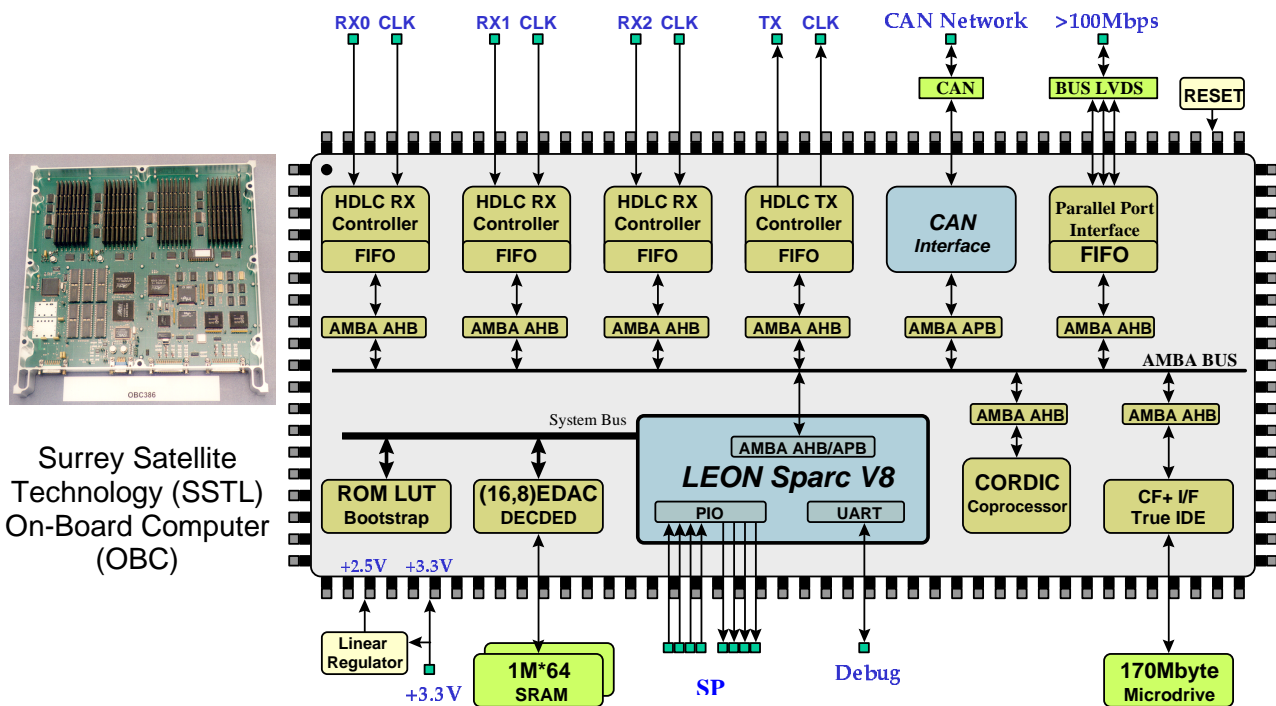Surrey Satellite Technology (SSTL) On-Board Computer (OBC)

Figure 1. System Block-Diagram of the SoC-OBC

The SoC-OBC feasibility study has shown that it is possible to implement the functionality of a small satellite OBC on a single programmable logic chip. The design work during the feasibility experiment was supported by a purpose-built prototyping board.

Implementation of a Downsized SoC Prototype

A downsized version of the SoC-OBC was implemented on a XILINX Virtex XCV800 FPGA (HQ240, speed –4) using the prototyping board XSV-800 from the XESS Corporation. The downsized system represents a main subsystem of the SoC-OBC and consists of the LEON processor core, the HurriCANe core and an EDAC core. The EDAC IP core used in this study is developed by SSTL. The prototyping board is connected to a personal computer (PC) via a serial and a parallel interface. The parallel connection is used for downloading of the SoC-OBC design, while the serial connection is used for downloading of application programs. Communication with the Leon processor is achieved via its standard I/O device UART A. Figure 2 illustrates the experimental set-up for the implementation and testing of the SoC-OBC.

The HurriCANe core is integrated with the LEON processor core through the AMBA Advanced Peripheral Bus (APB). An external CAN controller card is employed in addition to the prototyping board to test the CAN core. The CAN IP core and the external CAN card act as two equivalent nodes on the CAN bus. The CAN card communicates with the PC through the serial port and is controlled by the software package CAN-PCS developed by SSTL.

The CAD software tools used were: VHDL simulator ModelSim, synthesis tool Synplify 6.0+, Place & Route tools in the XILINX Foundation package, versions 2.1i and 3.1i.
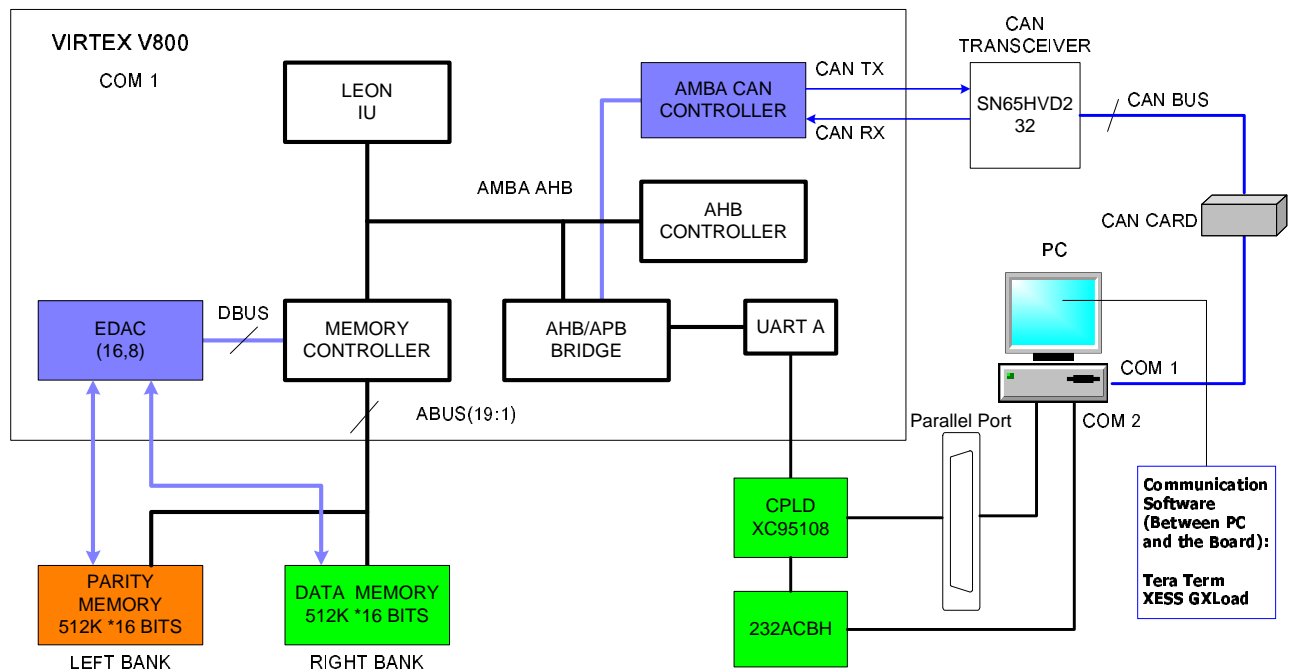
Figure 2. Implementation and Test of the LEON processor with the CAN and EDAC IP Cores

Three versions of the LEON processor IP core (1-2.2.2, 1-2.4.0 and 2-1.02a) were implemented and verified at 25 MHz on the XESS prototyping board. The implemented downsized SoC-OBC (LEON processor + CAN + EDAC) requires about 50% of the capacity of the target FPGA - Virtex XCV800. The bitstream file of the downsized system measures 576 Kbytes. Estimates of the area of the SoC-OBC, excluding the CORDIC co-processor, indicate that it fits in about three quarters of the XCV800 chip. However the entire OBC system, including the CORDIC co-processor, requires a larger chip. For example, Virtex XCV2000E will be able to house the whole system.

Development of a Software CCSDS Communication System

The developed software communication system is based on the Consultative Committee of Space Data Systems (CCSDS) protocol and satisfies the needs of a single-chip on-board computer. The system transmits telecommand (TC) and telemetry (TLM) data to/from a small satellite where the SoC-OBC acts as the on-board computer (Figure 3).

The complete implementation of the CCSDS TC & TLM protocol is very complex and hardware implementations are expensive for low-cost small satellites. Therefore the developed CCSDS software package focuses on a subset of functions such that it represents a simplified yet reliable standalone alternative software implementation of the CCSDS TC & TLM Command Operation Protocol (COP-1).

The CCSDS software package features a modular structure, which can facilitate easy expansions of functionality to suit specific mission requirements. The size of the CCSDS software is as follows: ground segment including the Reed-Solomon (R-S) decoder - 177 Kbytes; spacecraft segment including the R-S encoder - 176 Kbytes; R-S encoder/decoder - 21.7Kbytes. The software imposes minimal memory footprint and performance requirements on the OBC.
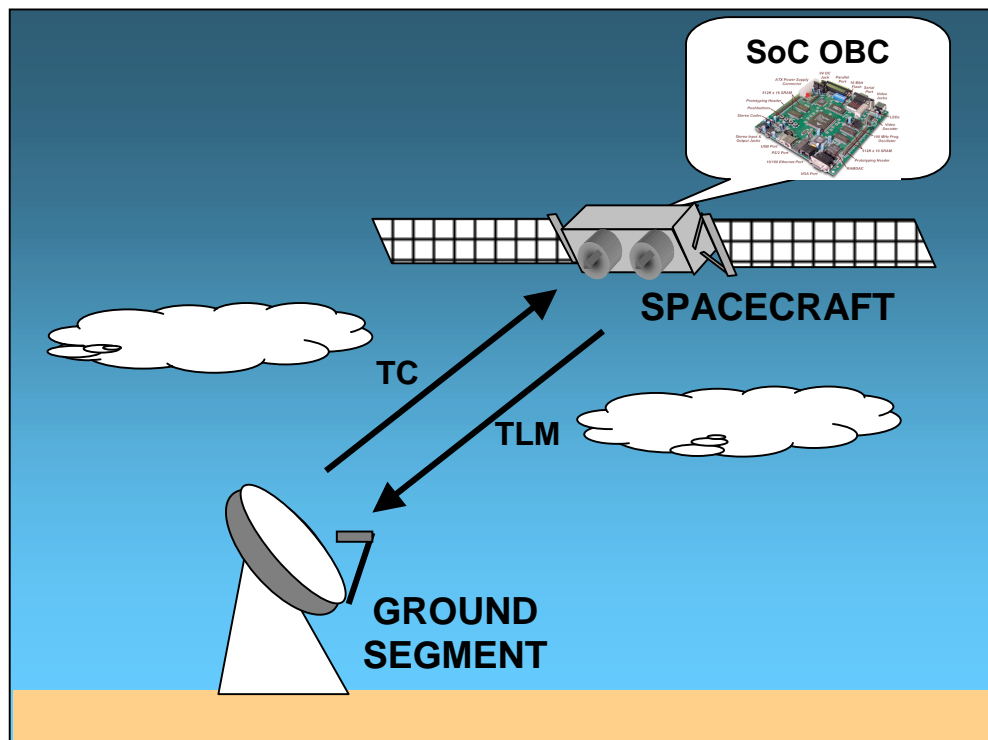
Figure 3. TC & TLM Communication System of a Small Satellite

System Verification with Software TLM/TC Loop

The main functionality of the CCSDS package and its operation on the implemented SoC-OBC were verified by simulation. The on-board segment software was executed by the SoC-OBC implementation on the XESS prototyping board; the ground station segment software ran on a personal computer. Communication between the on-board segment and the ground segment was carried out via a serial link. The CAN bus system (consisting of two nodes – the HurriCANe IP core and the CAN controller card) was used to verify the validity of the whole system. The CAN card emulated the responsibilities of an on-board payload which received TC data and generated TLM data. Figure 4 shows the simulation data-flow.

Simulation scenarios covering the entire communication data-flow cycle were tested – sending of TC data to the spacecraft, on-board processing of TC data, generation and sending of TLM data to ground. Verification results demonstrate that the software TC/TLM loop operates correctly. This simulation experiment confirms that a CCSDS based telemetry and telecommand on-board communication system could be developed using mainly software.

The combination of a single chip OBC and a software CCSDS-based communication system supported by a thin-layer hardware interface can provide a cost effective and flexible communication solution for small satellites.

We view this work as an important step facilitating further research on miniaturization of the small satellite platform and would like to acknowledge gratefully the financial support provided by ESA.
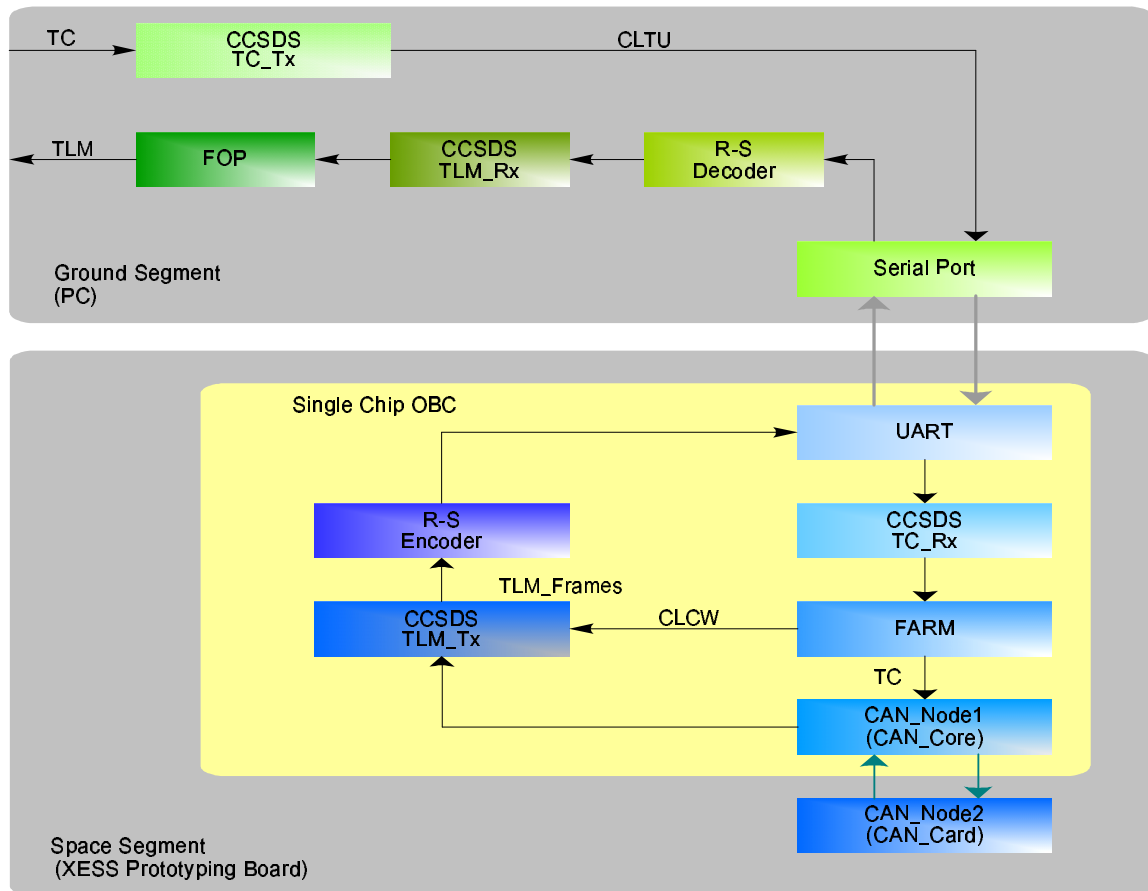
Figure 4. Simulation Data Flow of the CCSDS Communication System

General Experience with IP Usage

This work would not have been possible without the ESA IP cores LEON and HurriCANe. These soft VHDL IP cores are a great asset for the design community worldwide. They act as a driving force for many exciting projects. Free availability of high-quality RTL code gives a high degree of flexibility enabling application-specific modification and changes. Furthermore, due to its parameterizable nature the LEON IP core can be configured as appropriate, which allows users to select configurations that best suit their applications. The availability of design environment for the LEON processor in the public domain, which supports multiple platforms, is extremely useful. The LEON Internet user-group run by Jiri Gaisler has been an excellent source of information and help.

Our experience has shown that low-cost SoC solution can be achieved via the use of public domain IP cores and in-house core development, however the design effort in reusing existing IP cores can be very high. When reusing an existing core IP core, it pays off to look around for the right synthesis tool – the one that provides support for the particular IP core. The LEON core is a rather complex design, written at a very high behavioural level, and a colossal effort would be required if changes are to be introduced in it. LEON–based development require designers with a variety of software and hardware skills that can be difficult to recruit. HurriCANe-based designs would benefit from further software support in the form of accompanying test and API routines.