SPARC V7.0

Instruction Set

for Embedded Real time 32–bit Computer
(ERC32)
for SPACE Applications
1. Assembly Language Syntax

The notations given in this section are taken from Sun’s SPARC Assembler and are used to describe the suggested assembly language syntax for the instruction definitions given in Section 6.2.

Understanding the use of type fonts is crucial to understanding the assembly language syntax in the instruction definitions. Items in **typewriter font** are literals, to be entered exactly as they appear. Items in *italic font* are metasymbols that are to be replaced by numeric or symbolic values when actual assembly language code is written. For example, asi would be replaced by a number in the range of 0 to 255 (the value of the bits in the binary instruction), or by a symbol that has been bound to such a number.

Subscripts on metasymbols further identify the placement of the operand in the generated binary instruction. For example, regrs2 is a *reg* (i.e., register name) whose binary value will end up in the *rs2* field of the resulting instruction.

1.1. Register Names

*reg*

A *reg* is an integer unit register. It can have a value of:

- %0 through %31: all integer registers
- %g0 through %g7: global registers—same as %0 through %7
- %o0 through %o7: out registers—same as %8 through %15
- %l0 through %l7: local registers—same as %16 through %23
- %i0 through %i7: in registers—same as %24 through %31

Subscripts further identify the placement of the operand in the binary instruction as one of the following:

- **reg**<sub>rs1</sub> — *rs1* field
- **reg**<sub>rs2</sub> — *rs2* field
- **reg**<sub>rd</sub> — *rd* field

*freg*

A *freg* is a floating-point register. It can have a value from %f0 through %f31. Subscripts further identify the placement of the operand in the binary instruction as one of the following:

- **freg**<sub>rs1</sub> — *rs1* field
- **freg**<sub>rs2</sub> — *rs2* field
- **freg**<sub>rd</sub> — *rd* field

*creg*

A *creg* is a coprocessor register. It can have a value from %c0 through %c31. Subscripts further identify the placement of the operand in the binary instruction as one of the following:

- **creg**<sub>rs1</sub> — *rs1* field
- **creg**<sub>rs2</sub> — *rs2* field
- **creg**<sub>rd</sub> — *rd* field

1.2. Special Symbol Names

Certain special symbols need to be written exactly as they appear in the syntax table. These appear in **typewriter font**, and are preceded by a percent sign (%). The percent sign is part of the symbol name; it must appear as part of the literal value.
The symbol names are:

- \%psr: Processor State Register
- \%wim: Window Invalid Mask register
- \%tbr: Trap Base Register
- \%y: Y register
- \%fnsr: Floating-point State Register
- \%cnsr: Coprocessor State Register
- \%fqr: Floating-point Queue
- \%cq: Coprocessor Queue
- \%hi: Unary operator that extracts high 22 bits of its operand
- \%lo: Unary operator that extracts low 10 bits of its operand

### 1.3. Values

Some instructions use operands comprising values as follows:

- `simm13`: A signed immediate constant that fits in 13 bits
- `const22`: A constant that fits in 22 bits
- `asi`: An alternate address space identifier (0 to 255)

### 1.4. Label

A label is a sequence of characters comprised of alphabetic letters (a–z, A–Z (upper and lower case distinct)), underscore (_), dollar sign ($), period (.), and decimal digits (0–9), but which does not begin with a decimal digit.

Some instructions offer a choice of operands. These are grouped as follows:

- `reg_addr`:
  - `reg ns1`
  - `reg ns1 + reg ns2`
- `address`:
  - `reg ns1`
  - `reg ns1 + reg ns2`
  - `reg ns1 + simm13`
  - `reg ns1 - simm13`
  - `simm13`
  - `simm13 + reg ns1`
- `reg_or_imm`:
  - `reg ns2`
  - `simm13`

### 1.5. Instruction Mnemonics

Figure 1.1 illustrates the mnemonics used to describe the SPARC instruction set. Note that some combinations possible in Figure 1.1 do not correspond to valid instructions (such as store signed or floating-point convert extended to extended). Refer to the instruction summary on page 6–6 for a list of valid SPARC instructions.
### Data Transfer

**Load/Store**
- **Signed**
- **Unsigned**
- **Byte**
- **Halfword**
- **Word**
- **Double Word**
- **Register**
- **Status**
- **Register Queue**

**atomic SWAP word**

**atomic Load-Store Unsigned Byte**

### Integer Operations

<table>
<thead>
<tr>
<th>AND</th>
<th>OR</th>
<th>XOR</th>
<th>normal</th>
<th>Not</th>
<th>normal set CC</th>
<th>Shift</th>
<th>Left</th>
<th>Right</th>
<th>Logical Arithmetic</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD</td>
<td>SUB</td>
<td>normal</td>
<td>eXtended</td>
<td>normal set CC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read</td>
<td>Write</td>
<td>Y</td>
<td>PSR</td>
<td>WIM</td>
<td>TBR</td>
<td></td>
<td>Tagged</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**MUL**itp Step set CC

**SETHI**

**SAVE**

**RESTORE**

### Floating-Point Operations

**Fp convert**

<table>
<thead>
<tr>
<th>Integer</th>
<th>Single</th>
<th>Double</th>
<th>eXtended</th>
<th>Single</th>
<th>Double</th>
<th>eXtended</th>
<th>Fp</th>
<th>ADD</th>
<th>SUB</th>
<th>Brad</th>
<th>MULtiply</th>
<th>DIVide</th>
<th>SQRoot</th>
<th>Comp</th>
<th>COMPare and Exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fp</td>
<td>MOVe</td>
<td>NEGe</td>
<td>ABSolute</td>
<td>Single</td>
<td></td>
<td></td>
<td></td>
<td>ADD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Control Transfer

**Branch**

- **Integer CC**
- **Floating-point CC**
- **Coprocessor CC**

- **normal**
- **Anull delay instruction**

- **Jump and Link**
- **Return from Trap**

- **CALL**
- **Trap on Integer CC**

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**Figure 1.1. SPARC Instruction Mnemonic Summary**
2. Definitions

This section provides a detailed definition for each CY7C601 instruction. Each definition includes: the instruction operation; suggested assembly language syntax; a description of the salient features, restrictions and trap conditions; a list of synchronous or floating-point coprocessor traps which can occur as a consequence of executing the instruction; and the instruction format and op codes. Instructions are defined in alphabetical order with the instruction mnemonic shown in large bold type at the top of the page for easy reference. The instruction set summary that precedes the definitions, (Table 1.2), groups the instructions by type.

Table 1.1 identifies the abbreviations and symbols used in the instruction definitions. An example of how some of the description notations are used is given below in Figure 1.2. Register names, labels and other aspects of the syntax used in these instructions are described in the previous section.

![Image of LDD instruction](image)

**Figure 1.2. Instruction Description**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>Instruction field that controls instruction annulling during control transfers</td>
</tr>
<tr>
<td>AND, OR, XOR, etc.</td>
<td>AND, OR, XOR, etc operators</td>
</tr>
<tr>
<td>asr_reg</td>
<td>Any implemented ASR (Ancillary State )</td>
</tr>
<tr>
<td>c</td>
<td>The icc carry bit</td>
</tr>
<tr>
<td>ccc</td>
<td>The coprocessor condition code field of the CCSR</td>
</tr>
<tr>
<td>CONCAT</td>
<td>Concatenate</td>
</tr>
<tr>
<td>cond</td>
<td>Instruction field that selects the condition code test for branches</td>
</tr>
</tbody>
</table>

Table 1.1. Instruction Description Notations
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>creg</td>
<td>Communication Coprocessor Register: can be %ccsr, %ccfr, %ccpr, %cccrc</td>
</tr>
<tr>
<td>CWP</td>
<td>PSR's Current Window Pointer field</td>
</tr>
<tr>
<td>disp22</td>
<td>Instruction field that contains the 22-bit sign-extended displacement for branches</td>
</tr>
<tr>
<td>disp30</td>
<td>Instruction field that contains the 30-bit word displacement for calls</td>
</tr>
<tr>
<td>EC</td>
<td>PSR's Enable Coprocessor bit</td>
</tr>
<tr>
<td>EF</td>
<td>PSR's Enable FPU bit</td>
</tr>
<tr>
<td>ET</td>
<td>PSR's Enable Traps bit</td>
</tr>
<tr>
<td>i</td>
<td>Instruction field that selects rs2 or sign_extend(simm13) as the second operand</td>
</tr>
<tr>
<td>icc</td>
<td>The integer condition code field of the PSR</td>
</tr>
<tr>
<td>imm22</td>
<td>Instruction field that contains the 22-bit constant used by SETHI</td>
</tr>
<tr>
<td>n</td>
<td>The icc negative bit</td>
</tr>
<tr>
<td>not</td>
<td>Logical complement operator</td>
</tr>
<tr>
<td>nPC</td>
<td>Next Program Counter</td>
</tr>
<tr>
<td>opc</td>
<td>Instruction field that specifies the count for Coprocessor-operate instructions</td>
</tr>
<tr>
<td>operand2</td>
<td>Either r[rs2] or sign_extend(simm13)</td>
</tr>
<tr>
<td>PC</td>
<td>Program Counter</td>
</tr>
<tr>
<td>pS</td>
<td>PSR's previous Supervisor bit</td>
</tr>
<tr>
<td>PSR</td>
<td>Processor State Register</td>
</tr>
<tr>
<td>r[15]</td>
<td>A directly addressed register (could be floating-point or coprocessor)</td>
</tr>
<tr>
<td>rd</td>
<td>Instruction field that specifies the destination register (except for store)</td>
</tr>
<tr>
<td>r[rd]</td>
<td>Depending on context, the integer register (or its contents) specified by the instruction field, e.g., rd, rs1, rs2</td>
</tr>
<tr>
<td>r[rd]&lt;31&gt;</td>
<td>&lt;&gt; are used to specify bit fields of a particular register or I/O signal</td>
</tr>
<tr>
<td>[r[rs1] + r[rs2]]</td>
<td>The contents of the address specified by r[rs1] + r[rs2]</td>
</tr>
<tr>
<td>rs1</td>
<td>Instruction field that specifies the source 1 register</td>
</tr>
<tr>
<td>rs2</td>
<td>Instruction field that specifies the source 2 register</td>
</tr>
<tr>
<td>S</td>
<td>PSR's Supervisor bit</td>
</tr>
<tr>
<td>shcnt</td>
<td>Instruction field that specifies the count for shift instructions</td>
</tr>
<tr>
<td>sign_extend(simm13)</td>
<td>Instruction field that contains the 13-bit, sign-extended immediate value</td>
</tr>
</tbody>
</table>

### Symbol Description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TBR</td>
<td>Trap Base Register</td>
</tr>
<tr>
<td>tt</td>
<td>TBR's trap type field</td>
</tr>
<tr>
<td>uf</td>
<td>Floating-point exception: underflow</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>v</td>
<td>The icc overflow bit</td>
</tr>
<tr>
<td>WIM</td>
<td>Window Invalid Mask register</td>
</tr>
<tr>
<td>Y</td>
<td>Y Register</td>
</tr>
<tr>
<td>z</td>
<td>The icc zero bit</td>
</tr>
<tr>
<td>-</td>
<td>Subtract</td>
</tr>
<tr>
<td>x</td>
<td>Multiply</td>
</tr>
<tr>
<td>/</td>
<td>Divide</td>
</tr>
<tr>
<td>&lt;--</td>
<td>Replaced by</td>
</tr>
<tr>
<td>7FFFFFF H</td>
<td>Hexadecimal number representation</td>
</tr>
<tr>
<td>+</td>
<td>Add</td>
</tr>
</tbody>
</table>
Table 1.2. Instruction Set Summary

<table>
<thead>
<tr>
<th>Name</th>
<th>Operation</th>
<th>Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDSh(LDSBA)</td>
<td>Load Signed Byte</td>
<td>2</td>
</tr>
<tr>
<td>LDSh(LDSBA)</td>
<td>(from Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>LDUB(LDUBA)</td>
<td>Load Signed Halfword</td>
<td>2</td>
</tr>
<tr>
<td>LDUB(LDUBA)</td>
<td>(from Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>LDULH(LDULHA)</td>
<td>Load Unsigned Byte</td>
<td>2</td>
</tr>
<tr>
<td>LDULH(LDULHA)</td>
<td>(from Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>LD(LDA)</td>
<td>Load Word</td>
<td>2</td>
</tr>
<tr>
<td>LD(LDA)</td>
<td>(from Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>LD(DDA)</td>
<td>Load Doubleword</td>
<td>3</td>
</tr>
<tr>
<td>LD(DDA)</td>
<td>(from Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>LDF</td>
<td>Load Floating Point</td>
<td>2</td>
</tr>
<tr>
<td>LDF</td>
<td>(from Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>LDFF</td>
<td>Load Double Floating Point</td>
<td>3</td>
</tr>
<tr>
<td>LDFF</td>
<td>(from Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>LDC</td>
<td>Load Coprocessor</td>
<td>2</td>
</tr>
<tr>
<td>LDC</td>
<td>(from Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>LDCSR</td>
<td>Load Coprocessor State Register</td>
<td>2</td>
</tr>
<tr>
<td>LDCSR</td>
<td>(from Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>STB(STBA)</td>
<td>Store Byte</td>
<td>3</td>
</tr>
<tr>
<td>STB(STBA)</td>
<td>(into Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>STH(STHA)</td>
<td>Store Halfword</td>
<td>3</td>
</tr>
<tr>
<td>STH(STHA)</td>
<td>(into Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>STI(STA)</td>
<td>Store Word</td>
<td>3</td>
</tr>
<tr>
<td>STI(STA)</td>
<td>(into Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>STD(STD)</td>
<td>Store Doubleword</td>
<td>4</td>
</tr>
<tr>
<td>STD(STD)</td>
<td>(into Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>LDST(U/LDSTUBA)</td>
<td>Atomic Load/Store Signed byte</td>
<td>4</td>
</tr>
<tr>
<td>LDST(U/LDSTUBA)</td>
<td>Store word with Memory</td>
<td></td>
</tr>
<tr>
<td>SWAP(SWAPA)</td>
<td>(in Alternate Space)</td>
<td></td>
</tr>
<tr>
<td>LS</td>
<td>Add</td>
<td>1</td>
</tr>
<tr>
<td>LS</td>
<td>(and mod y)</td>
<td></td>
</tr>
<tr>
<td>LADD(LDAddc)</td>
<td>Tagged Add and modify icc</td>
<td>1</td>
</tr>
<tr>
<td>LADD(LDAddc)</td>
<td>(and Trap on overflow)</td>
<td></td>
</tr>
<tr>
<td>SUB(SUBcc)</td>
<td>Subtract</td>
<td>1</td>
</tr>
<tr>
<td>SUB(SUBcc)</td>
<td>(and mod y)</td>
<td></td>
</tr>
<tr>
<td>SUB(SUBcc)</td>
<td>(and Trap on overflow)</td>
<td></td>
</tr>
<tr>
<td>MULSec</td>
<td>Multiply Step and modify icc</td>
<td>1</td>
</tr>
<tr>
<td>AND(ANDExx)</td>
<td>And</td>
<td>1</td>
</tr>
<tr>
<td>AND(ANDExx)</td>
<td>(and mod y)</td>
<td></td>
</tr>
<tr>
<td>AND(NANDNcc)</td>
<td>And Not</td>
<td>1</td>
</tr>
<tr>
<td>AND(NANDNcc)</td>
<td>(and mod y)</td>
<td></td>
</tr>
<tr>
<td>ORN(ORNcc)</td>
<td>Inclusive Or</td>
<td>1</td>
</tr>
<tr>
<td>ORN(ORNcc)</td>
<td>(and mod y)</td>
<td></td>
</tr>
<tr>
<td>XORX(NORRcc)</td>
<td>Exclusive Or</td>
<td>1</td>
</tr>
<tr>
<td>XORX(NORRcc)</td>
<td>(and mod y)</td>
<td></td>
</tr>
<tr>
<td>SLL</td>
<td>Shift Left Logical</td>
<td>1</td>
</tr>
<tr>
<td>SRL</td>
<td>Shift Right Logical</td>
<td>1</td>
</tr>
<tr>
<td>SRA</td>
<td>Shift Right Arithmetic</td>
<td>1</td>
</tr>
<tr>
<td>SETH</td>
<td>Set High 22 Bits of r Register</td>
<td>1</td>
</tr>
<tr>
<td>SAVE</td>
<td>Save caller’s window</td>
<td>1</td>
</tr>
<tr>
<td>RESTORE</td>
<td>Restore caller’s window</td>
<td>1</td>
</tr>
<tr>
<td>Bcc</td>
<td>Branch on Condition Codes</td>
<td>1**</td>
</tr>
<tr>
<td>Bcc</td>
<td>Branch on Floating Point Condition Codes</td>
<td>1**</td>
</tr>
<tr>
<td>CALL</td>
<td>Call</td>
<td>1**</td>
</tr>
<tr>
<td>JMP</td>
<td>Jump and Link</td>
<td>2**</td>
</tr>
<tr>
<td>RET</td>
<td>Return from trap</td>
<td>2**</td>
</tr>
<tr>
<td>Icc</td>
<td>Trap on Integer Condition Codes</td>
<td>(1 if taken)</td>
</tr>
<tr>
<td>RDY</td>
<td>Read Y Register</td>
<td>1</td>
</tr>
<tr>
<td>RDPSR</td>
<td>Read Processor State Register</td>
<td>1</td>
</tr>
<tr>
<td>RDWIM</td>
<td>Read Window Invalid Mask</td>
<td>1</td>
</tr>
<tr>
<td>RTBR</td>
<td>Read Trap Base Register</td>
<td>1</td>
</tr>
<tr>
<td>WR</td>
<td>Write Y Register</td>
<td>1</td>
</tr>
<tr>
<td>WRPSR</td>
<td>Write Processor State Register</td>
<td>1</td>
</tr>
<tr>
<td>WRWIM</td>
<td>Write Window Invalid Mask</td>
<td>1</td>
</tr>
<tr>
<td>WRTBR</td>
<td>Write Trap Base Register</td>
<td>1</td>
</tr>
<tr>
<td>UNIMP</td>
<td>Unimplemented Instruction</td>
<td>1</td>
</tr>
<tr>
<td>IFLUSH</td>
<td>Instruction Cache Flush</td>
<td>1</td>
</tr>
<tr>
<td>COP0</td>
<td>Floating Point Unit Operations</td>
<td>1 to Launch</td>
</tr>
<tr>
<td>COP1</td>
<td>Coprocessor Operations</td>
<td>1 to Launch</td>
</tr>
</tbody>
</table>

* privileged instruction
** assuming only slot is filled with useful instructions

MATRA MHS
Rev. A (10/09/96)
ADD

Operation: 

\[ r[rd] \leftarrow r[rs1] + (r[rs2] \text{ or sign extnd(simm13)}) \]

Assembler Syntax: 

\[
\text{add } \text{reg}_{rs1}, \text{ reg}_{or\_imm}, \text{ reg}_{rd}
\]

Description: The ADD instruction adds the contents of the register named in the \(rs1\) field, \(r[rs1]\), to either the contents of \(r[rs2]\) if the instruction’s \(i\) bit equals zero, or to the 13-bit, sign-extended immediate operand contained in the instruction if \(i\) equals one. The result is placed in the register specified in the \(rd\) field.

Traps: 

none

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0 0 0 0 0</td>
<td>rs1</td>
<td>0=0</td>
<td>ignored</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0 0 0 0 0</td>
<td>rs1</td>
<td>0=1</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
ADDcc

Add and modify icc

**Operation:**

\[ r[rd] \leftarrow r[rs1] + \text{operand2}, \text{where } \text{operand2} = \begin{cases} r[rs2] & \text{if } i = 0 \\ \text{sign extnd(simm13)} & \text{if } i = 1 \end{cases} \]

- **n** \( \leftarrow r[rd]<31> \)
- **z** \( \leftarrow \) if \( r[rd] = 0 \) then 1, else 0
- **v** \( \leftarrow (r[rs1]<31> \text{ AND } \text{operand2}<31> \text{ AND } \neg r[rd]<31>) \text{ OR } (\neg r[rs1]<31> \text{ AND } \neg \text{operand2}<31> \text{ AND } r[rd]<31>) \)
- **c** \( \leftarrow (r[rs1]<31> \text{ AND } \text{operand2}<31>) \text{ OR } (\neg r[rd]<31> \text{ AND } (r[rs1]<31> \text{ OR } \text{operand2}<31>)) \)

**Assembler Syntax:**

```
addcc reg, reg_or_imm, reg
```

**Description:**

ADDcc adds the contents of \( r[rs1] \) to either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or to a 13-bit, sign-extended immediate operand if \( i \) equals one. The result is placed in the register specified in the \( rd \) field. In addition, ADDcc modifies all the integer condition codes in the manner described above.

**Traps:**

none

**Format:**

```
1 0  rd  0 1 0 0 0 0  rs1  i=0  ignored  rs2
```

```
1 0  rd  0 1 0 0 0 0  rs1  i=1  simm13
```
ADDX

Add with Carry

**Operation:**

\[ r[rd] \leftarrow r[rs1] + (r[rs2] \text{ or sign extnd(simm13)}) + c \]

**Assembler Syntax:**

`addx reg_rs1, reg_or_imm, reg_rd`

**Description:**

ADDX adds the contents of `r[rs1]` to either the contents of `r[rs2]` if the instruction’s `i` bit equals zero, or to a 13-bit, sign-extended immediate operand if `i` equals one. It then adds the PSR’s carry bit (`c`) to that result. The final result is placed in the register specified in the `rd` field.

**Traps:**

none

**Format:**

```
  31 30 29 28 27 26 25 24 19 18 14 13 12  5  4  0
  1 0  rd  0 0 1 0 0 0 rs1  i=0 ignored rs2

  31 30 29 28 27 26 25 24 19 18 14 13 12  0
  1 0  rd  0 0 1 0 0 0 rs1  i=1 simm13
```
ADDXcc | Add with Carry and modify icc | ADDXcc
---|---|---

**Operation:**
\[
r[rd] \leftarrow r[rs1] + \text{operand2} + c, \text{ where operand2} = (r[rs2] \text{ or sign extnd(simm13)})
\]

\[
n \leftarrow r[rd]<31>
\]

\[
z \leftarrow \begin{cases} 1 & \text{if } r[rd] = 0 \\ 0 & \text{else} \end{cases}
\]

\[
v \leftarrow (r[rs1]<31> \text{ AND operand2}<31> \text{ AND not } r[rd]<31>) \text{ OR (not } r[rs1]<31> \text{ AND not operand2}<31> \text{ AND } r[rd]<31>)
\]

\[
c \leftarrow (r[rs1]<31> \text{ AND operand2}<31>) \text{ OR (not } r[rd]<31> \text{ AND (r[rs1]<31> OR operand2}<31>))
\]

**Assembler Syntax:**
\[
\text{ADDXcc } \text{reg}_{rs1}, \text{ reg}_{or IMM}, \text{ reg}_{rd}
\]

**Description:**
ADDXcc adds the contents of \(r[rs1]\) to either the contents of \(r[rs2]\) if the instruction’s \(i\) bit equals zero, or to a 13-bit, sign-extended immediate operand if \(i\) equals one. It then adds the PSR’s carry bit (\(c\)) to that result. The final result is placed in the register specified in the \(rd\) field. ADDXcc also modifies all the integer condition codes in the manner described above.

**Traps:**
none

**Format:**

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<tr>
<th>31</th>
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<th>29</th>
<th>25</th>
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<th>14</th>
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<th>4</th>
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<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
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<td>rs1</td>
<td>(i=0)</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
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<td>0</td>
<td>simm13</td>
<td>rs1</td>
<td>(i=1)</td>
<td></td>
</tr>
</tbody>
</table>
AND

Operation: \( r[rd] \leftarrow r[rs1] \land (r[rs2] \text{ or } \text{sign extnd(simm13)}) \)

Assembler Syntax: \( \text{and } r_{rs1}, r_{or \_imm}, r_{rd} \)

Description: This instruction does a bitwise logical AND of the contents of register \( r[rs1] \) with either the contents of \( r[rs2] \) (if if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if if bit field \( i=1 \)). The result is stored in register \( r[rd] \).

Traps: none

Format:

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<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
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<td>i=0</td>
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</tr>
</tbody>
</table>
```

```
<table>
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<tr>
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<td></td>
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<td></td>
<td></td>
<td>simm13</td>
</tr>
</tbody>
</table>
```
**ANDcc**

**And and modify icc**

**ANDcc**

**Operation:**
\[ r[rd] \leftarrow r[rs1] \text{ AND } (r[rs2] \text{ or sign extnd(simm13)}) \]

\[ n \leftarrow r[rd]<31> \]

\[ z \leftarrow \text{if } r[rd] = 0 \text{ then 1, else 0} \]

\[ v \leftarrow 0 \]

\[ c \leftarrow 0 \]

**Assembler Syntax:**
\[ \text{andc} \ reg_{rs1}, \ reg_{or\_imm}, \ reg_{rd} \]

**Description:**
This instruction does a bitwise logical AND of the contents of register \([rs1]\) with either the contents of \([rs2]\) (if if bit field \(i=0\)) or the 13-bit, sign-extended immediate value contained in the instruction (if if bit field \(i=1\)). The result is stored in register \([rd]\). \text{ANDcc} also modifies all the integer condition codes in the manner described above.

**Traps:**
none

**Format:**

```
31 30 29 25 24 19 18 14 13 12 5 4 0
1 0    rd  0 1 0 0 0 1    rs1  i=0  ignored  rs2
```

```
31 30 29 25 24 19 18 14 13 12 0
1 0    rd  0 1 0 0 0 1    rs1  i=1  simm13
```
ANDN

Operation:
\[ r[rd] \leftarrow r[rs1] \text{ AND } (r[rs2] \text{ or sign extnd(simm13)}) \]

Assembler Syntax:
\text{andn reg\_s1, reg\_or\_imm, reg\_rd}

Description:
ANDN does a bitwise logical AND of the contents of register \( r[rs1] \) with the logical compliment (not) of either \( r[rs2] \) (if if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if if bit field \( i=1 \)). The result is stored in register \( r[rd] \).

Traps:
none

Format:

```
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<tr>
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<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
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<th>18</th>
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</thead>
<tbody>
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<td>i=0</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>rs2</td>
</tr>
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</table>
```

```
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<th>29</th>
<th>25</th>
<th>24</th>
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<th>14</th>
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<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>000101</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
ANDNcc  And Not and modify icc  ANDNcc

Operation:
\[ r_{[rd]} \leftarrow r_{[rs1]} \text{ AND } (r_{[rs2]} \text{ or sign extnd(simm13)}) \]
\[ n \leftarrow r_{[rd]} < 31 > \]
\[ z \leftarrow \text{if } r_{[rd]} = 0 \text{ then } 1, \text{ else } 0 \]
\[ v \leftarrow 0 \]
\[ c \leftarrow 0 \]

Assembler Syntax:
\text{andncc} \text{ reg}_{(rs1)}, \text{ reg}_{or_imm}, \text{ reg}_{rd} \]

Description:
ANDNcc does a bitwise logical AND of the contents of register \text{r}[rs1] with the logical compliment (not) of either \text{r}[rs2] (if bit field i=0) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field i=1). The result is stored in register \text{r}[rd]. ANDNcc also modifies all the integer condition codes in the manner described above.

Traps:
none

Format:

```
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<tr>
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<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
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<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
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<td>rd</td>
<td>0 1 0 1 0 1</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>
```

```
<table>
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<tr>
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<th>28</th>
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<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0 1 0 1 0 1</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
Bicc

Integer Conditional Branch

Operation:

PC ← nPC
If condition true then nPC ← PC + (sign extnd(disp22) x 4)
else nPC ← nPC + 4

Assembler Syntax:

\texttt{ba[a]}\quad label
\texttt{bn[a]}\quad label
\texttt{bnc[a]}\quad label\quad synonym:.bnz
\texttt{be[a]}\quad label\quad synonym: bz
\texttt{bg[a]}\quad label
\texttt{ble[a]}\quad label
\texttt{bge[a]}\quad label
\texttt{bl[a]}\quad label
\texttt{bgu[a]}\quad label
\texttt{bgeu[a]}\quad label\quad synonym: bgeu
\texttt{bcs[a]}\quad label\quad synonym: blu
\texttt{bpos[a]}\quad label
\texttt{bne[a]}\quad label
\texttt{bvc[a]}\quad label
\texttt{bvs[a]}\quad label

Note: The instruction’s annul bit field, a, is set by appending “,a” after the branch name. If it is not
append, the a field is automatically reset. “,a” is shown in braces because it is optional.

Description:

The Bicc instructions (except for BA and BN) evaluate specific integer condition code combinations
(from the PSR’s \texttt{icc} field) based on the branch type as specified by the value in the instruction’s \texttt{cond}
field. If the specified combination of condition codes evaluates as true, the branch is taken, causing a
delayed, PC-relative control transfer to the address (PC + 4) + (sign extnd(disp22) x 4). If the condition
codes evaluate as false, the branch is not taken. Refer to Section NO TAG for additional
information on control transfer instructions.

If the branch is not taken, the annul bit field (a) is checked. If a is set, the instruction immediate-
ly following the branch instruction (the delay instruction) is not executed (i.e., it is annulled). If the
annul field is zero, the delay instruction is executed. If the branch is taken, the annul field is
ignored, and the delay instruction is executed. See Section NO TAG regarding delay-branch
instructions.

Branch Never (BN) executes like a NOP, except it obeys the annul field with respect to its delay
instruction.

Branch Always (BA), because it always branches regardless of the condition codes, would nor-
mally ignore the annul field. Instead, it follows the same annul field rules: if a=1, the delay
instruction is annulled; if a=0, the delay instruction is executed.

The delay instruction following a Bicc (other than BA) should not be a delayed-control-transfer
instruction. The results of following a Bicc with another delayed control transfer instruction
are implementation-dependent and therefore unpredictable.

Traps:

none
<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Cond.</th>
<th>Operation</th>
<th>Instruction Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>BN</td>
<td>0000</td>
<td>Branch Never</td>
<td>No test</td>
</tr>
<tr>
<td>BE</td>
<td>0001</td>
<td>Branch on Equal</td>
<td>$z$</td>
</tr>
<tr>
<td>BLE</td>
<td>0010</td>
<td>Branch on Less or Equal</td>
<td>$z$ OR (n XOR v)</td>
</tr>
<tr>
<td>BL</td>
<td>0011</td>
<td>Branch on Less</td>
<td>n XOR v</td>
</tr>
<tr>
<td>BLEU</td>
<td>0100</td>
<td>Branch on Less or Equal, Unsigned</td>
<td>c OR z</td>
</tr>
<tr>
<td>BCS</td>
<td>0101</td>
<td>Branch on Carry Set (Less than, Unsigned)</td>
<td>c</td>
</tr>
<tr>
<td>BNEG</td>
<td>0110</td>
<td>Branch on Negative</td>
<td>n</td>
</tr>
<tr>
<td>BVS</td>
<td>0111</td>
<td>Branch on oVerflow Set</td>
<td>v</td>
</tr>
<tr>
<td>BA</td>
<td>1000</td>
<td>Branch Always</td>
<td>No test</td>
</tr>
<tr>
<td>BNE</td>
<td>1001</td>
<td>Branch on Not Equal</td>
<td>not z</td>
</tr>
<tr>
<td>BG</td>
<td>1010</td>
<td>Branch on Greater</td>
<td>not(z OR (n XOR v))</td>
</tr>
<tr>
<td>BGE</td>
<td>1011</td>
<td>Branch on Greater or Equal</td>
<td>not(n XOR v)</td>
</tr>
<tr>
<td>BGU</td>
<td>1100</td>
<td>Branch on Greater, Unsigned</td>
<td>not(c OR z)</td>
</tr>
<tr>
<td>BCC</td>
<td>1101</td>
<td>Branch on Carry Clear (Greater than or Equal, Unsigned)</td>
<td>not c</td>
</tr>
<tr>
<td>BPOS</td>
<td>1110</td>
<td>Branch on Positive</td>
<td>not n</td>
</tr>
<tr>
<td>BVC</td>
<td>1111</td>
<td>Branch on oVerflow Clear</td>
<td>not v</td>
</tr>
</tbody>
</table>

Format:

```
 31  30  29  28  25  24  22  21  0
 0  0  a  cond.  0  1  0  disp22
```
CALL

Operation: r[15] ← PC
PC ← nPC
nPC ← PC + (disp30 x 4)

Assembler Syntax: call label

Description: The CALL instruction causes a delayed, unconditional, PC-relative control transfer to the address (PC + 4) + (disp30 x 4). The CALL instruction does not have an annul bit, therefore the delay slot instruction following the CALL instruction is always executed (See Section NO TAG). CALL first writes its return address (PC) into the outs register, r[15], and then adds 4 to the PC. The 32-bit displacement which is added to the new PC is formed by appending two low-order zeros to the 30-bit word displacement contained in the instruction. Consequently, the target address can be anywhere in the CY7C601's user or supervisor address space.

If the instruction following a CALL uses register r[15] as a source operand, hardware interlocks add a one cycle delay.

Programming note: a register-indirect CALL can be constructed using a JMPL instruction with rd set to 15.

Traps: none

Format:

\[
\begin{array}{ccc}
31 & 30 & 29 \\
\hline
0 & 1 & \text{disp30}
\end{array}
\]
CBcc

Coprocessor Conditional Branch

Operation:

PC ← nPC

If condition true then nPC ← PC + (sign extnd(disp22) x 4)
else nPC ← nPC + 4

Assembler Syntax:

cba{,a} label
cbn{,a} label
cb3{,a} label
cb2{,a} label
cb23{,a} label
cb1{,a} label
cb13{,a} label
cb12{,a} label
cb123{,a} label
cb0{,a} label
cb03{,a} label
cb02{,a} label
cb023{,a} label
cb01{,a} label
cb013{,a} label
cb012{,a} label

Note: The instruction’s annul bit field, a, is set by appending “.a” after the branch name. If it is not appended, the a field is automatically reset. “.a” is shown in braces because it is optional.

Description:

The CBccc instructions (except for CBA and CBN) evaluate specific coprocessor condition code combinations (from the CCC<1:0> inputs) based on the branch type as specified by the value in the instruction’s cond field. If the specified combination of condition codes evaluates as true, the branch is taken, causing a delayed, PC-relative control transfer to the address (PC + 4) + (sign extnd(disp22) x 4). If the condition codes evaluate as false, the branch is not taken. See Section NO TAG regarding control transfer instructions.

If the branch is not taken, the annul bit field (a) is checked. If a is set, the instruction immediately following the branch instruction (the delay instruction) is not executed (i.e., it is annulled). If the annul field is zero, the delay instruction is executed. If the branch is taken, the annul field is ignored, and the delay instruction is executed. See Section NO TAG regarding delayed branching.

Branch Never (CBN) executes like a NOP, except it obeys the annul field with respect to its delay instruction.

Branch Always (CBA), because it always branches regardless of the condition codes, would normally ignore the annul field. Instead, it follows the same annul field rules: if a = 1, the delay instruction is annulled; if a = 0, the delay instruction is executed.

To prevent misapplication of the condition codes, a non-coprocessor instruction must immediately precede a CBccc instruction.

A CBccc instruction generates a cp_disabled trap (and does not branch or annul) if the PSR’s EC bit is reset or if no coprocessor is present.
Traps: cp_disabled
        cp_exception

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>cond.</th>
<th>CCC&lt;:1:9&gt; test</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBN</td>
<td>0000</td>
<td>Never</td>
</tr>
<tr>
<td>CB123</td>
<td>0001</td>
<td>1 or 2 or 3</td>
</tr>
<tr>
<td>CB12</td>
<td>0010</td>
<td>1 or 2</td>
</tr>
<tr>
<td>CB13</td>
<td>0011</td>
<td>1 or 3</td>
</tr>
<tr>
<td>CB1</td>
<td>0100</td>
<td>1</td>
</tr>
<tr>
<td>CB23</td>
<td>0101</td>
<td>2 or 3</td>
</tr>
<tr>
<td>CB2</td>
<td>0110</td>
<td>2</td>
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<tr>
<td>CB3</td>
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<td>1011</td>
<td>0 or 2</td>
</tr>
<tr>
<td>CB023</td>
<td>1100</td>
<td>0 or 2 or 3</td>
</tr>
<tr>
<td>CB01</td>
<td>1101</td>
<td>0 or 1</td>
</tr>
<tr>
<td>CB013</td>
<td>1110</td>
<td>0 or 1 or 3</td>
</tr>
<tr>
<td>CB012</td>
<td>1111</td>
<td>0 or 1 or 2</td>
</tr>
</tbody>
</table>

Format:

```
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<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>25</th>
<th>24</th>
<th>22</th>
<th>21</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>a</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>disp22</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
**Operation:** Dependent on Coprocessor implementation

**Assembler Syntax:** Unspecified

**Description:** CPop1 and CPop2 are the instruction formats for coprocessor operate instructions. The op3 field for CPop1 is 110110; for CPop2 it's 110111. The coprocessor operations themselves are encoded in the opc field and are dependent on the coprocessor implementation. Note that this does not include load/store coprocessor instructions, which fall into the integer unit's load/store instruction category.

All CPop instructions take all operands from, and return all results to, the coprocessor’s registers. The data types supported, how the operands are aligned, and whether a CPop generates a cp_exception trap are Coprocessor dependent.

A CPop instruction causes a cp_disabled trap if the PSR’s EC bit is reset or if no coprocessor is present.

**Traps:**
cp_disabled
cp_exception

**Format:**

```
  31  30  29  28  27  26  25  24  19  18  14  13  5  4  0
  1  0  rd  1 1 0 1 1 0  rs1  opc  rs2
```

```
  31  30  29  28  27  26  25  24  19  18  14  13  5  4  0
  1  0  rd  1 1 0 1 1 1  rs1  opc  rs2
```
FABSs  
**Absolute Value Single**  
**(FPU Instruction Only)**

**Operation:**  
\[ f[rd] \leftarrow f[rs2] \text{ AND } 7FFFFFFF H \]

**Assembler Syntax:**  
\[ \text{fabss } freg_{rs2}, freg_{rd} \]

**Description:**  
The FABSs instruction clears the sign bit of the word in \( f[rs2] \) and places the result in \( f[rd] \). It does not round.  
Since \( rs2 \) can be either an even or odd register, FABSs can also operate on the high-order words of double and extended operands, which accomplishes sign bit clear for these data types.

**Traps:**  
- \( \text{fp\_disabled} \)
- \( \text{fp\_exception*} \)

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>ignored</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

*NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.*
FADDd

Add Double

(FPU Instruction Only)

Operation: \( f[d] ← f[s1]d + f[s2]d \)

Assembler Syntax: \( fadd \, freg_{rs1}, \, freg_{rs2}, \, freg_{rd} \)

Description: The FADDd instruction adds the contents of \( f[rs1] \) CONCAT \( f[rs1+1] \) to the contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd] \) and \( f[rd+1] \).

Traps: fp_disabled, fp_exception (of, uf, nv, nx)

Format:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 0  | rd | 11 | 10 | 0  | rs1| 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
FADDs

(FPU Instruction Only)

Operation: \[ f[rd] \leftarrow f[rs1] + f[rs2] \]

Assembler Syntax: `fadds freg\_rs1, freg\_rs2, freg\_rd`

Description: The FADDs instruction adds the contents of \( f[rs1] \) to the contents of \( f[rs2] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd] \).

Traps: `fp\_disabled`
`fp\_exception (of, uf, nv, nx)`

Format:

\[
\begin{array}{cccccccc}
1 & 0 & rd & 1 & 1 & 0 & 1 & 0 & 0 & rs1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & rs2
\end{array}
\]
FADDx

Add Extended FADDx

(FPU Instruction Only)

Operation: \[ f[rd]x \leftarrow f[rs1]x + f[rs2]x \]

Assembler Syntax: \( \text{faddx } freg_{rs1}, freg_{rs2}, freg_{rd} \)

Description: The FADDx instruction adds the contents of \( f[rs1] \) CONCAT \( f[rs1+1] \) CONCAT \( f[rs1+2] \) to the contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) CONCAT \( f[rs2+2] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd], f[rd+1], \) and \( f[rd+2] \).

Traps: \( \text{fp_disabled, fp_exception (of, uf, nv, nx)} \)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>11</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

\( f[rs1], f[rs2], f[rd] \)
**FBfcc**

**Floating-Point Conditional Branch**

**Operation:**

\[
\text{PC} \leftarrow \text{nPC}
\]

If condition true then \( \text{nPC} \leftarrow \text{PC} + (\text{sign extnd(disp22)} \times 4) \)

else \( \text{nPC} \leftarrow \text{nPC} + 4 \)

**Assembler Syntax:**

- `fba{,a} label`
- `fbn{,a} label`
- `fbu{,a} label`
- `fbc{,a} label`
- `fbcg{,a} label`
- `fbil{,a} label`
- `fbul{,a} label`
- `fbtn{,a} label`
- `fbn0{,a} label`

**Note:** The instruction’s annul bit field, \( a \), is set by appending “\( ,a \)” after the branch name. If it is not appended, the \( a \) field is automatically reset. “\( ,a \)” is shown in braces because it is optional.

**Description:**

The FBfcc instructions (except for FBA and FBN) evaluate specific floating-point condition code combinations (from the FCC<1:0> inputs) based on the branch type, as specified by the value in the instruction’s `cond` field. If the specified combination of condition codes evaluates as true, the branch is taken, causing a delayed, PC-relative control transfer to the address \( (\text{PC} + 4) + (\text{sign extnd(disp22)} \times 4) \) if the condition codes evaluate as false, the branch is not taken. See Section NO TAG for additional information on control transfer instructions.

If the branch is not taken, the annul bit field (\( a \)) is checked. If \( a \) is set, the instruction immediately following the branch instruction (the delay instruction) is not executed (i.e., it is annulled). If the annul field is zero, the delay instruction is executed. If the branch is taken, the annul field is ignored, and the delay instruction is executed. See Section NO TAG regarding delayed branch instructions.

Branch Never (FBN) executes like a NOP, except it obeys the annul field with respect to its delay instruction.

Branch Always (FBA), because it always branches regardless of the condition codes, would normally ignore the annul field. Instead, it follows the same annul field rules: if \( a=1 \), the delay instruction is annulled; if \( a=0 \), the delay instruction is executed.

To prevent misapplication of the condition codes, a non-floating-point instruction must immediately precede an FBfcc instruction.

An FBfcc instruction generates an fp_disabled trap (and does not branch or annul) if the PSR’s EF bit is reset or if no Floating-Point Unit is present.
Traps:
- `fp_disabled`
- `fp_exception`

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Cond.</th>
<th>Operation</th>
<th>fcc Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>FBN</td>
<td>0000</td>
<td>Branch Never</td>
<td>no test</td>
</tr>
<tr>
<td>FBNE</td>
<td>0001</td>
<td>Branch on Not Equal</td>
<td>U or L, or G</td>
</tr>
<tr>
<td>FBLG</td>
<td>0010</td>
<td>Branch on Less or Greater</td>
<td>L or G</td>
</tr>
<tr>
<td>FBUL</td>
<td>0011</td>
<td>Branch on Unordered or Less</td>
<td>U or L</td>
</tr>
<tr>
<td>FBL</td>
<td>0100</td>
<td>Branch on Less</td>
<td>L</td>
</tr>
<tr>
<td>FBUG</td>
<td>0101</td>
<td>Branch on Unordered or Greater</td>
<td>U or G</td>
</tr>
<tr>
<td>FBG</td>
<td>0110</td>
<td>Branch on Greater</td>
<td>G</td>
</tr>
<tr>
<td>FBU</td>
<td>0111</td>
<td>Branch on Unordered</td>
<td>U</td>
</tr>
<tr>
<td>FBA</td>
<td>1000</td>
<td>Branch Always</td>
<td>no test</td>
</tr>
<tr>
<td>FBE</td>
<td>1001</td>
<td>Branch on Equal</td>
<td>E</td>
</tr>
<tr>
<td>FBUE</td>
<td>1010</td>
<td>Branch on Unordered or Equal</td>
<td>U or E</td>
</tr>
<tr>
<td>FBGE</td>
<td>1011</td>
<td>Branch on Greater or Equal</td>
<td>G or E</td>
</tr>
<tr>
<td>FBUGE</td>
<td>1100</td>
<td>Branch on Unordered or Greater or Equal</td>
<td>U or G or E</td>
</tr>
<tr>
<td>FBLE</td>
<td>1101</td>
<td>Branch on Less or Equal</td>
<td>L or E</td>
</tr>
<tr>
<td>FBULE</td>
<td>1110</td>
<td>Branch on Unordered or Less or Equal</td>
<td>U or L or E</td>
</tr>
<tr>
<td>FBO</td>
<td>1111</td>
<td>Branch on Ordered</td>
<td>L or G or E</td>
</tr>
</tbody>
</table>

Format:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>25</th>
<th>24</th>
<th>22</th>
<th>21</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>a</td>
<td>cond.</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
<td>disp22</td>
</tr>
</tbody>
</table>
```

*NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.*
**FCMPd**

**Compare Double**

*(FPU Instruction Only)*

**Operation:**

\[ \text{fcc} \leftarrow f[r1]d \text{ COMPARE } f[r2]d \]

**Assembler Syntax:**

\[ \text{fcmpd } freg_{rs1}, freg_{rs2} \]

**Description:**

FCMPd subtracts the contents of \( f[r2] \) CONCAT \( f[r2+1] \) from the contents of \( f[r1] \) CONCAT \( f[r1+1] \) following the ANSI/IEEE 754-1985 standard. The result is evaluated, the FSR’s fcc bits are set accordingly, and then the result is discarded. The codes are set as follows:

<table>
<thead>
<tr>
<th>fcc</th>
<th>relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>( f[s1] = f[s2] )</td>
</tr>
<tr>
<td>1</td>
<td>( f[s1] &lt; f[s2] )</td>
</tr>
<tr>
<td>2</td>
<td>( f[s1] &gt; f[s2] )</td>
</tr>
<tr>
<td>3</td>
<td>( f[s1] \neq f[s2] ) (unordered)</td>
</tr>
</tbody>
</table>

In this table, \( f[s1] \) stands for the contents of \( f[r1] \), \( f[r1+1] \) and \( f[s2] \) represents the contents of \( f[r2], f[r2+1] \).

Compare instructions are used to set up the floating-point condition codes for a subsequent FBlc instruction. However, to prevent misapplication of the condition codes, at least one non-floating-point instruction must be executed between an FCMPd and a subsequent FBlc instruction.

FCMPd causes an invalid exception (nv) if either operand is a signaling NaN.

**Traps:**

- \text{fp}_\text{disabled}
- \text{fp}_\text{exception} (nv)

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>ignored</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>rs2</td>
</tr>
</tbody>
</table>

MATRA MHS
Rev. A (10/09/96)
FCMPEd Compare Double and Exception if Unordered FCMPEd
(FPU Instruction Only)

Operation: \( fcc \leftarrow f[r1]d \text{ COMPARE } f[r2]d \)

Assembler Syntax: \( \text{fcmped } \text{freg}_{rs1}, \text{freg}_{rs2} \)

Description: FCMPEd subtracts the contents of \( f[r2] \text{ CONCAT } f[r2+1] \) from the contents of \( f[r1] \text{ CONCAT } f[r1+1] \) following the ANSI/IEEE 754-1985 standard. The result is evaluated, the FSR’s \( fcc \) bits are set accordingly, and then the result is discarded. The codes are set as follows:

<table>
<thead>
<tr>
<th>fcc</th>
<th>Relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>( f_{1} = f_{2} )</td>
</tr>
<tr>
<td>1</td>
<td>( f_{1} &lt; f_{2} )</td>
</tr>
<tr>
<td>2</td>
<td>( f_{1} &gt; f_{2} )</td>
</tr>
<tr>
<td>3</td>
<td>( f_{1} \neq f_{2} ) (unordered)</td>
</tr>
</tbody>
</table>

In this table, \( f_{1} \) stands for the contents of \( f[r1] \), \( f[r1+1] \) and \( f_{2} \) represents the contents of \( f[r2], f[r2+1] \).

Compare instructions are used to set up the floating-point condition codes for a subsequent FBfcc instruction. However, to prevent misapplication of the condition codes, at least one non-floating-point instruction must be executed between an FCMP and a subsequent FBfcc instruction.

FCMPEd causes an invalid exception (nv) if either operand is a signaling or quiet NaN.

Traps: fp_disabled, fp_exception (nv)

Format:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td></td>
<td>110101</td>
<td>rs1</td>
<td>001010110</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
FCMPEs  Compare Single and Exception if Unordered FCMPEs
(FPU Instruction Only)

Operation:  \( fcc \leftarrow f[rs1] \) \( \text{COMPARE} \ f[rs2] \)

Assembler Syntax:  \( fcmpes \ freg_{rs1}, freg_{rs2} \)

Description:  FCMPEs subtracts the contents of \( f[rs2] \) from the contents of \( f[rs1] \) following the ANSI/IEEE 754-1985 standard. The result is evaluated, the FSR’s \( fcc \) bits are set accordingly, and then the result is discarded. The codes are set as follows:

<table>
<thead>
<tr>
<th>( fcc )</th>
<th>Relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>( fs1 = fs2 )</td>
</tr>
<tr>
<td>1</td>
<td>( fs1 &lt; fs2 )</td>
</tr>
<tr>
<td>2</td>
<td>( fs1 &gt; fs2 )</td>
</tr>
<tr>
<td>3</td>
<td>( fs1 \neq \text{fs2} ) (unordered)</td>
</tr>
</tbody>
</table>

In this table, \( fs1 \) stands for the contents of \( f[rs1] \) and \( fs2 \) represents the contents of \( f[rs2] \).

Compare instructions are used to set up the floating-point condition codes for a subsequent FBfcc instruction. However, to prevent misapplication of the condition codes, at least one non-floating-point instruction must be executed between an FCMP and a subsequent FBfcc instruction.

FCMPEs causes an invalid exception (nv) if either operand is a signaling or quiet NaN.

Traps:  \( \text{fp\_disabled} \)  
\( \text{fp\_exception (nv)} \)

Format:

\[
\begin{array}{ccccccccc}
1 & 0 & \text{ignored} & 1 & 1 & 0 & 1 & 0 & 1 & rs1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & rs2
\end{array}
\]
FCMPEx

Compare Extended and Exception if Unordered

(FPU Instruction Only)

**Operation:**
\[ \text{fcc} \leftarrow f[\text{rs1}] \text{ COMPARE } f[\text{rs2}] \]

**Assembler Syntax:**
\[ \text{fcmpex } \text{freg}, \text{rs1}, \text{freg}, \text{rs2} \]

**Description:**
FCMPEx subtracts the contents of \( f[\text{rs2}] \) CONCAT \( f[\text{rs2}+1] \) CONCAT \( f[\text{rs2}+2] \) from the contents of \( f[\text{rs1}] \) CONCAT \( f[\text{rs1}+1] \) CONCAT \( f[\text{rs1}+2] \) following the ANSI/IEEE 754-1985 standard. The result is evaluated, the FSR’s \( \text{fcc} \) bits are set accordingly, and then the result is discarded. The codes are set as follows:

<table>
<thead>
<tr>
<th>( \text{fcc} )</th>
<th>Relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>( f[\text{rs1}] = f[\text{rs2}] )</td>
</tr>
<tr>
<td>1</td>
<td>( f[\text{rs1}] &lt; f[\text{rs2}] )</td>
</tr>
<tr>
<td>2</td>
<td>( f[\text{rs1}] &gt; f[\text{rs2}] )</td>
</tr>
<tr>
<td>3</td>
<td>( f[\text{rs1}] \neq f[\text{rs2}] ) (unordered)</td>
</tr>
</tbody>
</table>

In this table, \( f[\text{rs1}] \) stands for the contents of \( f[\text{rs1}], f[\text{rs1}+1], f[\text{rs1}+2] \) and \( f[\text{rs2}] \) represents the contents of \( f[\text{rs2}], f[\text{rs2}+1], f[\text{rs2}+2] \).

Compare instructions are used to set up the floating-point condition codes for a subsequent FBfcc instruction. However, to prevent misapplication of the condition codes, at least one non-floating-point instruction must be executed between an FCMP and a subsequent FBfcc instruction.

FCMPEx causes an invalid exception (nv) if either operand is a signaling or quiet NaN.

**Traps:**
- \( \text{fp_disabled} \)
- \( \text{fp_exception (nv)} \)

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>ignored</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
FCMPs Compare Single FCMPs
(FPU Instruction Only)

Operation:  
\[
\text{fcc} \leftarrow \text{f}[\text{rs1}]: \text{COMPARE} \ f[\text{rs2}]
\]

Assembler Syntax:  
\[
fcmps \ freg_{\text{rs1}}, freg_{\text{rs2}}
\]

Description:  
FCMPs subtracts the contents of f[rs2] from the contents of f[rs1] following the ANSI/IEEE 754-1985 standard. The result is evaluated, the FSR's fcc bits are set accordingly, and then the result is discarded. The codes are set as follows:

<table>
<thead>
<tr>
<th>fcc</th>
<th>Relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>f1 = f2</td>
</tr>
<tr>
<td>1</td>
<td>f1 &lt; f2</td>
</tr>
<tr>
<td>2</td>
<td>f1 &gt; f2</td>
</tr>
<tr>
<td>3</td>
<td>f1 \neq f2 (unordered)</td>
</tr>
</tbody>
</table>

In this table, f1 stands for the contents of f[rs1] and f2 represents the contents of f[rs2].

Compare instructions are used to set up the floating-point condition codes for a subsequent FBfcc instruction. However, to prevent misapplication of the condition codes, at least one non-floating-point instruction must be executed between an FCMP and a subsequent FBfcc instruction.

FCMPs causes an invalid exception (nv) if either operand is a signaling NaN.

Traps:  
- fp_disabled
- fp_exception (nv)

Format:

```
|  31 |  30 |  29 |  28 |  27 |  26 |  25 |  24 |  23 |  22 |  21 |  20 |  19 |  18 |  17 |  16 |  15 |  14 |  13 |  12 |  11 |  10 |  9  |  8  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|  1  |  0  | ignored |  1 |  1 |  0 |  1 |  0 |  1 |  rs1 |  0 |  0 |  1 |  0 |  1 |  0 |  0 |  1 |  rs2 |
```
FCMPx

Compare Extended

(FPU Instruction Only)

Operation:

\[ fc \leftarrow f[r_{s1}]x \text{ COMPARE } f[r_{s2}]x \]

Assembler Syntax:

\[ \text{fcmpx } freg_{rs1}, freg_{rs2} \]

Description:

FCMPx subtracts the contents of \( f[r_{s2}] \) CONCAT \( f[r_{s2}+1] \) CONCAT \( f[r_{s2}+2] \) from the contents of \( f[r_{s1}] \) CONCAT \( f[r_{s1}+1] \) CONCAT \( f[r_{s1}+2] \) following the ANSI/IEEE 754-1985 standard. The result is evaluated, the FSR’s \( fcc \) bits are set accordingly, and then the result is discarded. The codes are set as follows:

<table>
<thead>
<tr>
<th>fcc</th>
<th>Relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1 = s2</td>
</tr>
<tr>
<td>1</td>
<td>1 &lt; s2</td>
</tr>
<tr>
<td>2</td>
<td>1 &gt; s2</td>
</tr>
<tr>
<td>3</td>
<td>1 \neq 2 (unordered)</td>
</tr>
</tbody>
</table>

In this table, \( s1 \) stands for the contents of \( f[r_{s1}], f[r_{s1}+1], f[r_{s1}+2] \) and \( s2 \) represents the contents of \( f[r_{s2}], f[r_{s2}+1], f[r_{s2}+2] \).

Compare instructions are used to set up the floating-point condition codes for a subsequent FBfcc instruction. However, to prevent misapplication of the condition codes, at least one non-floating-point instruction must be executed between an FCMP and a subsequent FBfcc instruction.

FCMPx causes an invalid exception (nv) if either operand is a signaling NaN.

Traps:

fp_disabled
fp_exception (nv)

Format:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>ignored</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
```
FDIVd  Divide Double  FDIVd
(FPU Instruction Only)

Operation:  \( \text{f[rd]d} \leftarrow \frac{\text{f[rs1]d}}{\text{f[rs2]d}} \)

Assembler Syntax:  \text{fdvd } \text{freg}_{rs1}, \text{freg}_{rs2}, \text{freg}_{rd} \)

Description:  The FDIVd instruction divides the contents of \( \text{f[rs1] CONCAT f[rs1+1]} \) by the contents of \( \text{f[rs2 CONCAT f[rs2+1]} \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( \text{f[rd]} \) and \( \text{f[rd+1]} \).

Traps:  \text{fp_disabled}
\text{fp_exception (of, uf, dz, nv, nx)}

Format:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 0  | rd | 1  | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | rs1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | rs2 |
FDIVs

Divide Single

(FPU Instruction Only)

Operation: \( f[rd] \leftarrow f[rs1] / f[rs2] \)

Assembler Syntax: \( \text{fdivs } freg_{rs1}, freg_{rs2}, freg_{rd} \)

Description: The FDIVs instruction divides the contents of \( f[rs1] \) by the contents of \( f[rs2] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd] \).

Traps: \( \text{fp\_disabled} \)
\( \text{fp\_exception (of, uf, dz, nv, nx)} \)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>11</td>
<td>10</td>
<td>0</td>
<td>rs1</td>
<td>00</td>
<td>10</td>
<td>01</td>
<td>11</td>
<td>01</td>
</tr>
</tbody>
</table>

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FDIVx

Divide Extended

(FPU Instruction Only)

Operation: \[
\text{f}[\text{rd}]x \leftarrow \text{f}[\text{rs1}]x / \text{f}[\text{rs2}]x
\]

Assembler Syntax: \[
\text{fdiva } \text{freg}_{rs1}, \text{freg}_{rs2}, \text{freg}_{rd}
\]

Description:
The FDIVx instruction divides the contents of f[rs1] CONCAT f[rs1+1] CONCAT f[rs1+2] by the contents of f[rs2] CONCAT f[rs2+1] CONCAT f[rs2+2] as specified by the ANSI/IEEE 754-1985 standard and places the results in f[rd], f[rd+1], and f[rd+2].

Traps:
fp_disabled
fp_exception (of, uf, dz, nv, nx)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>110100</td>
<td>rs1</td>
<td>00100111</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**FdTOi**

*Convert Double to Integer (FPU Instruction Only)*

**Operation:**

\[ f[rd] \leftarrow f[rs2] \]

**Asmblr Syntax:**

\[ \text{fdtoi } freg_{rs2}, freg_{rd} \]

**Description:**

FdTOi converts the floating-point double contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) to a 32-bit, signed integer by rounding toward zero as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \). The rounding direction field \( (RD) \) of the FSR is ignored.

**Traps:**

fp_disabled
fp_exception (nv, nx)

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>ignored</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
FdTOs  Convert Double to Single  FdTOs
(FPU Instruction Only)

Operation: \( f[rd] \leftarrow f[rs2]d \)

Assembler Syntax: \( fdtos\ freg_{rs2}\ freg_{rd} \)

Description: FdTOs converts the floating-point double contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) to a single-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \). Rounding is performed according to the rounding direction field (RD) of the FSR.

Traps: fp_disabled
fp_exception (of, uf, nv, nx)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
FdTOx  Convert Double to Extended  FdTOx
(FPU Instruction Only)

Operation:  \( f[rd]x \leftarrow f[rs2]d \)

Assembler Syntax:  \( \text{fdtox } freg_{rs2}, freg_{rd} \)

Description:  FdTOx converts the floating-point double contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) to an extended-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \), \( f[rd+1] \), and \( f[rd+2] \). Rounding is performed according to the rounding direction (\( RD \)) and rounding precision (\( RP \)) fields of the FSR.

Traps:  \( \text{fp\_disabled} \)
\( \text{fp\_exception (nv)} \)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>\text{rd}</td>
<td>1 1 0 1 0 0</td>
<td>\text{ignored}</td>
<td>0 1 1 0 0 1 1 0</td>
<td>\text{rs2}</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
FiTOd  Convert Integer to Double
(FPU Instruction Only)

Operation:  \[ f[rd]d \leftarrow f[rs2]i \]

Assembler Syntax:  \[ fitod \ freg_{rs2} , \ freg_{rd} \]

Description:  FiTOd converts the 32-bit, signed integer contents of \( f[rs2] \) to a floating-point, double-precision format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \) and \( f[rd+1] \).

Traps:  \[ \text{fp\_disabled} \]
\[ \text{fp\_exception}^* \]

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>110100</td>
<td>ignored</td>
<td>011001000</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
FiTOs  Convert Integer to Single  FiTOs  
(FPU Instruction Only)

Operation:  \( f[r_{d}] \leftarrow f[r_{s2}]i \)

Assembler Syntax:  \texttt{fitos\_freg}_{rs2}\_freg_{rd} 

Description:  FiTOs converts the 32-bit, signed integer contents of \( f[r_{s2}] \) to a floating-point, single-precision format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[r_{d}] \). Rounding is performed according to the rounding direction field, \( RD \).

Traps:  
- \texttt{fp\_disabled}
- \texttt{fp\_exception (nx)}

Format:

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 28 & 25 & 24 & 19 & 18 & 14 & 13 & 5 & 4 & 0 \\
\hline
1 & 0 & \text{rd} & 110100 & \text{ignored} & 011000100 & \text{rs2} \\
\end{array}
\]
FiTOx Convert Integer to Extended (FPU Instruction Only)

**Operation:**
\[ f[rd]\times \leftarrow f[rs2]\]

**Assembler Syntax:**
`fitox freg, freg, freg`

**Description:** FiTOx converts the 32-bit, signed integer contents of `f[rs2]` to an extended-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in `f[rd]`, `f[rd+1]`, and `f[rd+2]`.

**Traps:**
- `fp_disabled`
- `fp_exception`

**Format:**

|       | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|       | 1  | 0  | rd | 1  | 1  | 0  | 1  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |   |

*NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.*
FMOVs

(FPU Instruction Only)

Operation: \( f[rd] \leftarrow f[rs2] \)

Assembler Syntax: 

\[ \text{fmovs } freg_{rs2}, freg_{rd} \]

Description: The FMOVs instruction moves the word content of register \( f[rs2] \) to the register \( f[rd] \). Multiple FMOVs’ are required to transfer multiple-precision numbers between \( f \) registers.

Traps: 

- \( \text{fp_disabled} \)
- \( \text{fp_exception}^* \)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>11</td>
<td>01</td>
<td>00</td>
<td>ignored</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
FMULd

Multiply Double

(FPU Instruction Only)

Operation:
\[ f[rd]d \leftarrow f[rs1]d \times f[rs2]d \]

Assembler Syntax:
\[ \text{fmuld} freg_{rs1}, freg_{rs2}, freg_{rd} \]

Description:
The FMULd instruction multiplies the contents of \( f[rs1] \) CONCAT \( f[rs1+1] \) by the contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd] \) and \( f[rd+1] \).

Traps:
- \text{fp\_disabled}
- \text{fp\_exception (of, uf, nv, nx)}

Format:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>110100</td>
<td>rs1</td>
<td>001001010</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
FMULs Multiply Single
(FPU Instruction Only)

Operation: \( f[rd] \leftarrow f[rs1] \times f[rs2] \)

Assembler Syntax: `fmuls freg rs1, freg rs2, freg rd`

Description: The FMULs instruction multiplies the contents of \( f[rs1] \) by the contents of \( f[rs2] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd] \).

Traps: `fp_disabled`
`fp_exception (of, uf, nv, nx)`

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
**FMULx** Multiply Extended FMULx (FPU Instruction Only)

**Operation:**  
\[ f[rd] \leftarrow f[rs1] \times f[rs2] \]

**Assembler Syntax:**  
\[ \text{fmulx } freg_{rs1}, freg_{rs2}, freg_{rd} \]

**Description:** The FMULx instruction multiplies the contents of \( f[rs1] \) CONCAT \( f[rs1+1] \) CONCAT \( f[rs1+2] \) by the contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) CONCAT \( f[rs2+2] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd] \), \( f[rd+1] \), and \( f[rd+2] \).

**Traps:**  
- \( \text{fp\_disabled} \)
- \( \text{fp\_exception (of, uf, nv, nx)} \)

**Format:**

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>rs2</td>
</tr>
</tbody>
</table>
```

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FNEGs

Negate FNEGs

(FPU Instruction Only)

Operation:
\[ f[rd] \leftarrow f[rs2] \text{ XOR } 80000000 \text{ H} \]

Assembler Syntax:
\[ \text{fnegs } \text{freg}_{rs2}, \text{freg}_{rd} \]

Description:
The FNEGs instruction complements the sign bit of the word in \( f[rs2] \) and places the result in \( f[rd] \). It does not round.
Since this FPop can address both even and odd \( f \) registers, FNEGs can also operate on the high-order words of double and extended operands, which accomplishes sign bit negation for these data types.

Traps:
\[ \text{fp\_disabled} \]
\[ \text{fp\_exception}^* \]

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>11</td>
<td>0</td>
<td>0</td>
<td>ignored</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\[ \text{NOTE: } \text{An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.} \]
FSQRTd

Square Root Double

(FPU Instruction Only)

Operation:   \( \text{f[rd]d} \leftarrow \text{SQRT f[rs2]d} \)

Assembler Syntax:   \text{fsqtd} \ freg$_{rs2}$, freg$_{rd}$

Description:   FSQRTd generates the square root of the floating-point double contents of \( \text{f[rs2]} \) CONCAT \( \text{f[rs2+1]} \) as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( \text{f[rd]} \) and \( \text{f[rd+1]} \). Rounding is performed according to the rounding direction field (RD) of the FSR.

Traps:   fp_disabled
          fp_exception (nv, nx)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>ignored</td>
<td>0</td>
<td>0</td>
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</tbody>
</table>
FSQRTs

Square Root Single

(FPU Instruction Only)

Operation:
\[ f[rd] \leftarrow \text{SQRT} f[rs2] \]

Assembler Syntax:
\[ \text{fsqrts } freg_{rs2}, freg_{rd} \]

Description:
FSQRTs generates the square root of the floating-point single contents of \( f[rs2] \) as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \). Rounding is performed according to the rounding direction field (RD) of the FSR.

Traps:
f_p\_disabled
f_p\_exception (nv, nx)

Format:

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 5 & 4 & 0 \\
1 & 0 & \text{rd} & 1 & 1 & 0 & 1 & 0 & 0 & \text{ignored} & 0 & 0 & 1 & 0 & 1 & 0 & 1 & \text{rs2} \\
\end{array}
\]
FSQRTx
Square Root Extended
(FPU Instruction Only)

Operation: \( f[rd] \leftarrow \text{SQRT} f[rs2] \)

Assembler Syntax: `fsqrtx freg\_rs2, freg\_rd`

Description: FSQRTx generates the square root of the floating-point extended contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) CONCAT \( f[rs2+2] \) as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \), \( f[rd+1] \), and \( f[rd+2] \). Rounding is performed according to the rounding direction (RD) and rounding precision (RP) fields of the FSR.

Traps:
- \text{fp\_disabled}
- \text{fp\_exception (nv, nx)}

Format:

<p>| | | | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
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</table>

<p>| | | | | | | | | | |</p>
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</tr>
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<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>rs2</td>
</tr>
</tbody>
</table>
**FsTOd**

**Convert Single to Double**

*(FPU Instruction Only)*

**Operation:**

\[ f[rd] \leftarrow f[rs2] \]

**Assembler Syntax:**

`fs
tod \; \textit{freg}_{rs2}, \textit{freg}_{rd}`

**Description:**

FsTOd converts the floating-point single contents of \( f[rs2] \) to a double-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \) and \( f[rd+1] \). Rounding is performed according to the rounding direction field (\( RD \)) of the FSR.

**Traps:**

- `fp_disabled`
- `fp_exception (nv)`

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
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<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
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<th>13</th>
<th>5</th>
<th>4</th>
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</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
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<td>ignored</td>
<td>011001001</td>
<td>rs2</td>
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</tbody>
</table>
 FsTOi
Convert Single to Integer
(FPU Instruction Only)

Operation: \[ f[rd] \leftarrow f[rs2] \]

Assembler Syntax: `fstoi freg.rs2, freg.rd`

Description: FsTOi converts the floating-point single contents of \( f[rs2] \) to a 32-bit, signed integer by rounding toward zero as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \). The rounding field (\( RD \)) of the FSR is ignored.

Traps: `fp_disabled`, `fp_exception` (nv, nx)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
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<th>27</th>
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<th>24</th>
<th>19</th>
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<th>13</th>
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<th>4</th>
<th>0</th>
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<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>100</td>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
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</table>
FsTOx

Convert Single to Extended
(FPU Instruction Only)

**Operation:**
\[ f[r]x \leftarrow f[r2]s \]

**Assembler Syntax:**
\[ fstox \_freg\_rs2, \_freg\_rd \]

**Description:** FsTOx converts the floating-point single contents of \( f[r2] \) to an extended-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \), \( f[rd+1] \), and \( f[rd+2] \). Rounding is performed according to the rounding direction (\( RD \)) and rounding precision (\( RP \)) fields of the FSR.

**Traps:**
- fp_disabled
- fp_exception (nv)

**Format:**

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<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
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<td>rd</td>
<td>11 01 00</td>
<td>ignored</td>
<td>01 10 01 10 1</td>
<td>rs2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Rev. A (10/09/96)
FSUBd \hspace{1cm} \textbf{Subtract Double} \hspace{1cm} \textbf{FSUBd} \\
\quad \text{(FPU Instruction Only)}

\textbf{Operation:} \quad \text{f[rd]d} \leftarrow \text{f[rs1]d} - \text{f[rs2]d}

\textbf{Assembler Syntax:} \quad \text{fsubd \_\_freg\_rs1, \_\_freg\_rs2, \_\_freg\_rd}

\textbf{Description:} \quad \text{The FSUBd instruction subtracts the contents of f[rs2] CONCAT f[rs2+1] from the contents of f[rs1] CONCAT f[rs1+1] as specified by the ANSI/IEEE 754-1985 standard and places the results in f[rd] and f[rd+1].}

\textbf{Traps:} \quad \text{fp\_disabled}
\quad \text{fp\_exception (of, uf, nx, nv)}

\textbf{Format:}

\begin{center}
\begin{tabular}{cccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 \\
1 & 0 & rd & 1 & 1 & 0 & 1 & 0 \\
18 & 17 & 16 & 15 & 14 & 13 & 5 & 4 \\
0 & 0 & 1 & 0 & 0 & 0 & 1 & 1 \\
rs1 & rs2
\end{tabular}
\end{center}
FSUBs Subtract Single FSUBs
(FPU Instruction Only)

Operation: $f[rd] \leftarrow f[rs1] - f[rs2]$

Assembler Syntax: 

<table>
<thead>
<tr>
<th>rd</th>
<th>rs1</th>
<th>rs2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Description: The FSUBs instruction subtracts the contents of $f[rs2]$ from the contents of $f[rs1]$ as specified by the ANSI/IEEE 754-1985 standard and places the results in $f[rd]$.

Traps: 

- fp_disabled
- fp_exception (of, uf, nx, nv)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
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<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>11</td>
<td>00</td>
<td>00</td>
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<td></td>
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|   |    |    |    |    |    |    |    |    |    |    |    |

<table>
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<th>00</th>
<th>10</th>
<th>1</th>
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<tbody>
<tr>
<td>rs1</td>
<td></td>
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</tr>
</tbody>
</table>

Rev. A (10/09/96)
FSUBx Subtract Extended
(FPU Instruction Only)

Operation: \[ f[rd]x \leftarrow f[rs1]x - f[rs2]x \]

Assembler Syntax: \( fsubx \ freg_{rs1}, \ freg_{rs2}, \ freg_{rd} \)

Description: The FSUBx instruction subtracts the contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) CONCAT \( f[rs2+2] \) from the contents of \( f[rs1] \) CONCAT \( f[rs1+1] \) CONCAT \( f[rs1+2] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd] \), \( f[rd+1] \), and \( f[rd+2] \).

Traps: \( fp\\_disabled \)
\( fp\_exception\) (of, uf, nv, nx)

Format:

```
    31 30 29 28 25 24 19 18 14 13 5 4 0
  1 0  rd  1 1 0 1 0 0  rs1  0 0 1 0 0 0 1 1 1  rs2
```
FxTOd  Convert Extended to Double
(FPU Instruction Only)

Operation:  \( f[rd] \leftarrow f[rs2]x \)

Assembler Syntax:  fxtod \( freg_{rs2}, freg_{rd} \)

Description:  FxTOd converts the floating-point extended contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) CONCAT \( f[rs2+2] \) to a double-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \) and \( f[rd+1] \). Rounding is performed according to the rounding direction (\( RD \)) field of the FSR.

Traps:  fp_disabled
fp_exception (of, uf, nv, nx)

Format:

<table>
<thead>
<tr>
<th>31</th>
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<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>110100</td>
<td>ignored</td>
<td>011001011</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>
FxTOi Convert Extended to Integer
(FPU Instruction Only)

Operation: \( f[rd] \leftarrow f[rs2] \times \)

Assembler Syntax: `fxtoi fregrs2, fregrd`

Description: FxTOi converts the floating-point extended contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) CONCAT \( f[rs2+2] \) to a 32-bit, signed integer by rounding toward zero as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \). The rounding field (RD) of the FSR is ignored.

Traps: `fp_disabled`
        `fp_exception (nv, nx)`

Format:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 0  | rd | 1  | 1  | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
FxTOs

Convert Extended to Single
(FPU Instruction Only)

Operation: \( f[rd] \leftarrow f[rs2] \times \)

Assembler Syntax: `fxtos freg, freg`

Description: FxTOs converts the floating-point extended contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) CONCAT \( f[rs2+2] \) to a single-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \). Rounding is performed according to the rounding direction \( RD \) field of the FSR.

Traps: fp_disabled
fp_exception (of, uf, nv, nx)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
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<th>18</th>
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<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>110100</td>
<td>ignored</td>
<td>01100011</td>
<td>rs2</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>
IFLUSH Instruction Cache Flush

Operation: \( \text{FLUSH} \leftarrow [r[rs1] + (r[rs2] \text{ or sign extnd(simm13))}] \)

Assembler Syntax: iflush address

Description: The IFLUSH instruction causes a word to be flushed from an instruction cache which may be internal to the processor. The word to be flushed is at the address specified by the contents of \( r[rs1] \) plus either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate op-erand contained in the instruction if \( i \) equals one.

Since there is no internal instruction cache in the current CY7C600 family, the result of executing an IFLUSH instruction is dependent on the state of the input signal, Instruction Cache Flush Trap (IFT). If \( IFT = 1 \), IFLUSH executes as a NOP, with no side effects. If \( IFT = 0 \), execution of IFLUSH causes an illegal_instruction trap.

Traps: illegal_instruction

Format:

<table>
<thead>
<tr>
<th>Bit</th>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
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<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>ignored</td>
<td>1</td>
<td>1</td>
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<td>1</td>
<td>i=0</td>
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<td>rs1</td>
<td>rs2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>31</th>
<th>30</th>
<th>29</th>
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</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td>0</td>
<td>ignored</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>i=1</td>
<td>simm13</td>
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<td></td>
</tr>
</tbody>
</table>
**JMPL**

**Jump and Link**

**JMPL**

**Operation:**

\[
\begin{align*}
    r[rd] &\rightarrow PC \\
    \text{PC} &\rightarrow \text{nPC} \\
    \text{nPC} &\rightarrow r[rs1] + (r[rs2] \text{ or sign extnd(simm13)})
\end{align*}
\]

**Assembler Syntax:**

\[
jmpl \ address, \ reg\ rd
\]

**Description:**

JMPL first provides linkage by saving its return address into the register specified in the \textit{rd} field. It then causes a register-indirect, delayed control transfer to an address specified by the sum of the contents of \textit{r[rs1]} and either the contents of \textit{r[rs2]} if the instruction’s \textit{i} bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \textit{i} equals one.

If either of the low-order two bits of the jump address is nonzero, a memory_address_not_aligned trap is generated.

**Programming note:** A register-indirect CALL can be constructed using a JMPL instruction with \textit{rd} set to 15. JMPL can also be used to return from a CALL. In this case, \textit{rd} is set to 0 and the return (jump) address would be equal to \textit{r[31] + 8}.

**Traps:**

memory_address_not_aligned

**Format:**

<table>
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<tr>
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<th>Bit 30</th>
<th>Bit 29</th>
<th>Bit 28</th>
<th>Bit 27</th>
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<th>Bit 14</th>
<th>Bit 13</th>
<th>Bit 12</th>
<th>Bit 5</th>
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<tr>
<td>\textit{i=0}</td>
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</tr>
<tr>
<td>\textit{rs1}</td>
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<td>\textit{rs2}</td>
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<table>
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<th>Bit 29</th>
<th>Bit 28</th>
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<th>Bit 14</th>
<th>Bit 13</th>
<th>Bit 12</th>
<th>Bit 5</th>
<th>Bit 4</th>
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<tr>
<td>\textit{i=1}</td>
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</tbody>
</table>
LD Load Word

Operation: \( r[rd] \leftarrow [r[rs1] + (r[rs2] \text{ or sign extnd(simm13))] \)

Assembler Syntax: `ld [address], reg_rd`

Description: The LD instruction moves a word from memory into the destination register, \( r[rd] \). The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one.

If LD takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s \( r[rd] \) register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem.

*Programming note:* If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps: memory_address_not_aligned
data_access_exception

Format:

```
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<thead>
<tr>
<th></th>
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<td>rd</td>
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<td>=0</td>
<td>ignored</td>
<td></td>
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```

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<td>=1</td>
<td>simm13</td>
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</tbody>
</table>
```
LDA

Load Word from Alternate space

(Privileged Instruction)

Operation: address space ← asi
r[rd] ← [r[rs1] + r[rs2]]

Assembler Syntax: lda [regaddr] asi, reg rd

Description: The LDA instruction moves a word from memory into the destination register, r[rd]. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of r[rs1] and r[rs2].

If LDA takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load's r[rd] register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem.

Traps: illegal_instruction (if i=1)
privileged_instruction (if S=0)
memory_address_not_aligned
data_access_exception

Format:

<table>
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<tr>
<th>31</th>
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<td>1</td>
<td>rd</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>rs1</td>
<td>i=0</td>
<td>asi</td>
<td>rs2</td>
<td></td>
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</tbody>
</table>
**LDC**

**Load Coprocessor register**

**Operation:**

c[rd] ← [r[rs1] + (r[rs2] or sign extnd(simm13))]

**Assembler Syntax:**

ld [address], creg rd

**Description:**

The LDC instruction moves a word from memory into a coprocessor register, c[rd]. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one.

If the PSR’s EC bit is set to zero or if no coprocessor is present, a cp_disabled trap will be generated. If LDC takes a trap, the state of the coprocessor depends on the particular implementation.

If the instruction following a coprocessor load uses the load’s c[rd] register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem.

*Programming note:* If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

**Traps:**

cp_disabled

memory_address_not_aligned

data_access_exception

**Format:**

```
<table>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
</tr>
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</table>
```

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<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>i=1</td>
<td>simm13</td>
</tr>
</tbody>
</table>
```
**Operation:** CSR ← [r[rs1] + (r[rs2] or sign extnd(simm13))]

**Assembler Syntax:**

```
ld [address], %csr
```

**Description:**
The LDCSR instruction moves a word from memory into the Coprocessor State Register. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one.

If the PSR’s EC bit is set to zero or if no coprocessor is present, a cp_disabled trap will be generated. If LDCSR takes a trap, the state of the coprocessor depends on the particular implementation.

If the instruction following a LDCSR uses the CSR as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon implementation of the coprocessor.

*Programming note:* If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

**Traps:**
- cp_disabled
- cp_exception
- memory_address_not_aligned
- data_access_exception

**Format:**

```
    31  30  29  25  24  19  18  14  13  12     5  4  0
 1 1    rd  1 1 0 0 0 1  rs1  i=0  ignored   rs2

    31  30  29  25  24  19  18  14  13  12     0
 1 1    rd  1 1 0 0 0 1  rs1  i=1        simm13
```
LDD Load Doubleword

Operation:
\[ \text{r[rd]} \leftarrow [\text{r[rs1]} + (\text{r[rs2]} \text{ or sign extnd(simm13))}] \]
\[ \text{r[rd + 1]} \leftarrow [(\text{r[rs1]} + (\text{r[rs2]} \text{ or sign extnd(simm13))}) + 4] \]

Assembler Syntax:
\text{ldd [address], regrd}

Description:
The LDD instruction moves a doubleword from memory into a destination register pair, r[rd] and r[rd+1]. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one. The most significant memory word is always moved into the even-numbered destination register and the least significant memory word is always moved into the next odd-numbered register (see discussion in Section NO TAG).

If a data_access_exception trap takes place during the effective address memory access, the destination registers remain unchanged.

If the instruction following an integer load uses the load’s r[rd] register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem. For an LDD, this applies to both destination registers.

Programming note: If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps:
- memory_address_not_aligned
- data_access_exception

Format:

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</tr>
</thead>
<tbody>
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<td>1</td>
<td>rd</td>
<td>0 0 0 0 1 1</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
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<td></td>
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<tr>
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<td>1</td>
<td>rd</td>
<td>0 0 0 0 1 1</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
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</tbody>
</table>
```
LDDA (Privileged Instruction)

Operation:
- Address space $\leftrightarrow$ asi
- $r[rd] \leftarrow r[rs1] + r[rs2]$
- $r[rd+1] \leftarrow r[rs1] + r[rs2] + 4$

Assembler Syntax:
- `ldda [regaddr] asi, reg rd`

Description:
The LDDA instruction moves a doubleword from memory into the destination registers, $r[rd]$ and $r[rd+1]$. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of $r[rs1]$ and $r[rs2]$. The most significant memory word is always moved into the even-numbered destination register and the least significant memory word is always moved into the next odd-numbered register (see discussion in Section NO TAG).

If a trap takes place during the effective address memory access, the destination registers remain unchanged.

If the instruction following an integer load uses the load’s $r[rd]$ register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem. For an LDDA, this applies to both destination registers.

Traps:
- illegal_instruction (if $i=1$)
- privileged_instruction (if $S=0$)
- memory_address_not_aligned
- data_access_exception

Format:

```
<table>
<thead>
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<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>j=0</td>
<td>asi</td>
<td></td>
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</tr>
</tbody>
</table>
```

MATRA MHS
Rev. A (10/09/96)
LDDC Load Doubleword Coprocessor

**Operation:**
\[
\begin{align*}
\text{c}[rd] &\leftarrow [\text{r}[\text{rs1}]+(\text{r}[\text{rs2}] \text{ or sign extnd(simm13)])] \\
\text{c}[rd+1] &\leftarrow [(\text{r}[\text{rs1}]+(\text{r}[\text{rs2}] \text{ or sign extnd(simm13)])+4]
\end{align*}
\]

**Asmblwr Syntax:**
\[
\text{ldd [address], creg rd}
\]

**Description:**
The LDDC instruction moves a doubleword from memory into the coprocessor registers, c[rd] and c[rd+1]. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one. The most significant memory word is always moved into the even-numbered destination register and the least significant memory word is always moved into the next odd-numbered register (see discussion in Section NO TAG).

If the PSR’s EC bit is set to zero or if no coprocessor is present, a cp_disabled trap will be generated. If LDDC takes a trap, the state of the coprocessor depends on the particular implementation.

If the instruction following a coprocessor load uses the load’s c[rd] register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem and coprocessor implementation. For an LDDC, this applies to both destination registers.

**Programming note:** If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

**Traps:**
cp_disabled

**cp_exception**

memory_address_not_aligned
data_access_exception

**Format:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 1  | rd | 1  | 1  | 0 | 0 | 1 | 1 | rs1| i=0| ignored| rs2|
| 1  | 1  | rd | 1  | 1  | 0 | 0 | 1 | 1 | rs1| i=1| simm13|
LDDF: Load Doubleword Floating-Point

Operation:
\[ f[rd] \leftarrow [(r[rs1] + (r[rs2] or sign extnd(simm13))] \]
\[ f[rd + 1] \leftarrow [(r[rs1] + (r[rs2] or sign extnd(simm13))) + 4] \]

Assembler Syntax:
\texttt{ldd [address],freg\_rd}

Description:
The LDDF instruction moves a doubleword from memory into the floating-point registers, \( f[rd] \) and \( f[rd+1] \). The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. The most significant memory word is always moved into the even-numbered destination register and the least significant memory word is always moved into the next odd-numbered register (see discussion in Section NO TAG).

If the PSR’s EF bit is set to zero or if no floating-point unit is present, an \texttt{fp\_disabled} trap will be generated. If a trap takes place during the effective address memory access, the destination registers remain unchanged.

If the instruction following a floating-point load uses the load’s \( f[rd] \) register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem. For an LDDF, this applies to both destination registers.

*Programming note*: If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps:
- \texttt{fp\_disabled}
- \texttt{fp\_exception*}
- \texttt{memory\_address\_not\_aligned}
- \texttt{data\_access\_exception}

Format:

\[
\begin{array}{ccccccccc}
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 1 & rd & 1 & 0 & 0 & 0 & 1 & 1 & rs1 & i=0 & ignored & rs2 \\
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 0 \\
1 & 1 & rd & 1 & 0 & 0 & 0 & 1 & 1 & rs1 & i=1 & simm13 \\
\end{array}
\]

*NOTE*: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
LDF Load Floating-Point register

Operation: \[ f[rd] \leftarrow [r[rs1] + (r[rs2] \text{ or sign extnd(simm13))] \]

Assembler Syntax: \[ \text{ld } \text{[address]} \text{, freg}_rd \]

Description: The LDF instruction moves a word from memory into a floating-point register, \( f[rd] \). The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one.

If the PSR’s EF bit is set to zero or if no Floating-Point Unit is present, an \( \text{fp_disabled} \) trap will be generated. If LDF takes a trap, the contents of the destination register remain unchanged.

If the instruction following a floating-point load uses the load’s \( f[rd] \) register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem.

Programming note: If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps: \( \text{fp_disabled} \)
\( \text{fp_exception}^* \)
\( \text{memory_address_not_aligned} \)
\( \text{data_access_exception} \)

Format:

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 1 & \text{rd} & 1 & 0 & 0 & 0 & 0 & \text{rs1} & i=0 & \text{ignored} & \text{rs2} \\
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 0 \\
1 & 1 & \text{rd} & 1 & 0 & 0 & 0 & 0 & \text{rs1} & i=1 & \text{simm13} \\
\end{array}
\]

* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
LDFSR

Load Floating-Point State Register

Operation:  \[ \text{FSR} \leftarrow [r[\text{rs1}] + (r[\text{rs2}] \text{ or sign extnd(simm13)])] \]

Assembler Syntax:  \( \text{ld [address], %fsr} \)

Description: The LDFSR instruction moves a word from memory into the floating-point state register. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one. This instruction will wait for all pending FPops to complete execution before it loads the memory word into the FSR.

If the PSR’s EF bit is set to zero or if no floating-point unit is present, an fp_disabled trap will be generated. If LDFSR takes a trap, the contents of the FSR remain unchanged.

If the instruction following a LDFSR uses the FSR as a source operand, hardware interlocks add one or more cycle delay to the following instruction depending upon the memory subsystem.

Programming note: If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps: fp_disabled

fp_exception*

memory_address_not_aligned

data_access_exception

Format:

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<td>i=0</td>
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<td>i=1</td>
<td>simm13</td>
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* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
**LDSB**  
**Load Signed Byte**  

**Operation:**  
\[ r[rd] \leftarrow \text{sign extnd}[r[rs1] + (r[rs2] \text{ or sign extnd(sim13))}] \]

**Assembler Syntax:**  
`ldsb [address], reg_rd`

**Description:**  
The **LDSB** instruction moves a signed byte from memory into the destination register, \( r[rd] \). The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. The fetched byte is right-justified and sign-extended in \( r[rd] \).

If **LDSB** takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s \( r[rd] \) register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem.

**Programming note:** If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

**Traps:**  
data_access_exception

**Format:**

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LDSBA
Load Signed Byte from Alternate space (Privileged Instruction)

Operation:
address space ← asi
r[rd] ← sign extnd[r[rs1] + r[rs2]]

Assembler Syntax:
ldsba [regaddr] asi, reg rd

Description:
The LDSBA instruction moves a signed byte from memory into the destination register, r[rd]. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of r[rs1] and r[rs2]. The fetched byte is right-justified and sign-extended in r[rd].

If LDSBA takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s r[rd] register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

Traps:
illegal_instruction (if i=1)
privileged_instruction (if S=0)
data_access_exception

Format:

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<td>0</td>
<td>1</td>
<td>rs1</td>
<td>i=0</td>
<td>asi</td>
<td>rs2</td>
</tr>
</tbody>
</table>
**LDSH**  
Load Signed Halfword  

**Operation:**  
\[ r[rd] \leftarrow \text{sign extnd}[r[rs1] + (r[rs2] \text{ or sign extnd}(\text{simm13})]] \]

**Assembler Syntax:**  
ldsh \ [address] , reg,rd

**Description:**  
The LDSH instruction moves a signed halfword from memory into the destination register, r[rd]. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction's \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. The fetched halfword is right-justified and sign-extended in r[rd]. If LDSH takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s r[rd] register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.  

*Programming note:* If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

**Traps:**  
memory_address_not_aligned  
data_access_exception

**Format:**

```
  31  30  29  25  24  19  18  14  13  12  5  4  0
  1  1  rd  0 0  1  0  1  0  rs1  i=0  ignored  rs2
```

```
  31  30  29  25  24  19  18  14  13  12  0
  1  1  rd  0 0  1  0  1  0  rs1  i=1  simm13
```
LDSA 

Load Signed Halfword from Alternate space 

(Privileged Instruction)

Operation:
address space ← asi
r[rd] ← sign extnd[r[rs1] + r[rs2]]

Assembler Syntax:
ldsha [reg addr] asi, reg rd

Description:
The LDSHA instruction moves a signed halfword from memory into the destination register, r[rd]. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of r[rs1] and r[rs2]. The fetched halfword is right-justified and sign-extended in r[rd].

If LDSHA takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s r[rd] register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

Traps:
- illegal_instruction (if i=1)
- privileged_instruction (if S=0)
- memory_address_not_aligned
- data_access_exception

Format:

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<td>1</td>
<td>0</td>
<td>1</td>
<td>i=0</td>
<td>asi</td>
<td>rs2</td>
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</tbody>
</table>
**LDSTUB**

**Atomic Load/Store Unsigned Byte**

**LDSTUB**

**Operation:**

\[
\text{r[rd]} \leftarrow \text{zero extnd}[\text{r[rs1]} + (\text{r[rs2]} \text{ or sign extnd(simm13)})]
\]

\[
(\text{r[rs1]} + (\text{r[rs2]} \text{ or sign extnd(simm13)})) \leftarrow \text{FFFFFFFF H}
\]

**Assembler Syntax:**

\[
\text{ldstub } [\text{address}], \text{ reg rd}
\]

**Description:**

The LDSTUB instruction moves an unsigned byte from memory into the destination register, r[rd], and rewrites the same byte in memory to all ones, while preventing asynchronous trap interruptions.

In a multiprocessor system, two or more processors executing atomic load/store instructions which address the same byte simultaneously are guaranteed to execute them serially, in some order.

The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction's i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one. The fetched byte is right-justified and zero-extended in r[rd].

If the instruction following an integer load uses the load's r[rd] register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

If LDSTUB takes a trap, the contents of the memory address remain unchanged.

Programming note: If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

**Traps:**

_data_access_exception_

**Format:**

```
  31  30  29  25  24  19  18  14  13  12  5  4  0
  1  1  rd  0 0 1 1 0 1  rs1  i=0  ignored  rs2

  31  30  29  25  24  19  18  14  13  12  0
  1  1  rd  0 0 1 1 0 1  rs1  i=1  simm13
```
LDSTUBA Atomic Load/Store Unsigned Byte in Alternate space

(Privileged Instruction)

Operation: 
address space ← asi 
r[rd] ← zero extnd[rs1 + r[rs2]] 
[r[rs1] + r[rs2]] ← FFFFFFFF H

Assembler Syntax: 
ldstub a [reg addr] asi, reg rd

Description: 
The LDSTUBA instruction moves an unsigned byte from memory into the destination register, r[rd], and rewrites the same byte in memory to all ones, while preventing asynchronous trap interruptions.

In a multiprocessor system, two or more processors executing atomic load/store instructions which address the same byte simultaneously are guaranteed to execute them in some serial order.

The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of r[rs1] and r[rs2]. The fetched byte is right-justified and zero-extended in r[rd].

If the instruction following an integer load uses the load’s r[rd] register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

If LDSTUBA takes a trap, the contents of the memory address remain unchanged.

Traps: 
illegal_instruction (if i=1)
privileged_instruction (if S=0)
data_access_exception

Format:

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MATRA MHS
Rev. A (10/09/96)
LDUB Load Unsigned Byte

Operation: \[ r[rd] \leftarrow \text{zero extnd}[r[rs1] + (r[rs2] \text{ or sign extnd}(\text{simm13})]] \]

Assembler Syntax: \text{ldub \{address\}, regrd}

Description: The LDUB instruction moves an unsigned byte from memory into the destination register, r[rd]. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. The fetched byte is right-justified and zero-extended in r[rd]. If LDUB takes a trap, the contents of the destination register remain unchanged. If the instruction following an integer load uses the load’s r[rd] register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

Programming note: If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps: data_access_exception

Format:

```
 31 30 29 25 24 19 18 14 13 12  5 4  0
 1 1  rd  0 0 0 0 0 1  rs1  \( i=0 \) ignored  rs2
```

```
 31 30 29 25 24 19 18 14 13 12  0
 1 1  rd  0 0 0 0 0 1  rs1  \( i=1 \) simm13
```
**LDUBA**  
Load Unsigned Byte from Alternate space  
_(Privileged Instruction)_

**Operation:**

\[
\text{address space} \leftrightarrow \text{asi} \\
\text{r}[\text{rd}] \leftarrow \text{zero extnd}[\text{r}[\text{rs1}] + \text{r}[\text{rs2}]]
\]

**Assembler Syntax:**

\[
\text{lduba} \ [\text{reg addr}] \text{asi}, \text{reg rd}
\]

**Description:**

The LDUBA instruction moves an unsigned byte from memory into the destination register, \(\text{r}[\text{rd}]\). The effective memory address is a combination of the address space value given in the \(\text{asi}\) field and the address derived by summing the contents of \(\text{r}[\text{rs1}]\) and \(\text{r}[\text{rs2}]\). The fetched byte is right-justified and zero-extended in \(\text{r}[\text{rd}]\).

If LDUBA takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s \(\text{r}[\text{rd}]\) register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

**Traps:**

- illegal_instruction (if \(i=1\))
- privileged_instruction (if \(S=0\))
- data_access_exception

**Format:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 1  |   | rd | 0 | 1 | 0 | 0 | 0 | 1 | rs1 |  | i=0 |   | asi |   |    |   | rs2 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
**LDUH**

**Operation:**

\[ r[rd] \leftarrow \text{zero extnd}[r[rs1] + (r[rs2] \text{ or sign extnd(simm13))}] \]

**Assembler Syntax:**

`lduh [address], reg rd`

**Description:**

The LDUH instruction moves an unsigned halfword from memory into the destination register, \( r[rd] \). The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. The fetched halfword is right-justified and zero-extended in \( r[rd] \).

If LDUH takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s \( r[rd] \) register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

*Programming note:* If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

**Traps:**

- memory_address_not_aligned
- data_access_exception

**Format:**

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- \( rd \)
- \( rs1 \)
- \( i=0 \)
- \( ignored \)
- \( rs2 \)
- \( 0 \)
- \( simm13 \)
**LDUHA** **Load Unsigned Halfword from Alternate space**

*(Privileged Instruction)*

**Operation:**

\[ \text{address space} \leftarrow \text{asi} \]
\[ r[rd] \leftarrow \text{zero extnd}[r[rs1] + r[rs2]] \]

**Assembler Syntax:**

```
lduha [regaddr] asi, reg rd
```

**Description:**

The LDUHA instruction moves an unsigned halfword from memory into the destination register, \( r[rd] \). The effective memory address is a combination of the address space value given in the \( \text{asi} \) field and the address derived by summing the contents of \( r[rs1] \) and \( r[rs2] \). The fetched halfword is right-justified and zero-extended in \( r[rd] \).

If LDUHA takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s \( r[rd] \) register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

**Traps:**

- illegal_instruction (if \( i=1 \))
- privileged_instruction (if \( S=0 \))
- memory_address_not_aligned
- data_access_exception

**Format:**

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**Definitions:**

- asi: Address space
- rs1, rs2: Source registers
- rd: Destination register
- i: Illegal instruction flag
- S: Privileged instruction flag
**MULScc**

**Multiply Step and modify icc**

**Operation:**

\[ \text{op1} = (n \oplus v) \text{ CONCAT } r[rs1]<31:1> \]

if \( Y<0> = 0 \)

\[ \text{op2} = 0 \]

else \( \text{op2} = r[rs2] \) or sign extnd(simm13)

\[ r[rd] = \text{op1} + \text{op2} \]

\[ Y = r[rs1]<0> \text{ CONCAT } Y<31:1> \]

\[ n = r[rd]<31> \]

\[ z = \text{if} [r[rd]]=0 \text{ then } 1, \text{ else } 0 \]

\[ v = ((\text{op1}<31> \text{ AND } \text{op2}<31> \text{ AND } \neg r[rd]<31>) \]

\[ \text{OR (not } \text{op1}<31> \text{ AND not } \text{op2}<31> \text{ AND } r[rd]<31>) \]

\[ c = ((\text{op1}<31> \text{ AND } \text{op2}<31>) \]

\[ \text{OR (not } r[rd] \text{ AND (op1}<31> \text{ OR op2}<31>) \) \]

**Assembler Syntax:**

`mulcc reg, reg_or_imm, reg`  

**Description:**

The multiply step instruction can be used to generate the 64-bit product of two signed or unsigned words. MULScc works as follows:

1. The “incoming partial product” in \( r[rs1] \) is shifted right by one bit and the high-order bit is replaced by the sign of the previous partial product (\( n \oplus v \)). This is operand1.
2. If the least significant bit of the multiplier in the \( Y \) register equals zero, then operand2 is set to zero. If the LSB of the \( Y \) register equal one, then operand2 becomes the multiplicand, which is either the contents of \( r[rs2] \) if the instruction \( i \) field is zero, or sign extnd(simm13) if the \( i \) field is one. Operand2 is then added to operand1 and stored in \( r[rd] \) (the outgoing partial product).
3. The multiplier in the \( Y \) register is then shifted right by one bit and its high-order bit is replaced by the least significant bit of the incoming partial product in \( r[rs1] \).
4. The PSR’s integer condition codes are updated according to the addition performed in step 2.

**Traps:** none

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\( i=0 \) ignored \( rs2 \)

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<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\( i=1 \) \( \text{simmm13} \)
**Operation:**
\[ r[rd] \leftarrow r[rs1] \text{ OR } (r[rs2] \text{ or sign extnd(simm13))} \]

**Assembler Syntax:**
\[ \text{or reg}_{rs1}, \text{ reg}_{or}_{imm}, \text{ reg}_{rd} \]

**Description:**
This instruction does a bitwise logical OR of the contents of register \( r[rs1] \) with either the contents of \( r[rs2] \) (if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \( i=1 \)). The result is stored in register \( r[rd] \).

**Traps:**
None

**Format:**

```
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

```
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

```
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

```
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```
**ORcc**  Inclusive-Or and modify icc

**ORcc**

**Operation:**

\[
\begin{align*}
    r[rd] &\leftarrow r[rs1] \text{ OR } (r[rs2] \text{ or sign extnd(simm13)}) \\
    n &\leftarrow r[rd]<31> \\
    z &\leftarrow \text{if } r[rd]=0 \text{ then 1, else 0} \\
    v &\leftarrow 0 \\
    c &\leftarrow 0
\end{align*}
\]

**Assembler Syntax:**

\[\text{orcc } \text{reg}_{rs1}, \text{ reg}_{or\text{-}imm}, \text{ reg}_{rd}\]

**Description:**

This instruction does a bitwise logical OR of the contents of register \(r[rs1]\) with either the contents of \(r[rs2]\) (if bit field \(i=0\)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \(i=1\)). The result is stored in register \(r[rd]\). ORcc also modifies all the integer condition codes in the manner described above.

**Traps:**

none

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
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<th>25</th>
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<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0 1 0 0 1 0</td>
<td>rs1</td>
<td>(i=0)</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
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<th>31</th>
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</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0 1 0 0 1 0</td>
<td>rs1</td>
<td>(i=1)</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**ORN**

**Inclusive-Or Not**

**Operation:**
\[ r[rd] \leftarrow r[rs1] \text{ OR not(operand2), where } \text{operand2} = (r[rs2] \text{ or sign extnd(simm13)}) \]

**Assembler Syntax:**
\[ \text{orn } r_{rs1}, \text{ reg_or_imm, reg}_rd \]

**Description:**
This instruction does a bitwise logical OR of the contents of register \( r[rs1] \) with the one’s complement of either the contents of \( r[rs2] \) (if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \( i=1 \)). The result is stored in register \( r[rd] \).

**Traps:**
none

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
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<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>( rd )</td>
<td>0 0 0 1 1 0</td>
<td>( rs1 )</td>
<td>( i=0 )</td>
<td>ignored</td>
<td>( rs2 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
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<th>29</th>
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<th>14</th>
<th>13</th>
<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>( rd )</td>
<td>0 0 0 1 1 0</td>
<td>( rs1 )</td>
<td>( i=1 )</td>
<td>( \text{simm13} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**ORNcc**  
Inclusive-Or Not and modify icc

**Operation:**

\[
\begin{align*}
    r[rd] &\leftarrow r[rs1] \text{ OR not(operand2)}, \text{ where } \text{operand2} = (r[rs2] \text{ or sign extnd(simm13)}) \\
    n &\leftarrow r[rd]<31> \\
    z &\leftarrow \text{if } [r[rd]]=0 \text{ then 1, else 0} \\
    v &\leftarrow 0 \\
    c &\leftarrow 0
\end{align*}
\]

**Assembler Syntax:**

\[\text{orncc } reg_{rs1}, \text{ reg_or_imm, reg}_{rd}\]

**Description:**

This instruction does a bitwise logical OR of the contents of register \(r[rs1]\) with the one’s complement of either the contents of \(r[rs2]\) (if bit field \(i=0\)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \(i=1\)). The result is stored in register \(r[rd]\). ORNcc also modifies all the integer condition codes in the manner described above.

**Traps:**

none

**Format:**

<table>
<thead>
<tr>
<th>31</th>
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<th>18</th>
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<th>12</th>
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<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
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<th>14</th>
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<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>ignored</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
RDPSR Read Processor State Register
(Privileged Instruction)

Operation:  \( r[rd] \leftarrow \text{PSR} \)

Assembler Syntax:  \( rd \ %\text{psr}, \ reg_{rd} \)

Description:  RDPSR copies the contents of the PSR into the register specified by the \( rd \) field.

Traps:  privileged-instruction (if S=0)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
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<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>101001</td>
<td></td>
<td></td>
<td></td>
<td>ignored</td>
</tr>
</tbody>
</table>
RDTBR
Read Trap Base Register
(Privileged Instruction)

Operation:  \( r[rd] \leftarrow TBR \)

Assembler Syntax:  \( rd \%tbr, reg_{rd} \)

Description:  RDTBR copies the contents of the TBR into the register specified by the \( rd \) field.

Traps:  privileged_instruction (if \( S=0 \))

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>ignored</td>
</tr>
</tbody>
</table>
RDWIM

Read Window Invalid Mask register

(Privileged Instruction)

Operation: \( r[d] \leftarrow WIM \)

Assembler Syntax: \( rd \ %\text{wim}, \ reg_{rd} \)

Description: RDWIM copies the contents of the WIM register into the register specified by the \( rd \) field.

Traps: privileged_instruction (if S=0)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

ignored
RDY

Read Y register

Operation: \( r[r_{rd}] \leftarrow Y \)

Assembler Syntax: \( \text{rd} \ %y, \ reg_{rd} \)

Description: RDY copies the contents of the Y register into the register specified by the \( rd \) field.

Traps: none

Format:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|  1  |  0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | rd |    |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 101000 | ignored |
RESTORE

Restore caller’s window

Operation:
\[ \text{ncwp} \leftarrow \text{CWP} + 1 \]
\[ \text{result} \leftarrow r[\text{rs1}] + (r[\text{rs2}] \text{ or sign extnd(simm13)}) \]
\[ \text{CWP} \leftarrow \text{ncwp} \]
\[ r[\text{rd}] \leftarrow \text{result} \]

RESTORE does not affect condition codes

Assembler Syntax:
\text{restore reg}_{\text{rs1}}, \text{reg}_{\text{or}_-\text{imm}}, \text{reg}_{\text{rd}}

Description:
RESTORE adds one to the Current Window Pointer (modulo the number of implemented windows) and compares this value against the Window Invalid Mask register. If the new window number corresponds to an invalidated window (WIM AND 2^{\text{ncwp}} = 1), a window_underflow trap is generated. If the new window number is not invalid (i.e., its corresponding WIM bit is reset), then the contents of \( r[\text{rs1}] \) is added to either the contents of \( r[\text{rs2}] \) (field bit \( i = 1 \)) or to the 13-bit, sign-extended immediate value contained in the instruction (field bit \( i = 0 \)). Because the CWP has not been updated yet, \( r[\text{rs1}] \) and \( r[\text{rs2}] \) are read from the currently addressed window (the called window).

The new CWP value is written into the PSR, causing the previous window (the caller’s window) to become the active window. The result of the addition is now written into the \( r[\text{rd}] \) register of the restored window.

Note that arithmetic operations involving the CWP are always done modulo the number of implemented windows (8 for the CY7C601).

Traps:
window_underflow

Format:

- \[ i = 0 \]
- \[ i = 1 \]

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
</tr>
</tbody>
</table>
RET

Return from Trap

(Privileged Instruction)

Operation:

\[
\begin{align*}
\text{ncwp} & \leftarrow \text{CWP} + 1 \\
\text{ET} & \leftarrow 1 \\
\text{PC} & \leftarrow \text{nPC} \\
\text{nPC} & \leftarrow r[\text{rs1}] + (r[\text{rs2}] \text{ or sign extnd(simm13)}) \\
\text{CWP} & \leftarrow \text{ncwp} \\
S & \leftarrow \text{pS}
\end{align*}
\]

Assembler Syntax: \quad \text{rett } \text{address}

Description: RETT adds one to the Current Window Pointer (modulo the number of implemented windows) and compares this value against the Window Invalid Mask register. If the new window number corresponds to an invalidated window (WIM AND 2^ncwp = 1), a window_underflow trap is generated. If the new window number is not invalid (i.e., its corresponding WIM bit is reset), then RETT causes a delayed control transfer to the address derived by adding the contents of r[rs1] to either the contents of r[rs2] (field bit i = 1) or to the 13-bit, sign-extended immediate value contained in the instruction (field bit i = 0).

Before the control transfer takes place, the new CWP value is written into the PSR, causing the previous window (the one in which the trap was taken) to become the active window. In addition, the PSR's ET bit is set to one (traps enabled) and the previous Supervisor bit (pS) is restored to the S field.

Although in theory RETT is a delayed control transfer instruction, in practice, RETT must always be immediately preceded by a JMPI instruction, creating a delayed control transfer couple (see Section NO TAG). This has the effect of annulling the delay instruction.

If traps were already enabled before encountering the RETT instruction, an illegal_instruction trap is generated. If traps are not enabled (ET=0) when the RETT is encountered, but (1) the processor is not in supervisor mode (S=0), or (2) the window underflow condition described above occurs, or (3) if either of the two low-order bits of the target address are nonzero, then a reset trap occurs. If a reset trap does occur, the n field of the TBR encodes the trap condition: privileged_instruction, window_underflow, or memory_address_not_aligned.

*Programming note:* To re-execute the trapping instruction when returning from a trap handler, use the following sequence:

\[
\begin{align*}
\text{jmpl} & \quad %17, %0 & \quad ! \text{old PC} \\
\text{rett} & \quad %18 & \quad ! \text{old nPC}
\end{align*}
\]

Note that the CY7C601 saves the PC in r[17](local 1) and the nPC in r[18](local2) of the trap window upon entering a trap.

To return to the instruction after the trapping instruction (e.g., when the trapping instruction is emulated), use the sequence:

\[
\begin{align*}
\text{jmpl} & \quad %18, %0 & \quad ! \text{old nPC} \\
\text{rett} & \quad %18 + 4 & \quad ! \text{old nPC + 4}
\end{align*}
\]
RET'T  Return from Trap  RETT
(Privileged Instruction)

Traps:
- illegal_instruction
- reset (privileged_instruction)
- reset (memory_address_not_aligned)
- reset (window_underflow)

Format:

```
  31 30 29 25 24 19 18 14 13 12  5  4  0
  1 0 ignored 1 1 1 0 0 1  rs1 i=0 ignored rs2

  31 30 29 25 24 19 18 14 13 12  0
  1 0 ignored 1 1 1 0 0 1  rs1 i=1 simm13
```
SAVE

Save caller’s window

**Operation:**
ncwp ← CWP - 1
result ← r[rs1] + (r[rs2] or sign extnd(simm13))
CWP ← ncwp
r[rd] ← result

SAVE does not affect condition codes

**Assembler Syntax:**
save reg_rs1, reg_or_imm, reg_rd

**Description:**
SAVE subtracts one from the Current Window Pointer (modulo the number of implemented windows) and compares this value against the Window Invalid Mask register. If the new window number corresponds to an invalidated window (WIM AND 2^{ncwp} = 1), a window_overflow trap is generated. If the new window number is not invalid (i.e., its corresponding WIM bit is reset), then the contents of r[rs1] is added to either the contents of r[rs2] (field bit i = 1) or to the 13-bit, sign-extended immediate value contained in the instruction (field bit i = 0). Because the CWP has not been updated yet, r[rs1] and r[rs2] are read from the currently addressed window (the calling window).

The new CWP value is written into the PSR, causing the active window to become the previous window, and the called window to become the active window. The result of the addition is now written into the [rd] register of the new window.

Note that arithmetic operations involving the CWP are always done modulo the number of implemented windows (8 for the CY7C601).

**Traps:**
window_overflow

**Format:**

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<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
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<th>24</th>
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<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
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<td>1</td>
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<td>rd</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>
```

```
<table>
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<tr>
<th>31</th>
<th>30</th>
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<th>25</th>
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<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
</tr>
</tbody>
</table>
```
SETHI  Set High 22 bits of r register

Operation:
\[ r[rd]<31:10> \leftarrow \text{imm22} \]
\[ r[rd]<9:0> \leftarrow 0 \]

Assembler Syntax:
sethi  const22, reg;rd
sethi  %hi value, reg;rd

Description: SETHI zeros the ten least significant bits of the contents of r[rd] and replaces its high-order 22 bits with imm22. The condition codes are not affected.

Programming note: SETHI 0, %0 is the preferred instruction to use as a NOP, because it will not increase execution time if it follows a load instruction.

Traps: None

Format:
SLL
Shift Left Logical

Operation:  \[ r[rd] \leftarrow r[rs1] \text{ SLL by } (r[rs2] \text{ or } \text{shcnt}) \]

Assembler Syntax:  \text{sll } \text{reg}_rs1, \text{ reg_or_imm, reg}_rd \]

Description:  SLL shifts the contents of \( r[rs1] \) left by the number of bits specified by the shift count, filling the vacated positions with zeros. The shifted results are written into \( r[rd] \). No shift occurs if the shift count is zero.

If the i bit field equals zero, the shift count for SLL is the least significant five bits of the contents of \( r[rs2] \). If the i bit field equals one, the shift count for SLL is the 13-bit, sign extended immediate value, \( \text{simm}_{13} \). In the instruction format and the operation description above, the least significant five bits of \( \text{simm}_{13} \) is called \text{shcnt}.

This instruction does not modify the condition codes.

Traps:  none

Format:

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 0 & \text{rd} & 1 & 0 & 0 & 1 & 0 & 1 & \text{rs1} & \text{i=0} & \text{ignored} & \text{rs2} \\
1 & 0 & \text{rd} & 1 & 0 & 0 & 1 & 0 & 1 & \text{rs1} & \text{i=1} & \text{ignored} & \text{shcnt}
\end{array}
\]
SRA
Shift Right Arithmetic

Operation: \( r[rd] \leftarrow r[rs1] \) SRA by \((r[rs2] \text{ or } \text{shcnt})\)

Assembler
Syntax: \( \text{sra } \text{reg}_{rs1}, \text{ reg}_{or \_imm}, \text{reg}_{rd} \)

Description: SRA shifts the contents of \( r[rs1] \) right by the number of bits specified by the shift count, filling the vacated positions with the MSB of \( r[rs1] \). The shifted results are written into \( r[rd] \). No shift occurs if the shift count is zero.

If the \( i \) bit field equals zero, the shift count for SRA is the least significant five bits of the contents of \( r[rs2] \). If the \( i \) bit field equals one, the shift count for SRA is the 13-bit, sign extended immediate value, simm13. In the instruction format and the operation description above, the least significant five bits of simm13 is called \( \text{shcnt} \).

This instruction does not modify the condition codes.

Programming note: A “Shift Left Arithmetic by 1 (and calculate overflow)” can be implemented with an ADDcc instruction.

Traps: none

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
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<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>i=0</td>
<td>ignored</td>
<td></td>
<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>i=1</td>
<td>ignored</td>
<td></td>
<td>shcnt</td>
<td></td>
</tr>
</tbody>
</table>
Operation: \[ r[rd] \leftarrow r[rs1] \! \text{ SRL by } (r[rs2] \text{ or } \text{shcnt}) \]

Assembler Syntax: \( \text{srl } \text{reg}_c, \text{reg}_r, \text{imm} \), \( \text{reg}_d \)

Description: SRL shifts the contents of \( r[rs1] \) right by the number of bits specified by the shift count, filling the vacated positions with zeros. The shifted results are written into \( r[rd] \). No shift occurs if the shift count is zero.

If the 1 bit field equals zero, the shift count for SRL is the least significant five bits of the contents of \( r[rs2] \). If the 1 bit field equals one, the shift count for SRL is the 13-bit, sign extended immediate value, simm13. In the instruction format and the operation description above, the least significant five bits of simm13 is called \text{shcnt}.

This instruction does not modify the condition codes.

Traps: none

Format:

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 17 & 16 & 15 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 0 & \text{rd} & 1 & 0 & 0 & 1 & 1 & 0 & \text{rs1} & \text{i=0} & \text{ignored} & \text{rs2}
\end{array}
\]

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 17 & 16 & 15 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 0 & \text{rd} & 1 & 0 & 0 & 1 & 1 & 0 & \text{rs1} & \text{i=1} & \text{ignored} & \text{shcnt}
\end{array}
\]
ST Store Word ST

Operation: \([r[\text{rs1}]] + (r[\text{rs2}] \text{ or sign extnd(simm13)])] \rightarrow r[\text{rd}]\)

Assembler Syntax: \(\text{st } \text{reg}_{\text{rd}}, \text{[address]}\)

Description: The ST instruction moves a word from the destination register, \(r[\text{rd}]\), into memory. The effective memory address is derived by summing the contents of \(r[\text{rs1}]\) and either the contents of \(r[\text{rs2}]\) if the instruction’s \(i\) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \(i\) equals one.

If ST takes a trap, the contents of the memory address remain unchanged.

\textbf{Programming note:} If \(rs1\) is set to 0 and \(i\) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps: memory_address_not_aligned
data_access_exception

Format:

```
0  1  2  3  4  5 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1 1  rd  0 0 0 1 0 0  rs1  i=0  ignored  rs2
```

```
0  1  2  3  4  5 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1 1  rd  0 0 0 1 0 0  rs1  i=1     simm13
```
STA

Store Word into Alternate space

(Privileged Instruction)

Operation:
address space ← asi

\[ [r[rs1] + r[rs2]] ← r[rd] \]

Assembler Syntax:

sta regrd, [regaddr] asi

Description:
The STA instruction moves a word from the destination register, r[rd], into memory. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of r[rs1] and r[rs2].

If STA takes a trap, the contents of the memory address remain unchanged.

Traps:

illegal_instruction (if i=1)
privileged_instruction (if S=0)
memory_address_not_aligned
data_access_exception

Format:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>rs1</td>
<td>i=0</td>
<td>asi</td>
<td></td>
<td>rs2</td>
</tr>
</tbody>
</table>
```
**Operation:**
\[ r[r{s1}] + (r[r{s2}] or sign extnd(simm13)) \rightarrow r[r{d}] \]

**Assembler Syntax:**
```
stb reg, address
```

**Description:**
The STB instruction moves the least significant byte from the destination register, \( r[r{d}] \), into memory. The effective memory address is derived by summing the contents of \( r[r{s1}] \) and either the contents of \( r[r{s2}] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one.

If STB takes a trap, the contents of the memory address remain unchanged.

*Programming note:* If \( r{s1} \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

**Traps:**
data_access_exception

**Format:**

```
   31  30  29  25  24  19  18  14  13  12  5  4  0
   1  1    rd  0 0 0 1 0 1  rs1  i=0  ignored  rs2
```

```
   31  30  29  25  24  19  18  14  13  12  0
   1  1    rd  0 0 0 1 0 1  rs1  i=1  simm13
```
STBA Store Byte into Alternate space
(Privileged Instruction)

Operation:   
address space ← asi
[r[rs1] + r[rs2]] ← r[rd]

Assembler Syntax: 
stba reg, [reg addr] asi

Description: The STBA instruction moves the least significant byte from the destination register, r[rd], into memory. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of r[rs1] and r[rs2].

If STBA takes a trap, the contents of the memory address remain unchanged.

Traps:        
illegal_instruction (if i=1)
privileged_instruction (if S=0)
data_access_exception

Format:

```
  31 30 29 25 24 19 18 14 13 12  5  4  0
  1 1  rd 0 1 0 1 0 1  rs1  i=0  asi  rs2
```
**STC**

**Operation:**

\[ [r[rs1]] + (r[rs2] or sign extnd(simm13))] \rightarrow c[rd] \]

**Assembler Syntax:**

\[ st \ creg_{rd}, \ [address] \]

**Description:**

The STC instruction moves a word from a coprocessor register, c[rd], into memory. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one.

If the PSR’s EC bit is set to zero or if no coprocessor is present, a \texttt{cp\_disabled} trap will be generated. If STC takes a trap, memory remains unchanged.

*Programming note:* If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

**Traps:**

- \texttt{cp\_disabled}
- \texttt{cp\_exception}
- \texttt{memory\_address\_not\_aligned}
- \texttt{data\_access\_exception}

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>( i=0 )</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>( i=1 )</td>
<td>simm13</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
STCSR Store Coprocessor State Register

**Operation:** \([r[rs1] + (r[rs2] \text{ or sign extnd(simm13))}] \rightarrow CSR\)

**Assembler Syntax:** `st %csr, [address]`

**Description:** The STCSR instruction moves the contents of the Coprocessor State Register into memory. The effective memory address is derived by summing the contents of \(r[rs1]\) and either the contents of \(r[rs2]\) if the instruction’s \(i\) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \(i\) equals one.

If the PSR’s EC bit is set to zero or if no coprocessor is present, a cp_disabled trap will be generated. If STCSR takes a trap, the contents of the memory address remain unchanged.

*Programming note:* If \(rs1\) is set to 0 and \(i\) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

**Traps:** cp_disabled
memory_address_not_aligned
data_access_exception

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>i=1</td>
<td>simm13</td>
</tr>
</tbody>
</table>
STD Store Doubleword

Operation:
[r[rs1] + (r[rs2] or sign extnd(simm13))] ← r[rd]
[r[rs1] + (r[rs2] or sign extnd(simm13)) + 4] ← r[rd + 1]

Assembler Syntax:

std reg Rd, [address]

Description:
The STD instruction moves a doubleword from the destination register pair, r[rd] and r[rd+1], into memory. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one. The most significant word in the even-numbered destination register is written into memory at the effective address and the least significant memory word in the next odd-numbered register is written into memory at the effective address + 4.

If a data_access_exception trap takes place during the effective address memory access, memory remains unchanged.

Programming note: If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps:
memory_address_not_aligned
data_access_exception

Format:

```
  31  30  29  25  24  19  18  14  13  12  5  4  0
  1  1  rd  0 0 0 1 1 1  rs1  i=0  ignored  rs2
```

```
  31  30  29  25  24  19  18  14  13  12  0
  1  1  rd  0 0 0 1 1 1  rs1  i=1  simm13
```
STDA

Store Doubleword into Alternate space

(Privileged Instruction)

Operation:
address space ← asi
[r[rs1] + (r[rs2] or sign extnd(simm13))] ← r[rd]
[r[rs1] + (r[rs2] or sign extnd(simm13)) + 4] ← r[rd + 1]

Assembler Syntax:
stda reg rd, [reg addr] asi

Description:
The STDA instruction moves a doubleword from the destination register pair, r[rd] and r[rd+1], into memory. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of r[rs1] and r[rs2]. The most significant word in the even-numbered destination register is written into memory at the effective address and the least significant memory word in the next odd-numbered register is written into memory at the effective address + 4.

If a data_access_exception trap takes place during the effective address memory access, memory remains unchanged.

Traps:
illegal_instruction (if i=1)
privileged_instruction (if S=0)
memory_address_not_aligned
data_access_exception

Format:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 1  | rd | 0  | 1  | 1  | 1  | rs1| i=0| asi|  |    |    |    |    |    |    |    |    |    |    |    |    | rs2|    |    |    |    |    |    |    |    |
The STDC instruction moves a doubleword from the coprocessor register pair, c[rd] and c[rd+1], into memory. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one. The most significant word in the even-numbered destination register is written into memory at the effective address and the least significant memory word in the next odd-numbered register is written into memory at the effective address + 4.

If the PSR’s EC bit is set to zero or if no coprocessor is present, a cp_disabled trap will be generated. If a data_access_exception trap takes place during the effective address memory access, memory remains unchanged.

Programming note: If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps:
- cp_disabled
- cp_exception
- memory_address_not_aligned
- data_access_exception

Format:

```
  31 30 29 25 24 19 18 14 13 12  5  4  0
  1  1  rd 110111 rs1  i=0 ignored rs2

  31 30 29 25 24 19 18 14 13 12  0
  1  1  rd 110111 rs1  i=1 simm13
```
STDCQ

(Privileged Instruction)

Operation:

\[ [r[rs1] + (i[r[rs2]] or sign extnd(simm13))] \leftarrow \text{CQ.ADDR} \]

\[ [r[rs1] + (i[r[rs2]] or sign extnd(simm13)) + 4] \leftarrow \text{CQ.INSTR} \]

Assembler Syntax:

\text{std %cq, [address]}

Description:

The STDCQ instruction moves the front entry of the Coprocessor Queue into memory. The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. The address portion of the queue entry is written into memory at the effective address and the instruction portion of the entry is written into memory at the effective address + 4.

If the PSR’s EC bit is set to zero or if no coprocessor is present, a \text{cp_disabled} trap will be generated. If a \text{data_access_exception} trap takes place during the effective address memory access, memory remains unchanged.

\textit{Programming note:} If \textit{rs1} is set to \textit{0} and \textit{i} is set to \textit{1}, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps:

\text{cp_disabled}

\text{cp_exception}

\text{privileged_instruction (if S=0)}

\text{memory_address_not_aligned}

\text{data_access_exception}

Format:

\begin{center}
\begin{tabular}{cccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 1 & rd & 1 & 1 & 0 & 1 & 1 & 0 & rs1 & i=0 & ignored & & & & rs2 \\
1 & 1 & rd & 1 & 1 & 0 & 1 & 1 & 0 & rs1 & i=1 & & & & simm13 \\
\end{tabular}
\end{center}
STDF: Store Doubleword Floating-Point

Operation:
[r[rs1] + (r[rs2] or sign extnd(simm13))] —> f[rd]
[r[rs1] + (r[rs2] or sign extnd(simm13)) + 4] —> f[rd + 1]

Assembler Syntax:
std freg rd, [address]

Description:
The STDF instruction moves a doubleword from the floating-point register pair, f[rd] and f[rd+1], into memory. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one. The most significant word in the even-numbered destination register is written into memory at the effective address and the least significant memory word in the next odd-numbered register is written into memory at the effective address + 4.

If the PSR’s EF bit is set to zero or if no floating-point unit is present, an fp_disabled trap will be generated. If a trap takes place, memory remains unchanged.

Programming note: If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps:
fp_disabled
fp_exception*
memory_address_not_aligned
data_access_exception

Format:

```
  31 30 29 25 24 19 18 14 13 12  5 4  0
  1 1  rd   1 0 0 1 1 1     rs1  i=0  ignored  rs2

  31 30 29 25 24 19 18 14 13 12  0
  1 1  rd   1 0 0 1 1 1     rs1  i=1   simm13
```

* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
STDFQ

Store Doubleword Floating-Point Queue

(Privileged Instruction)

Operation:

\[ [r[rs1] + (r[rs2] \text{ or sign extnd(simm13))] \leftarrow \text{FQ.ADDR} \]

\[ [r[rs1] + (r[rs2] \text{ or sign extnd(simm13)}) + 4] \leftarrow \text{FQ.INSTR} \]

Assembler

Syntax:

\text{std} \ %fq, [address]

Description:

The STDFQ instruction moves the front entry of the floating-point queue into memory. The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. The address portion of the queue entry is written into memory at the effective address and the instruction portion of the entry is written into memory at the effective address + 4.

If the FPU is in exception mode, the queue is then advanced to the next entry, or it becomes empty (as indicated by the \( qn \) bit in the FSR).

If the PSR’s EF bit is set to zero or if no floating-point unit is present, an \( \text{fp_disabled} \) trap will be generated. If a trap takes place, memory remains unchanged.

Programming note: If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps:

\( \text{fp_disabled} \)

\( \text{fp_exception} \)

privileged_instruction (if \( S=0 \))

memory_address_not_aligned

data_access_exception

Format:

\[
\begin{array}{ccccccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 1 & rd & 1 & 0 & 0 & 1 & 1 & 0 & rs1 & i=0 & ignored & & rs2 \\
\end{array}
\]

\[
\begin{array}{ccccccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 0 \\
1 & 1 & rd & 1 & 0 & 0 & 1 & 1 & 0 & rs1 & i=1 & & simm13 \\
\end{array}
\]

*NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
STF

Operation: \[ r[rs1] + (r[rs2] \text{ or sign extnd(simm13)}) \rightarrow f[rd] \]

Assembler Syntax: \( st \ freg rd, \ [address] \)

Description: The STF instruction moves a word from a floating-point register, \( f[rd] \), into memory. The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one.

If the PSR’s EF bit is set to zero or if no floating-point unit is present, an fp_disabled trap will be generated. If STF takes a trap, memory remains unchanged.

Programming note: If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps: fp_disabled
        fp_exception*
        memory_address_not_aligned
        data_access_exception

Format:

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
\hline
1 & 1 & rd & 1 & 0 & 0 & 1 & 0 & 0 & rs1 & i=0 & ignored & rs2 \\
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 0 \\
\hline
1 & 1 & rd & 1 & 0 & 0 & 1 & 0 & 0 & rs1 & i=1 & simm13 \\
\end{array}
\]

* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
STFSR Store Floating-Point State Register

Operation: \[ \text{[r[rs1] + (r[rs2] or sign extnd(simm13))]} \rightarrow \text{FSR} \]

Assembler Syntax: \text{st \%fsr, [address]} \]

Description: The STFSR instruction moves the contents of the Floating-Point State Register into memory. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s \(i\) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \(i\) equals one. This instruction will wait for all pending FPops to complete execution before it writes the FSR into memory.

If the PSR’s EF bit is set to zero or if no floating-point unit is present, an fp_disabled trap will be generated. If STFSR takes a trap, the contents of the memory address remain unchanged.

Programming note: If \(rs1\) is set to 0 and \(i\) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps: fp_disabled
fp_exception*
memory_address_not_aligned
data_access_exception

Format:

```
 31 30 29 25 24 19 18 14 13 12 5 4 0
1 1          rd    1 0 0 1 0 1    rs1    i=0       ignored     rs2
```

```
 31 30 29 25 24 19 18 14 13 12
1 1          rd    1 0 0 1 0 1    rs1    i=1       simm13
```

* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
**Operation:**  
\[ r[rs1] + (r[rs2] \text{ or sign extnd(simm13)}) \rightarrow r[rd] \]

**Assembler Syntax:**  
```
sth regrd, [address]  synonyms: stuh, stsh
```

**Description:**  
The STH instruction moves the least significant halfword from the destination register, \( r[rd] \), into memory. The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction's \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one.

If STH takes a trap, the contents of the memory address remain unchanged.

*Programming note:* If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

**Traps:**  
- memory_address_not_aligned
- data_access_exception

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>( rs1 )</td>
<td>( i=0 )</td>
<td>ignored</td>
<td>( rs2 )</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
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<th>19</th>
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<td>1</td>
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<td>rd</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>( rs1 )</td>
<td>( i=1 )</td>
<td>simm13</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
STHA Store Halfword into Alternate space

(Privileged Instruction)

**Operation:**

- address space $\leftarrow$ asi
- $[r[rs1] + (r[rs2] or sign extnd(simm13))] \leftarrow r[rd]$

**Assembler Syntax:**

```
stha reg_rd, [address]
```

**Description:**

The STHA instruction moves the least significant halfword from the destination register, $r[rd]$, into memory. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of $r[rs1]$ and $r[rs2]$. If STHA takes a trap, the contents of the memory address remain unchanged.

**Traps:**

- illegal_instruction (if $i=1$)
- privileged_instruction (if $S=0$)
- memory_address_not_aligned
- data_access_exception

**Format:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 1  | RD | 010110 | RS1 | i=0 | ASI | RS2 |

**Syntax:**

```
stha reg_rd, [address]
```

**Synonyms:**

stuh, stsha
SUB Subtract

Operation: \[ r[rd] \leftarrow r[rs1] \cdot (r[rs2] \text{ or sign extnd(simm13)}) \]

Assembler Syntax: sub reg_rs1, reg_or_imm, reg_rd

Description: The SUB instruction subtracts either the contents of the register named in the \(rs2\) field, \(r[rs2]\), if the instruction’s \(i\) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \(i\) equals one, from register \(r[rs1]\). The result is placed in the register specified in the \(rd\) field.

Traps: none

Format:

```
  | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
  | 1  | 0  | rd | 0 0 0 1 0 | 0 | rs1 | i=0 | ignored |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
  | 1  | 0  | rd | 0 0 0 1 0 | 0 | rs1 | i=1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
```
**Operation:**

\[ r[rd] \leftarrow r[rs1] - \text{operand2, where operand2} = (r[rs2] \text{ or sign extnd(simm13)}) \]

- \( n \leftarrow r[rd] <31> \)
- \( z \leftarrow \text{if } r[rd] = 0 \text{ then } 1, \text{ else } 0 \)
- \( v \leftarrow (r[rs1]<31> \text{ AND not operand2}<31> \text{ AND not } r[rd]<31>) \text{ OR (not } r[rs1]<31> \text{ AND operand2}<31> \text{ AND } r[rd]<31>) \)
- \( c \leftarrow (\text{not } r[rs1]<31> \text{ AND operand2}<31>) \text{ OR (} r[rd]<31> \text{ AND (not } r[rs1]<31> \text{ OR operand2}<31>) \text{)} \)

**Assembler Syntax:**

\text{subcc regrs1, reg_or_imm, reged}

**Description:**

The SUBcc instruction subtracts either the contents of register \( r[rs2] \) (if the instruction’s \( i \) bit equals zero) or the 13-bit, sign-extended immediate operand contained in the instruction (if \( i \) equals one) from register \( r[rs1] \). The result is placed in register \( r[rd] \). In addition, SUBcc modifies all the integer condition codes in the manner described above.

*Programming note:* A SUBcc instruction with \( rd = 0 \) can be used for signed and unsigned integer comparison.

**Traps:**

none

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0 1 0 0 0</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0 1 0 0 0</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## SUBX - Subtract with Carry

**Operation:**
\[ r[rd] \leftarrow r[rs1] - (r[rs2] \text{ or sign extnd(simmm13)}) - c \]

**Assembler Syntax:**
```
subx reg, reg_or_imm, reg
```

**Description:**
SUBX subtracts either the contents of register \(r[rs2]\) (if the instruction's \(i\) bit equals zero) or the 13-bit, sign-extended immediate operand contained in the instruction (if \(i\) equals one) from register \(r[rs1]\). It then subtracts the PSR’s carry bit (\(c\)) from that result. The final result is placed in the register specified in the \(rd\) field.

**Traps:**
none

**Format:**

- For \(i = 0\):
  
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>001100</td>
<td>rs1</td>
<td>(i = 0)</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- For \(i = 1\):

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>001100</td>
<td>rs1</td>
<td>(i = 1)</td>
<td>simmm13</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**SUBXcc**

**Operation:**

\[
\begin{align*}
  &r[rd] \leftarrow r[rs1] - \text{operand2} - c, \text{ where operand2} = (r[rs2] \text{ or sign extnd(simm13)}) \\
  &n \leftarrow r[rd]<31> \\
  &z \leftarrow \text{if } r[rd] = 0 \text{ then 1, else 0} \\
  &v \leftarrow (r[rs1]<31> \text{ AND not operand2}<31> \text{ AND not } r[rd]<31>) \text{ OR (not } r[rs1]<31> \text{ AND operand2}<31> \text{ AND } r[rd]<31>) \\
  &c \leftarrow (\text{not } r[rs1]<31> \text{ AND operand2}<31>) \text{ OR ( } r[rd]<31> \text{ AND (not } r[rs1]<31> \text{ OR operand2}<31>)) \\
\end{align*}
\]

**Assembler Syntax:**

\[\text{subxcc } \text{reg}_{rs1}, \text{ reg}_{or} \_ \text{imm}, \text{ reg}_{rd}\]

**Description:**

SUBXcc subtracts either the contents of register \(r[rs2]\) (if the instruction’s \(i\) bit equals zero) or the 13-bit, sign-extended immediate operand contained in the instruction (if \(i\) equals one) from register \(r[rs1]\). It then subtracts the PSR’s carry bit (\(c\)) from that result. The final result is placed in the register specified in the \(rd\) field. In addition, SUBXcc modifies all the integer condition codes in the manner described above.

**Traps:**

none

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0 1 1 0 0</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
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<th>18</th>
<th>14</th>
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<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0 1 1 0 0</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
SWAP

Swap \( r \) register with memory

Operation:  
\[
\begin{align*}
\text{word} &\gets [r[rs1] + r[rs2] \text{ or sign extnd(simm13) }] \\
\text{temp} &\gets r[rd] \\
r[rd] &\gets \text{word} \\
r[rs1] + (r[rs2] \text{ or sign extnd(simm13)}) &\gets \text{temp}
\end{align*}
\]

Assembler Syntax:  
\[
\text{swap [source], reg}_{rd}
\]

Description:  
SWAP atomically exchanges the contents of \( r[rd] \) with the contents of a memory location, i.e., without allowing asynchronous trap interruptions. In a multiprocessor system, two or more processors executing SWAP instructions simultaneously are guaranteed to execute them serially, in some order. The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction's \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. If SWAP takes a trap, the contents of the memory address and the destination register remain unchanged.

Programming note: If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps:  
- memory_address_not_aligned  
- data_access_exception

Format:  
\[
\begin{array}{cccccccc}
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
\hline
1 & 1 & \text{rd} & 0 & 0 & 1 & 1 & 1 & 1 & i=0 & \text{ignored} & \text{rs2}
\end{array}
\]

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 0 \\
\hline
1 & 1 & \text{rd} & 0 & 0 & 1 & 1 & 1 & 1 & i=1 & \text{simm13}
\end{array}
\]
SWAPA

Swap \( r \) register with memory in Alternate space

(Privileged Instruction)

Operation:
- address space \( \leftrightarrow \) asi
- word \( \leftrightarrow [r[rs1] + r[rs2]] \)
- temp \( \leftrightarrow r[rd] \)
- \( r[rd] \leftarrow \) word
- \( [r[rs1] + r[rs2]] \leftarrow \) temp

Assembler Syntax:
```
swapa [regsource] asi, regrd
```

Description:
SWAPA atomically exchanges the contents of \( r[rd] \) with the contents of a memory location, i.e., without allowing asynchronous trap interruptions. In a multiprocessor system, two or more processors executing SWAPA instructions simultaneously are guaranteed to execute them serially, in some order.

The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of \( r[rs1] \) and \( r[rs2] \).

If SWAPA takes a trap, the contents of the memory address and the destination register remain unchanged.

Traps:
- illegal_instruction (if \( i=1 \))
- privileged_instruction (if \( S=0 \))
- memory_address_not_aligned
- data_access_exception

Format:
```
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 1  | rd | 0 | 1 | 1 | 1 | 1 | 1 | rs1 | 0  | asi | 0  | rs1 | 0  | asi | 0  | rs1 | 0  | asi | 0  | rs1 | 0  | asi | 0  | rs2 |
```
TADDcc
Tagged Add and modifyicc

Operation:
\( r[rd] \leftarrow r[rs1] + \text{operand2} \), where operand2 = (\( r[rs2] \) or sign extnd(simm13))
\n\( n \leftarrow r[rd]<31> \)
\( z \leftarrow \text{if } r[rd]=0 \text{ then } 1, \text{ else } 0 \)
\( v \leftarrow (r[rs1]<31> \text{ AND operand2}<31> \text{ AND not } r[rd]<31>) \)
\( \quad \text{OR (not } r[rs1]<31> \text{ AND not operand2}<31> \text{ AND } r[rd]<31>) \)
\( \quad \text{OR (} r[rs1]<1:0> \neq 0 \text{ OR operand2}<1:0> \neq 0) \)
\( c \leftarrow (r[rs1]<31> \text{ AND operand2}<31>) \)
\( \quad \text{OR (not } r[rd]<31> \text{ AND (} r[rs1]<31> \text{ OR operand2}<31>)) \)

Assembler
Syntax:
taddcc reg_{rs1}, reg_{or_imm}, reg_{rd}

Description:
TADDcc adds the contents of \( r[rs1] \) to either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or to a 13-bit, sign-extended immediate operand if \( i \) equals one. The result is placed in the register specified in the \( rd \) field. In addition to the normal arithmetic overflow, an overflow condition also exists if bit 1 or bit 0 of either operand is not zero. TADDcc modifies all the integer condition codes in the manner described above.

Traps:
none

Format:

\[
\begin{array}{cccccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
\end{array}
\begin{array}{cccccccc}
1 & 0 & rd & 1 & 0 & 0 & 0 & 0 & 0 & rs1 & i=0 & ignored & rs2 \\
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 0 \\
1 & 0 & rd & 1 & 0 & 0 & 0 & 0 & rs1 & i=1 & simm13 \\
\end{array}
\]
TADDeccTV  Tagged Add (modify icc) Trap on Overflow TADDeccTV

Operation:

\[
\text{result} \leftarrow r[rs1] + \text{operand2}, \text{ where operand 2} = (r[rs2] \text{ or sign extnd(simm13)})
\]

\[
tv \leftarrow (r[rs1]<31> \text{ AND operand2}<31> \text{ AND not r[rd]<31>) OR (not r[rs1]<31> \text{ AND not operand2}<31> \text{ AND r[rd]<31>) OR (r[rs1]<1:0> \neq 0 \text{ OR operand2}<1:0> \neq 0})
\]

if tv = 1, then tag overflow trap; else

\[
\text{r[rd] }\leftarrow \text{ result}
\]

Assembler Syntax:

taddcctv reg,reg_or_imm,reg

Description:

TADDeccTV adds the contents of r[rs1] to either the contents of r[rs2] if the instruction’s i bit equals zero, or to a 13-bit, sign-extended immediate operand if i equals one. In addition to the normal arithmetic overflow, an overflow condition also exists if bit 1 or bit 0 of either operand is not zero.

If TADDeccTV detects an overflow condition, a tag_overflow trap is generated and the destination register and condition codes remain unchanged. If no overflow is detected, TADDeccTV places the result in the register specified in the rd field and modifies all the integer condition codes in the manner described above (the overflow bit is, of course, set to zero).

Traps:
tag_overflow

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1 0 0 0 1 0</td>
<td>rs1</td>
<td>1=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
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<tbody>
<tr>
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<td>0</td>
<td>rd</td>
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<td>rs1</td>
<td>1=1</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Tricc

**Operation:**

If condition true, then trap_instruction;

\[
t = 128 + [r[rs1] + (r[rs2] \text{ or sign extnd(simm13))}] <6:0>
\]

else PC \rightarrow nPC

nPC \rightarrow nPC + 4

**Assembler Syntax:**

- ta{,a} label
- tn{,a} label
- tnc{,a} label synonym: tnz
- tc{,a} label synonym: tz
- tg{,a} label
- tle{,a} label
- tgu{,a} label
- tl{,a} label
- tleu{,a} label
- tcc{,a} label synonym: tgeu
- tcs{,a} label synonym: tl
- tpos{,a} label
- tneg{,a} label
- tvc{,a} label
- tvs{,a} label

**Description:**

A Ticc instruction evaluates specific integer condition code combinations (from the PSR’s `icc` field) based on the trap type as specified by the value in the instruction’s `cond` field. If the specified combination of condition codes evaluates as true, and there are no higher-priority traps pending, then a trap_instruction trap is generated. If the condition codes evaluate as false, the trap is not generated.

If a trap_instruction trap is generated, the `tt` field of the Trap Base Register (TBR) is written with 128 plus the least significant seven bits of `r[rs1]` plus either `r[rs2]` (bit field `i = 0`) or the 13-bit sign-extended immediate value contained in the instruction (bit field `i = 1`). See Section NO TAG for the complete definition of a trap.

**Traps:**

- trap_instruction
## Ticc

### Trap on integer condition codes

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Cond.</th>
<th>Operation</th>
<th>icc Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>TN</td>
<td>0000</td>
<td>Trap Never</td>
<td>No test</td>
</tr>
<tr>
<td>TE</td>
<td>0001</td>
<td>Trap on Equal</td>
<td>z</td>
</tr>
<tr>
<td>TLE</td>
<td>0010</td>
<td>Trap on Less or Equal</td>
<td>z OR (n XOR v)</td>
</tr>
<tr>
<td>TL</td>
<td>0011</td>
<td>Trap on Less</td>
<td>n XOR v</td>
</tr>
<tr>
<td>TLEU</td>
<td>0100</td>
<td>Trap on Less or Equal, Unsigned</td>
<td>c OR z</td>
</tr>
<tr>
<td>TCS</td>
<td>0101</td>
<td>Trap on Carry Set (Less than, Unsigned)</td>
<td>c</td>
</tr>
<tr>
<td>TNEG</td>
<td>0110</td>
<td>Trap on Negative</td>
<td>n</td>
</tr>
<tr>
<td>TVS</td>
<td>0111</td>
<td>Trap on Overflow Set</td>
<td>v</td>
</tr>
<tr>
<td>TA</td>
<td>1000</td>
<td>Trap Always</td>
<td>No test</td>
</tr>
<tr>
<td>TNE</td>
<td>1001</td>
<td>Trap on Not Equal</td>
<td>not z</td>
</tr>
<tr>
<td>TG</td>
<td>1010</td>
<td>Trap on Greater</td>
<td>not(z OR (n XOR v))</td>
</tr>
<tr>
<td>TGE</td>
<td>1011</td>
<td>Trap on Greater or Equal</td>
<td>not(n XOR v)</td>
</tr>
<tr>
<td>TGU</td>
<td>1100</td>
<td>Trap on Greater, Unsigned</td>
<td>not(c OR z)</td>
</tr>
<tr>
<td>TCC</td>
<td>1101</td>
<td>Trap on Carry Clear (Greater than or Equal, Unsigned)</td>
<td>not c</td>
</tr>
<tr>
<td>TPOS</td>
<td>1110</td>
<td>Trap on Positive</td>
<td>not n</td>
</tr>
<tr>
<td>TVC</td>
<td>1111</td>
<td>Trap on Overflow Clear</td>
<td>not v</td>
</tr>
</tbody>
</table>

**Format:**

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<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
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<th>4</th>
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</tr>
</thead>
<tbody>
<tr>
<td>1</td>
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<td>cond.</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
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<table>
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<th>31</th>
<th>30</th>
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<td>1</td>
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<td>ign.</td>
<td>cond.</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

*ign. = ignored
cond. = condition*
TSUBcc

Tagged Subtract and modify icc

Operation:
\[ r[rd] \leftarrow r[rs1] - \text{operand2}, \text{where} \quad \text{operand2} = (r[rs2] \text{ or } \text{sign extnd(simm13)}) \]
\[ n \leftarrow r[rd]<31> \]
\[ z \leftarrow \text{if } r[rd]=0 \text{ then 1, else 0} \]
\[ v \leftarrow (r[rs1]<31> \text{ AND not operand2}<31> \text{ AND not } r[rd]<31>) \text{ OR } (\text{not } r[rs1]<31> \text{ AND operand2}<31> \text{ AND } r[rd]<31>) \]
\[ c \leftarrow (\text{not } r[rs1]<31> \text{ AND operand2}<31> \text{ OR } (r[rd]<31> \text{ AND (not } r[rs1]<31> \text{ OR operand2}<31>))) \]

Assembler Syntax:
\[ \text{tsubcc } \text{reg}_rsl, \text{ reg}_o r\_i m m, \text{ reg}_r d \]

Description:
TSUBcc subtracts either the contents of register \( r[rs2] \) (if the instruction’s \( i \) bit equals zero) or the 13-bit, sign-extended immediate operand contained in the instruction (if \( i \) equals one) from register \( r[rs1] \). The result is placed in the register specified in the \( rd \) field. In addition to the normal arithmetic overflow, an overflow condition also exists if bit 1 or bit 0 of either operand is not zero. TSUBcc modifies all the integer condition codes in the manner described above.

Traps:
none

Format:

\[
\begin{array}{ccccccccccc}
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
& 1 & 0 & rd & 1 & 0 & 0 & 0 & 1 & rs1 & i=0 & ignored & rs2 \\
\end{array}
\]

\[
\begin{array}{ccccccccccc}
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
& 1 & 0 & rd & 1 & 0 & 0 & 0 & 1 & rs1 & i=1 & simm13 & \\
\end{array}
\]
TSUBccTV

Tagged Subtract (modify icc)

Trap on Overflow

Operation:

\[
\begin{align*}
\text{result} & \leftarrow r[rs1] - \text{operand2}, \text{where operand2} = (r[rs2] \text{ or sign extnd(simm13)}) \\
\text{tv} & \leftarrow \left( (r[rs1]<31> \text{ AND not operand2}<31> \text{ AND not r[rd]<31>}) \text{ OR (not r[rs1]<31> AND operand2}<31> \text{ AND r[rd]<31>}) \\
& \text{ OR (r[rs1]<1:0> \neq 0 \text{ OR operand2}<1:0> \neq 0})
\right)
\end{align*}
\]

if tv = 1, then tag overflow trap; else
\[
\begin{align*}
\text{a} & \leftarrow r[rd]<31>
\text{z} & \leftarrow \text{if r[rd]=0 then 1, else 0}
\text{v} & \leftarrow \text{tv}
\text{c} & \leftarrow \left( \text{not(r[rs1]<31>) AND operand2}<31> \text{ OR (r[rd]<31> AND (not(r[rs1]<31>) OR operand2}<31>)) \right)
\text{r[rd]} & \leftarrow \text{result}
\end{align*}
\]

Assembler Syntax:

\text{tsubccvt reg}_{rs1}, \text{reg}_{or_imm}, \text{reg}_{rd}

Description:

TSUBccTV subtracts either the contents of register r[rs2] (if the instruction’s i bit equals zero) or the 13-bit, sign-extended immediate operand contained in the instruction (if i equals one) from register r[rs1]. In addition to the normal arithmetic overflow, an overflow condition also exists if bit 1 or bit 0 of either operand is not zero.

If TSUBccTV detects an overflow condition, a tag_overflow trap is generated and the destination register and condition codes remain unchanged. If no overflow is detected, TSUBccTV places the result in the register specified in the rd field and modifies all the integer condition codes in the manner described above (the overflow bit is, of course, set to zero).

Traps:

\text{tag\_overflow}

Format:  

\[
\begin{array}{cccccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
\hline
1 & 0 & \text{rd} & 1 & 0 & 0 & 0 & 1 & 1 & \text{rs1} & \text{\_i=0} & \text{ignored} & \text{rs2} \\
\hline
1 & 0 & \text{rd} & 1 & 0 & 0 & 0 & 1 & 1 & \text{rs1} & \text{\_i=1} & \text{\_simm13} & \text{0} \\
\end{array}
\]
UNIMP  Unimplemented instruction  UNIMP

Operation: illegal instruction trap

Assembler Syntax: unimp const22

Description: Executing the UNIMP instruction causes an immediate illegal_instruction trap. The value in the const22 field is ignored.

*Programming note:* UNIMP can be used as part of the protocol for calling a function that is expected to return an aggregate value, such as a C-language structure.

1. An UNIMP instruction is placed after (not in) the delay slot after the CALL instruction in the calling function.

2. If the called function is expecting to return a structure, it will find the size of the structure that the caller expects to be returned as the const22 operand of the UNIMP instruction. The called function can check the opcode to make sure it is indeed UNIMP.

3. If the function is not going to return a structure, upon returning, it attempts to execute UNIMP rather than skipping over it as it should. This causes the program to terminate. The behavior adds some run-time checking to an interface that cannot be checked properly at compile time.

Traps: illegal_instruction

Format:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0  | 0  | ignored | 0  | 0 | 0  | const22 |
WRPSR Write Processor State Register

(Pri vileged Instruction)

Operation: \[ \text{PSR} \leftarrow r[rs1] \ XOR \ (r[rs2] \text{ or sign extnd(simm13)}) \]

Assembler Syntax: \[ \text{wr } \text{reg}_{rs1}, \text{ reg}_{or} \text{ _imm}, \%psr \]

Description: WRPSR does a bitwise logical XOR of the contents of register \(r[rs1]\) with either the contents of \(r[rs2]\) (if bit field \(i=0\)) or the 13-bit sign-extended immediate value contained in the instruction (if bit field \(i=1\)). The result is written into the writable subfields of the PSR. However, if the result’s CWP field would point to an unimplemented window, an illegal_instruction trap is generated and the PSR remains unchanged.

WRPSR is a delayed-write instruction:

1. If any of the three instructions following a WRPSR uses any PSR field that WRPSR modified, the value of that field is unpredictable. Note that any instruction which references a non-global register makes use of the CWP, so following WRPSR with three NOPs would be the safest course.

2. If a WRPSR instruction is updating the PSR’s Processor Interrupt Level (PIL) to a new value and is simultaneously setting Enable Traps (ET) to one, this could result in an interrupt trap at a level equal to the old PIL value.

3. If any of the three instructions after a WRPSR instruction reads the modified PSR, the value read is unpredictable.

4. If any of the three instructions after a WRPSR is trapped, a subsequent RDPSR in the trap handler will get the register’s new value.

Programming note: Two WRPSR instructions should be used when enabling traps and changing the PIL value. The first WRPSR should specify ET=0 with the new PIL value, and the second should specify ET=1 with the new PIL value.

Traps: illegal_instruction
privileged_instruction (if \(S=0\))

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
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<th>4</th>
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</tr>
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<tbody>
<tr>
<td>1</td>
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<td>ignored</td>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
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<table>
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<th>30</th>
<th>29</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>ignored</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>simm13</td>
<td></td>
</tr>
</tbody>
</table>
**WRTBR**

Write Trap Base Register

*(Privileged Instruction)*

**Operation:**

TBR ← \( r[rs1] \) XOR (\( r[rs2] \) or sign extnd(simm13))

**Assembler Syntax:**

```plaintext
wr reg, reg_or_imm, %tbr
```

**Description:**

WRTBR does a bitwise logical XOR of the contents of register \( r[rs1] \) with either the contents of \( r[rs2] \) (if bit field \( i=0 \)) or the 13-bit sign-extended immediate value contained in the instruction (if bit field \( i=1 \)). The result is written into the Trap Base Address field of the TBR.

WRTBR is a delayed-write instruction:

1. If any of the three instructions following a WRTBR causes a trap, the TBA used may be either the old or the new value.
2. If any of the three instructions after a WRTBR is trapped, a subsequent RDTBR in the trap handler will get the register’s new TBA value.

**Traps:**

privileged_instruction (if \( S=0 \))

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
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<th>28</th>
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<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|
| 1  | 0  | ignored | 1  | 1  | 0  | 0  | 0  | 1  | rs1 | 1  | ignored | simm13 |
WRWIM  Write Window Invalid Mask register  WRWIM

(Privileged Instruction)

Operation:  WIM ← r[rs1] XOR (r[rs2] or sign extnd(simm13))

Assembler Syntax:  wr reg, reg_or_imm, %wim

Description:  WRWIM does a bitwise logical XOR of the contents of register r[rs1] with either the contents of r[rs2] (if bit field i=0) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field i=1). The result is written into the writable bits of the WIM register.

WRWIM is a delayed-write instruction:

1. If any of the three instructions following a WRWIM is a SAVE, RESTORE, or RETT, the occurrence of window_overflow and window_underflow is unpredictable.
2. If any of the three instructions after a WRWIM instruction reads the modified WIM, the value read is unpredictable.
3. If any of the three instructions after a WRWIM is trapped, a subsequent RDWIM in the trap handler will get the register’s new value.

Traps:  privileged_instruction (if S=0)

Format:  

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1   | 0  | ignored | 110010 | rs1 | i=0 | ignored | rs2 | 1   | 0  | ignored | 110010 | rs1 | i=1 | simm13 |
WRY  Write Y register  WRY

Operation:  \( Y \leftarrow r[rs1] \ XOR (r[rs2] \text{ or } \text{sign extnd(simm13)}) \)

Assembler
Syntax:  \text{wr reg}_{rs1}, \text{reg_or_imm}, \%y

Description:  WRY does a bitwise logical XOR of the contents of register \( r[rs1] \) with either the contents of \( r[rs2] \) (if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \( i=1 \)). The result is written into the Y register.

WRY is a delayed-write instruction:
1. If any of the three instructions following a WRY is a MULSc or a RDY, the value of Y used is unpredictable.
2. If any of the three instructions after a WRY instruction reads the modified Y register, the value read is unpredictable.
3. If any of the three instructions after a WRY is trapped, a subsequent RDY in the trap handler will get the register’s new value.

Traps: none

Format:

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 28 & 25 & 24 & 18 & 14 \\
1 & 0 & \text{ignored} & 1 & 1 & 0 & 0 & 0 \\
\end{array}
\begin{array}{cccc}
13 & 12 & 5 & 4 & 0 \\
\text{rs1} & \text{i=0} & \text{ignored} & \text{rs2} \\
\end{array}
\]

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 28 & 25 & 24 & 18 & 14 \\
1 & 0 & \text{ignored} & 1 & 1 & 0 & 0 & 0 \\
\end{array}
\begin{array}{cccc}
13 & 12 & 5 & 4 & 0 \\
\text{rs1} & \text{i=1} & \text{simm13} \\
\end{array}
\]
XNOR

Exclusive-Nor

Description:
This instruction does a bitwise logical XOR of the contents of register r[rs1] with the one’s complement of either the contents of r[rs2] (if bit field i=0) or the 13-bit sign-extended immediate value contained in the instruction (if bit field i=1). The result is stored in register r[rd].

Traps: none

Format:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
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<th>18</th>
<th>14</th>
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<tbody>
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<td>0</td>
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<td>1</td>
<td>1</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>1</td>
<td>1</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
</tr>
</tbody>
</table>
```
**XNORcc**

**Operation:**
\[
\begin{align*}
    r[rd] &\leftarrow r[rs1] \quad \text{XOR} \quad \text{not}(r[rs2] \text{ or sign extnd(simm13)}) \\
    n &\leftarrow r[rd]<31> \\
    z &\leftarrow \text{if } r[rd] = 0 \text{ then } 1, \text{ else } 0 \\
    v &\leftarrow 0 \\
    c &\leftarrow 0
\end{align*}
\]

**Assembler Syntax:**
\[
\text{xnorcc } \text{reg}_{rs1}, \text{ reg}_{or\_imm}, \text{ reg}_{rd}
\]

**Description:**
This instruction does a bitwise logical XOR of the contents of register \(r[rs1]\) with the one's complement of either the contents of \(r[rs2]\) (if bit field \(i=0\)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \(i=1\)). The result is stored in register \(r[rd]\). XNORcc also modifies all the integer condition codes in the manner described above.

**Traps:**
none

**Format:**

```
\begin{array}{cccccccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 0 & \text{rd} & \text{0 1 0 1 1 1} & \text{rs1} & \text{i=0} & \text{ignored} & \text{rs2} \\
\end{array}
```

```
\begin{array}{cccccccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 0 & \text{rd} & \text{0 1 0 1 1 1} & \text{rs1} & \text{i=1} & \text{simm13} \\
\end{array}
```
XOR

Operation: \( r[rd] \leftarrow r[rs1] \text{ XOR } (r[rs2] \text{ or sign extnd(simm13)}) \)

Assembler Syntax: \( \text{xor reg}_{rs1}, \text{reg}_{or\_imm}, \text{reg}_{rd} \)

Description: This instruction does a bitwise logical XOR of the contents of register \( r[rs1] \) with either the contents of \( r[rs2] \) (if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \( i=1 \)). The result is stored in register \( r[rd] \).

Traps: none

Format:

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 0 & \text{rd} & 0 & 0 & 0 & 0 & 1 & 1 & \text{rs1} & i=0 & \text{ignored} & \text{rs2} \\
1 & 0 & \text{rd} & 0 & 0 & 0 & 0 & 1 & 1 & \text{rs1} & i=1 & \text{simm13} & \\
\end{array}
\]
**XORcc**  
Exclusive-Or and modify icc  

**Operation:**
\[ r[rd] \leftarrow r[rs1] \text{ XOR } (r[rs2] \text{ or sign extnd(simm13)}) \]

- \( n \leftarrow r[rd] < 31 > \)
- \( z \leftarrow \text{ if } r[rd]=0 \text{ then } 1, \text{ else } 0 \)
- \( v \leftarrow 0 \)
- \( c \leftarrow 0 \)

**Assembler Syntax:**
\[ \text{xorcc reg}_{rs1}, \text{ reg_or_imm}, \text{ reg}_{rd} \]

**Description:**
This instruction does a bitwise logical XOR of the contents of register \( r[rs1] \) with either the contents of \( r[rs2] \) (if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \( i=1 \)). The result is stored in register \( r[rd] \). XORcc also modifies all the integer condition codes in the manner described above.

**Traps:**
none

**Format:**

\[
\begin{array}{cccccccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
\hline
1 & 0 & & & & \text{rd} & 0 & 1 & 0 & 0 & 1 & 1 & \text{rs1} & \text{i=0} & \text{ignored} & \text{rs2} \\
\end{array}
\]

\[
\begin{array}{cccccccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 0 \\
\hline
1 & 0 & & & & \text{rd} & 0 & 1 & 0 & 0 & 1 & 1 & \text{rs1} & \text{i=1} & \text{simm13} & \\
\end{array}
\]