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IMEC ASIC SERVICES

ESA : 15th Feb 2010

Danny Lambrichts

Outline

General FM procurement

FM qualification of a Dare 180 nm Mixed signal Asic

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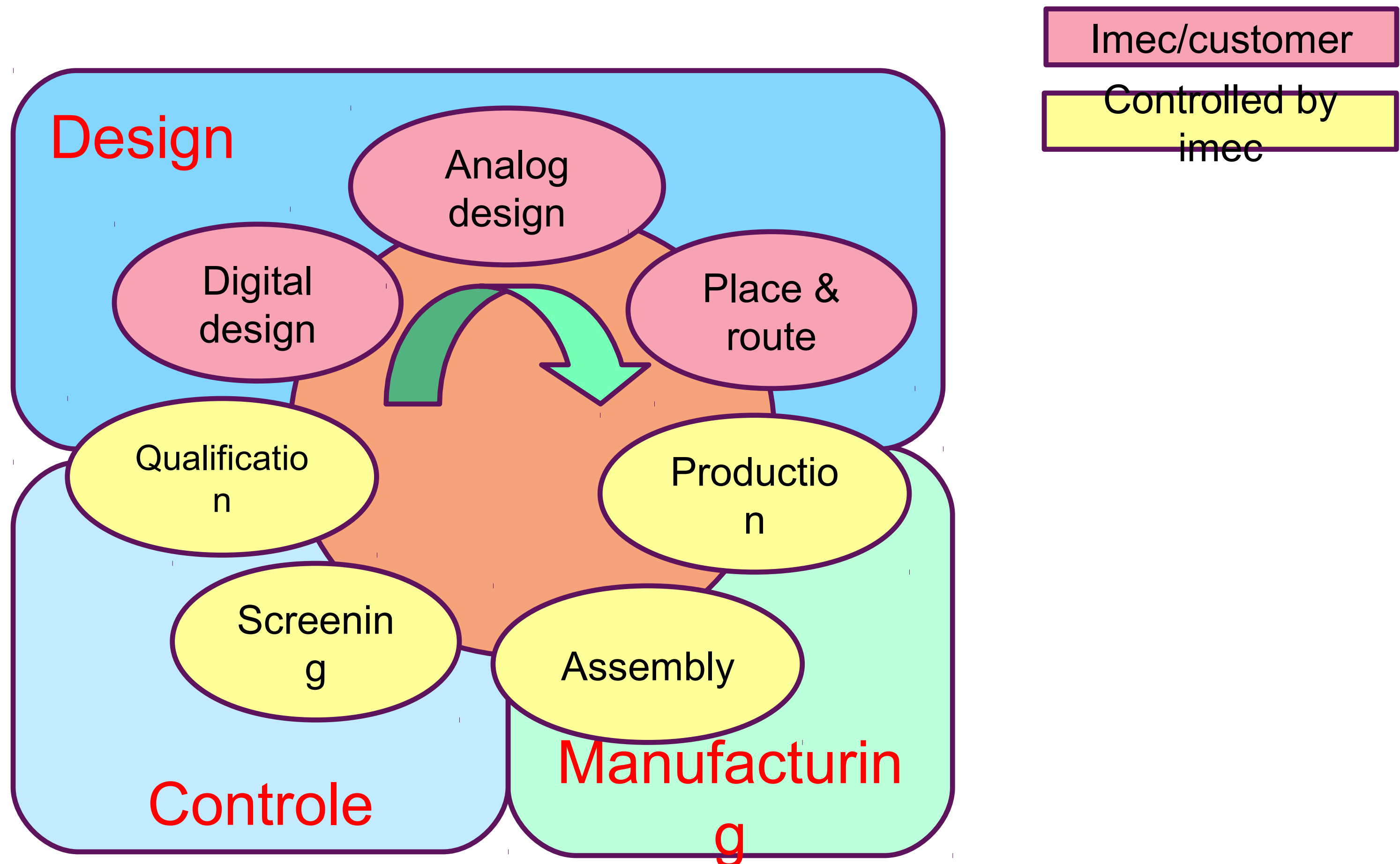
General FM ProcurEment flow



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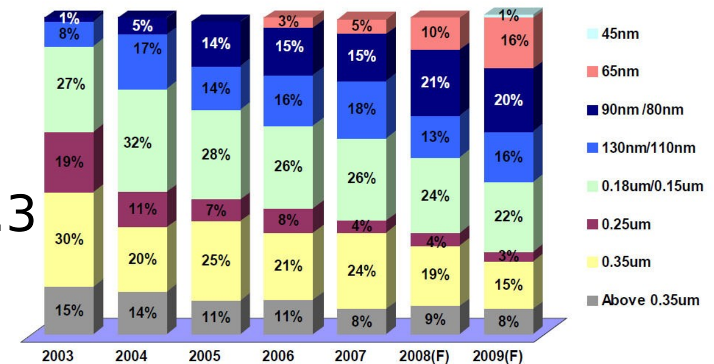
Subcontractors

Wafer production

- UMC
- Standard CMOS process, 8” wafers
- UMC 018um Logic GII 1P6M 1.8V/3.3



Assembly

- Package development – KYOCERA
- Assembly – HCM

Test solution

- Microtest – Italy

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Subcontractors

Qualification

- HCM - Assembly
- Microtest – Electrical tests/HTOL
- Maser Engineering – environmental tests
- Maprad - Radiation tests

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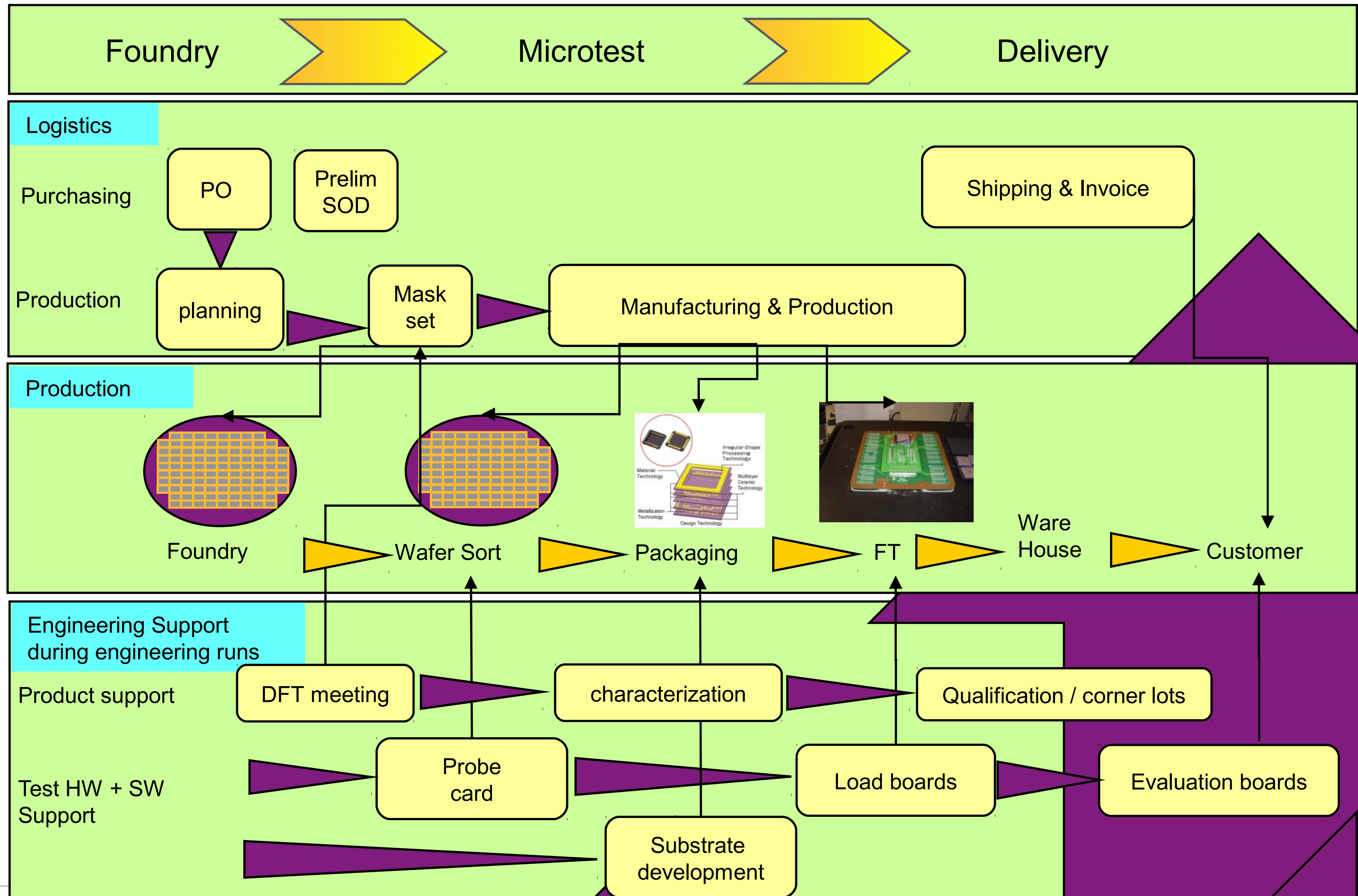
ASIC Supply flow : From foundry to packaged and tested parts



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Outline

General FM procurement

FM qualification of a Dare 180 nm Mixed signal Asic

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FM qualification of a dare 180 NM Mixed signal asic

Prototyping/ FM Production service

Assembly service

Test service

FM qualification according to ESCC9000

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FM qualification of a dare 180 NM Mixed signal asic

Prototyping/ FM Production service

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Test service

FM qualification according to ESCC9000

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Prototyping / FM production

Prototyping possible via MPW runs

- Proof the ASIC functionality
- First characterization
- Possible fine tuning of the ASIC performance
- Limited number of packaged samples
- Low cost

FM production only with dedicated runs

- Dedicated mask set
- Engineering run of 12 wafers
- High NRE cost

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FM qualification of a dare 180 NM Mixed signal asic

Prototyping service

Assembly service

Test service

FM qualification according to ESCC9000

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Assembly service

FM need Ceramic packages

- Sub-contractors
- Kyocera – tooling of dedicated packages
- HCM - assembly
- Different options
- Open tool package – very limited
- Customized package

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Ceramic packages: open tool – prototyping

- Large range of open tool packages
  - CLCC, JLCC, CQFP
  - CPGA, SOIC
  - DIL
- Advantage
  - NO NRE cost involved
  - Short Lead time – in stock
- Disadvantage
  - Fixed number of pins
  - Fixed cavity size
  - Fixed layout of the pin routing
  - NOT always possible to be used for FM

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Ceramic packages: customized

- Advantage
- Dedicated package
- Flexibility in # layers for pin routing
  - Reduce the capacitance
  - Signal shielding, ground shielding
- Space qualification
  - Top brazed leads
  - Specific lead bending
- Disadvantage
- NRE cost involved
  - Package tooling cost
  - Development of specific trays
- Long production time – 11 weeks

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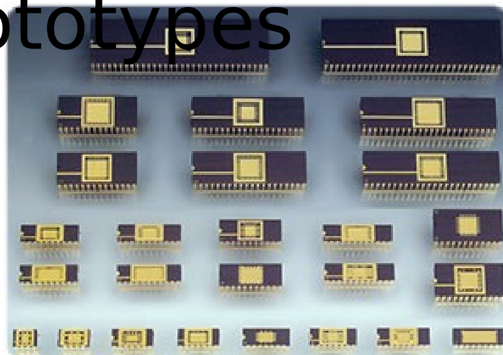
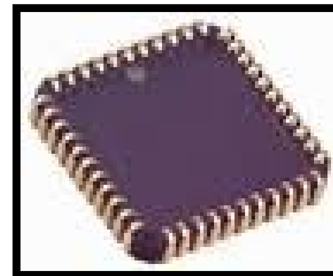
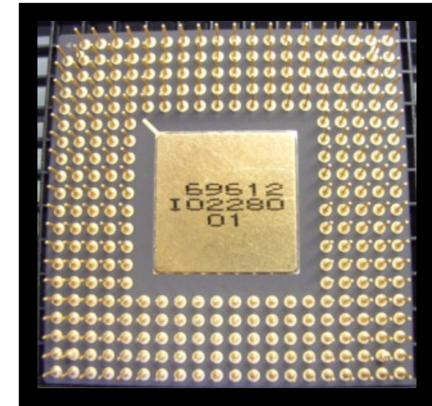
Ceramic Assembly examples

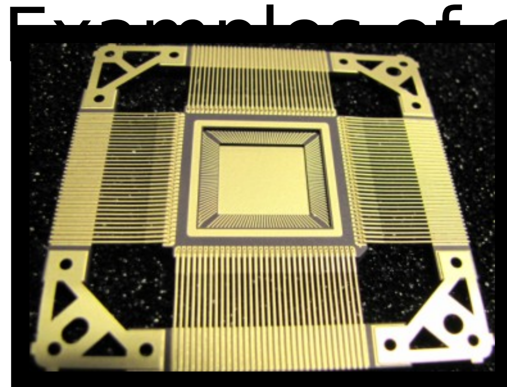
Examples of open tool packages - prototypes

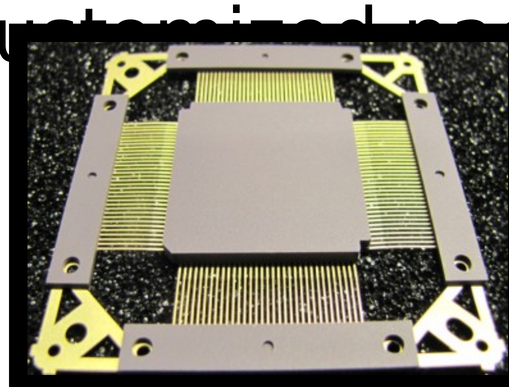


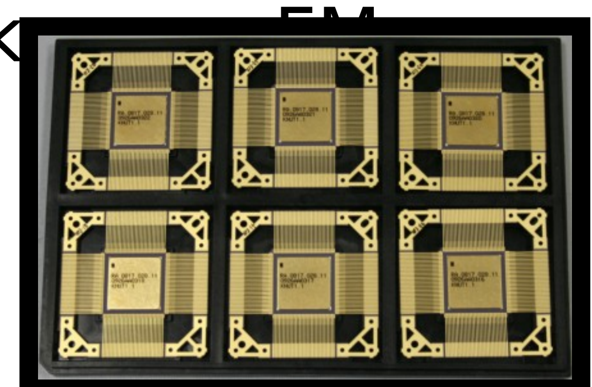




Examples of customized pack EM







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Dedicated package
DEVELOPED BY KYOCERA

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DedicaTED SOCKET DEVELOPED BY MICROTEST

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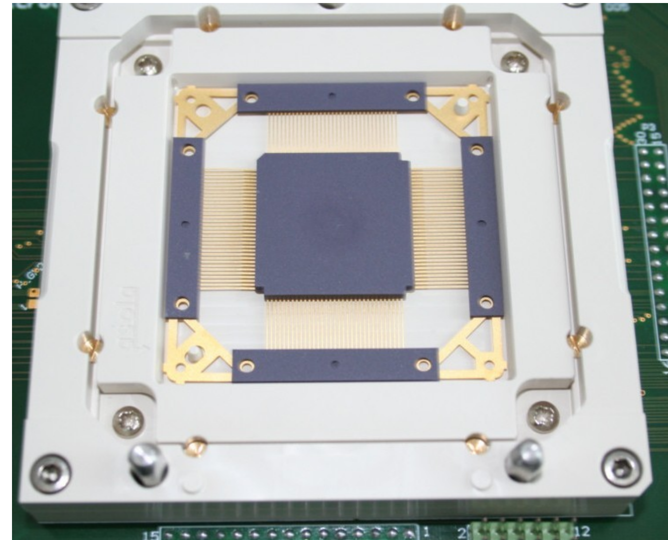

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FM qualification of a dare 180 NM Mixed signal asic

Prototyping

Assembly

Test service

FM qualification according to ESCC9000

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test service

- Test facility and capabilities
- Test flow
- Failure Analysis

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Test facility and capabilities

- Imec is using Microtest (Altopascio – Italy) as test house
- Focused on engineering, support and knowledge
  - Pure Digital
  - Mixed signal
  - RF
- Highly educated engineers
- High flexibility
- Time to market
- Volume test activities (< 1kk/yr)

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Test facility and capabilities

- Available tester platforms
- Teradyne J750 (digital + source digitizer AWG)
- Teradyne A565 – 10 Amps/supply
- Teradyne Microflex, Integraflex (RF option)
- Portable test system – Hatina (Rad tests)
- Clean room area
- Wafer sort
- Nitrogen storage
- Reliability tests
- HTOL oven
- Thermostream

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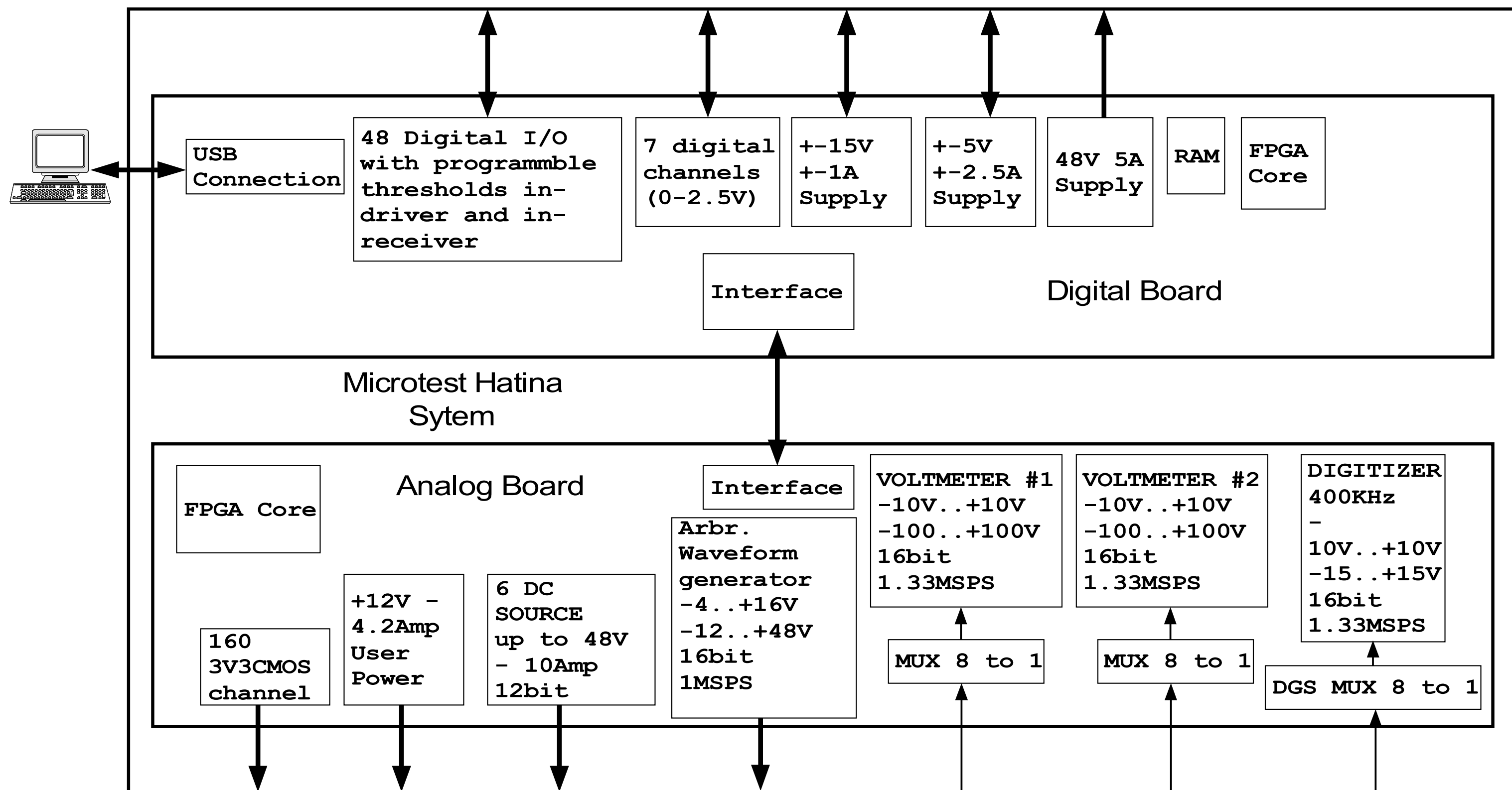
HATINA TESTSYSTEM

- 64 Kb memory/channel
- 40Mhz data rate
- AWG (1MSPS – 16 bit), Digitizer (400 Khz)



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Test facility and capabilities

Hatina

Teradyne I-flex

Teradyne Microflex

Robot handler

Wafer sort - Cleanroom

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test service

- Test facility and capabilities
- Test flow
- Failure Analysis

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Test flow

- Preparation of test solution
- Design For Test
- Test HW/SW development

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Test flow

- Preparation of test solution
- Design For Test
- Test HW/SW development

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preparation Test solution

- Evaluation of ASIC test spec
- Customer needs to provide detailed ASIC test spec
- If no ASIC test spec available
  - Meeting with customer to define high level test spec
  - Optional: Microtest can generate asic test spec
- KO meeting
- 2-days meeting
- Detailed discussion of all SW to be developed
  - Preliminary Test list doc
  - Parameters to be tested
- Definition of tester platform
  - Discussion of HW to be developed
- Time schedule

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preparation Test solution

- Final quote for test solution
  - Packaged devices
    - Test program + hardware
    - Prototype debug activities
  - Wafer level
    - Probe-card
    - Electrical wafer sort debug activities

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Test flow

- Preparation of test solution
- Design For Test
- Test HW/SW development

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Design for Test

On chip: extra logic, to improve testability

Advantages

- Increases accessibility
- Decreasing test time
- Reduces number of test vectors & test time

Disadvantages

- Area overhead (allowed 10% DfT area)

Examples

- Scan chains: Use of specific scan Flip-flops
- BIST: specific circuits for memories and logic
- Stimuli + Response generated on chip

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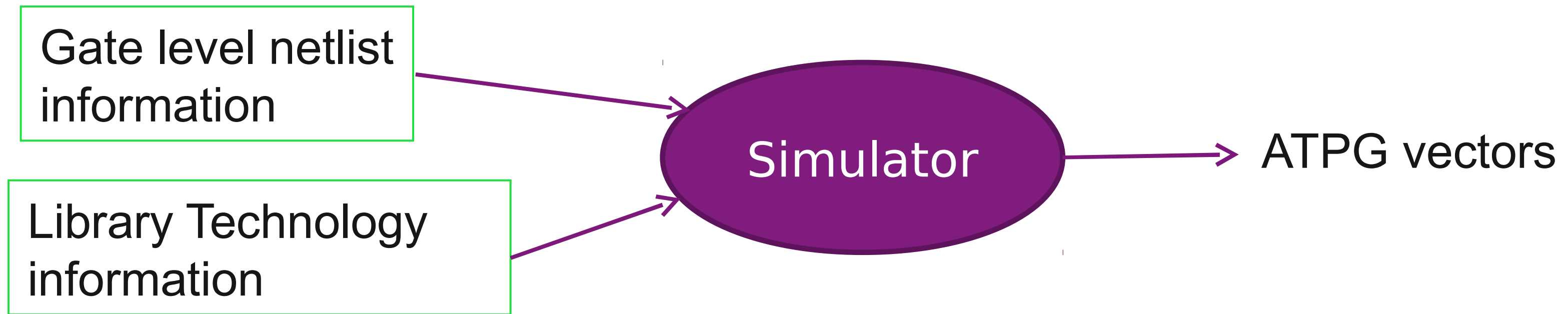
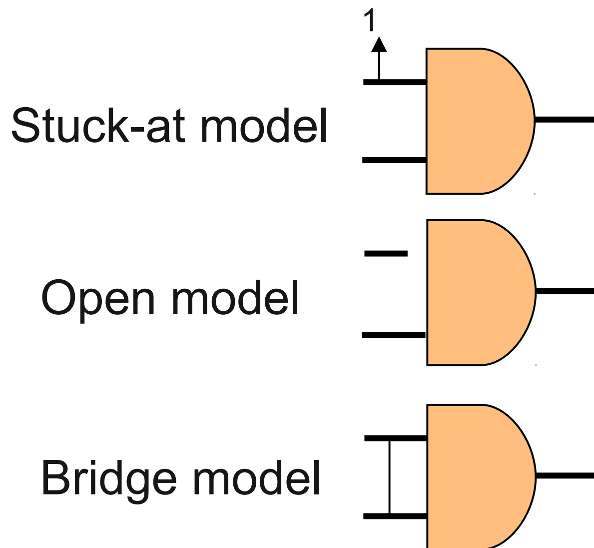
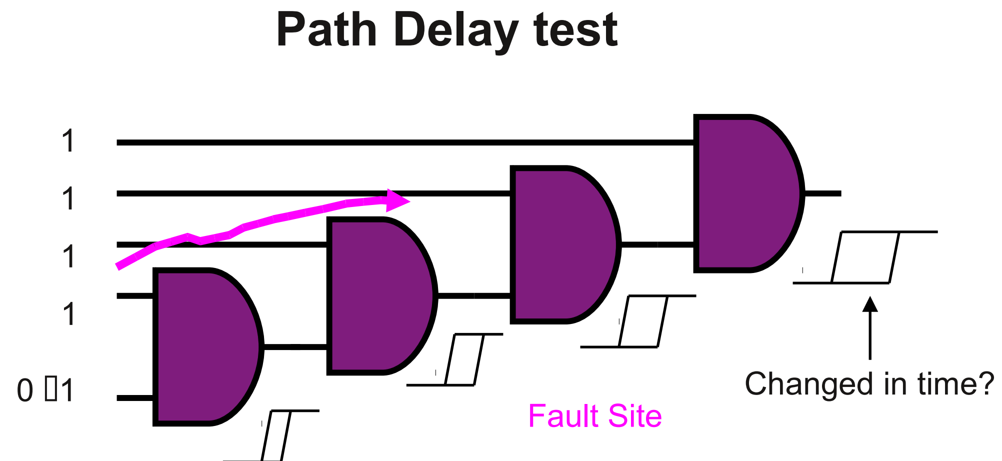
Test implementation



Example of fault models





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TEST IMPLEMENTATION

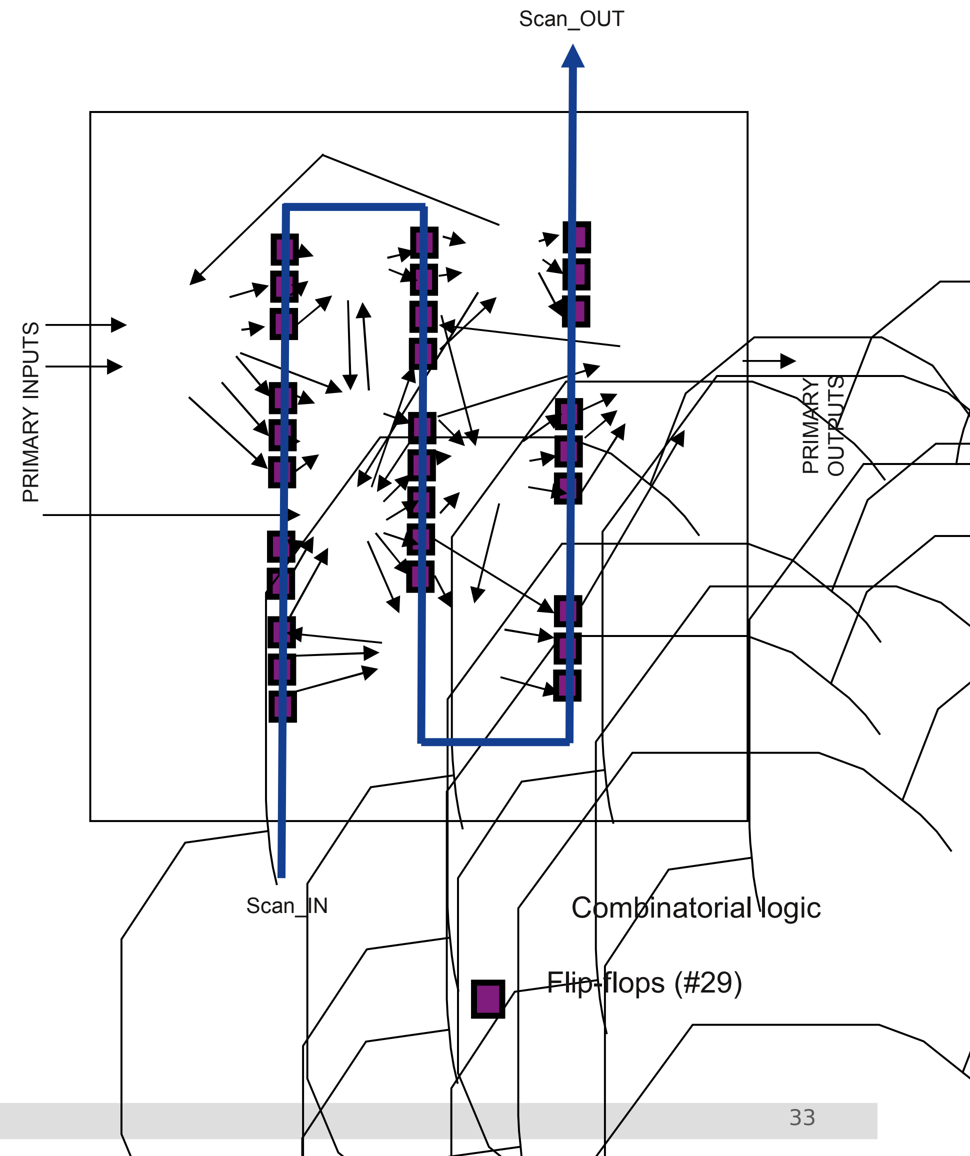
Scan chains

**In test mode **

FFs connected as shift register

Procedure:

1. Test mode Shift in a pattern
2. Normal mode Clock once
3. Test mode Shift out the results
   - Meanwhile shift in new pattern



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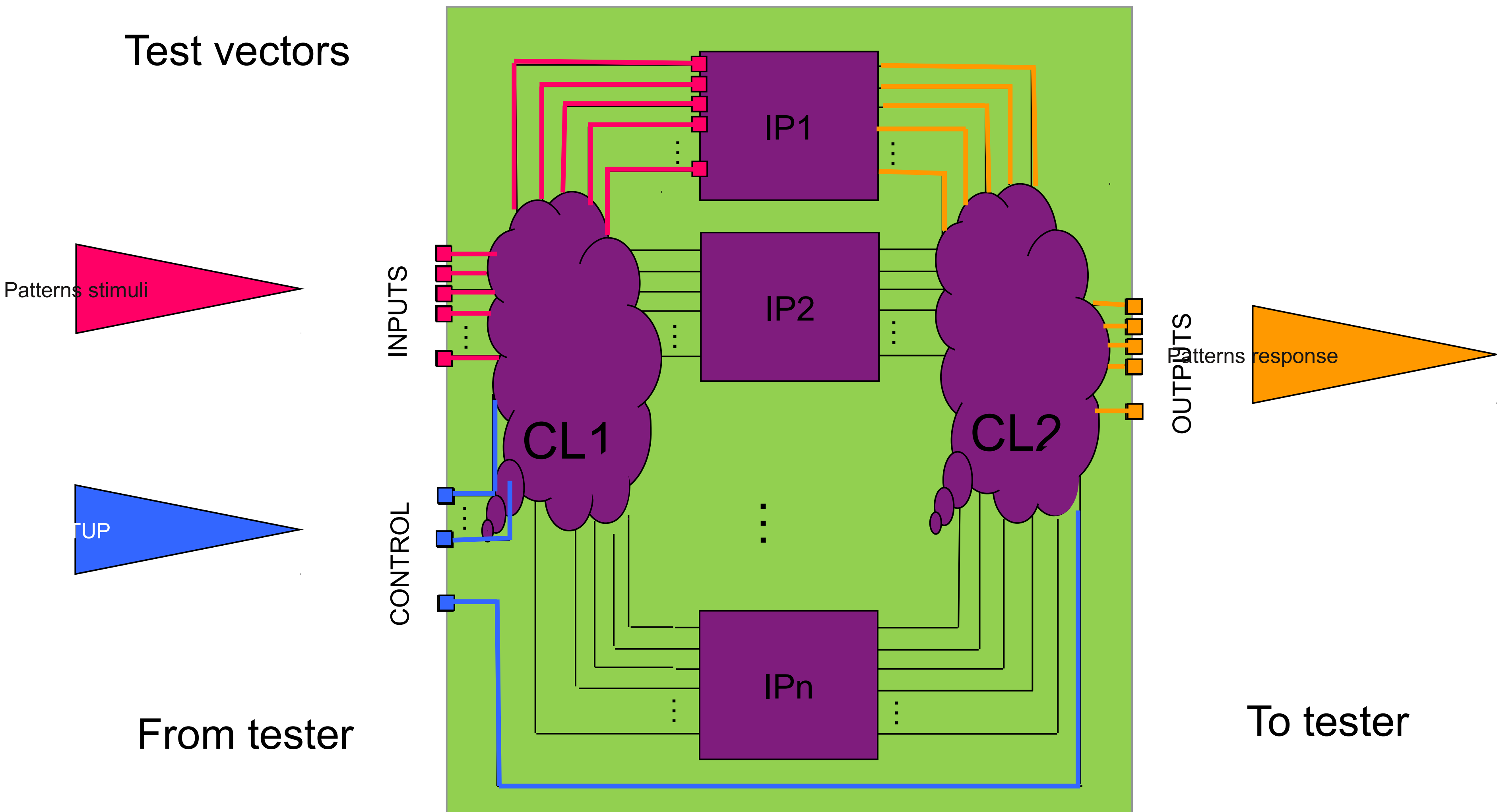
Test implementation



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Test flow

- Preparation of test solution
- Design For Test
- Test HW/SW development

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Test HW and sw development

- HW development for Final test / Wafer sort
- Schematic entry/layout of load boards
- Manufacturing of load boards (rider board/ large board)
- SW development off-line
- Test pattern conversion
- Test pattern generation
  - Dedicated test routines for analog tests
- SW development on-line
- Debug of ASIC
- ASIC characterization
- ESD & LU tests
- Characterization on 30 samples
- Data logs, data correlation, Final definition test windows

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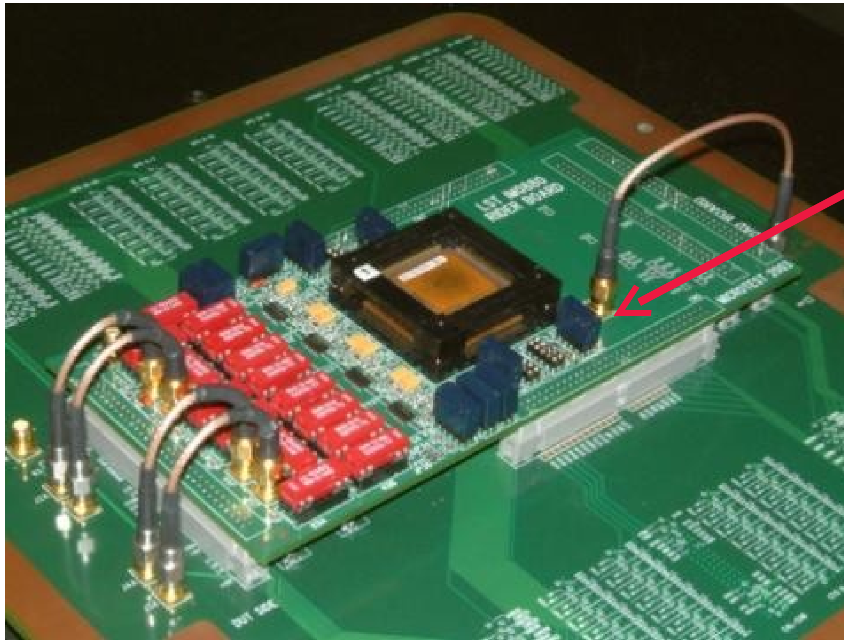
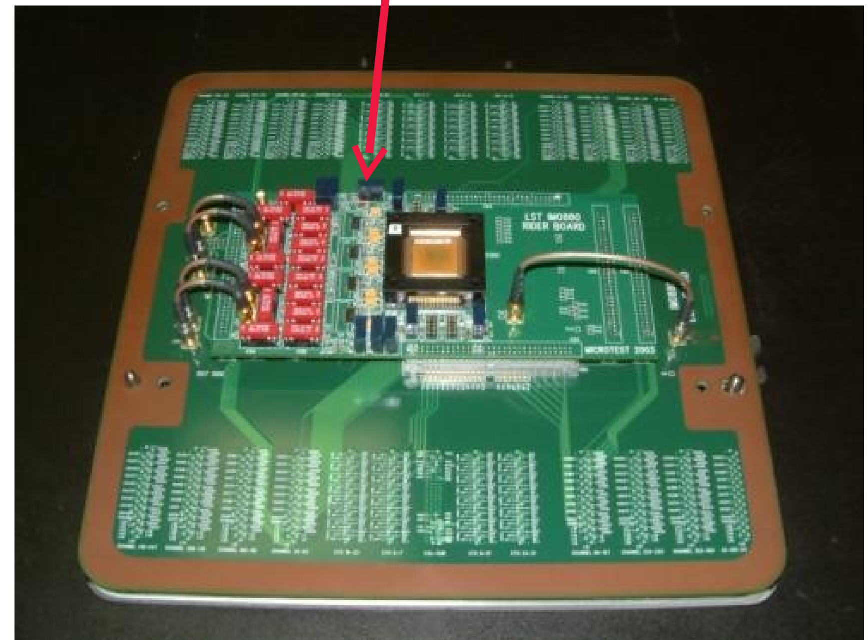
Small Test boards

- Example of LOW cost rider boards



Rider board with external components



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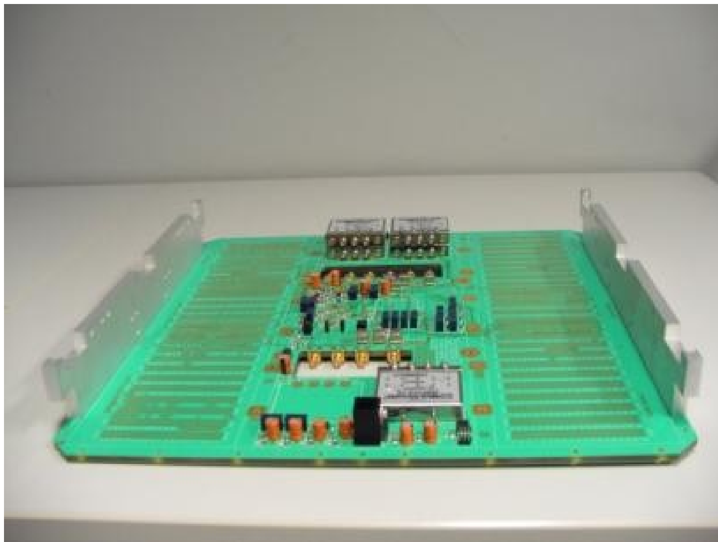
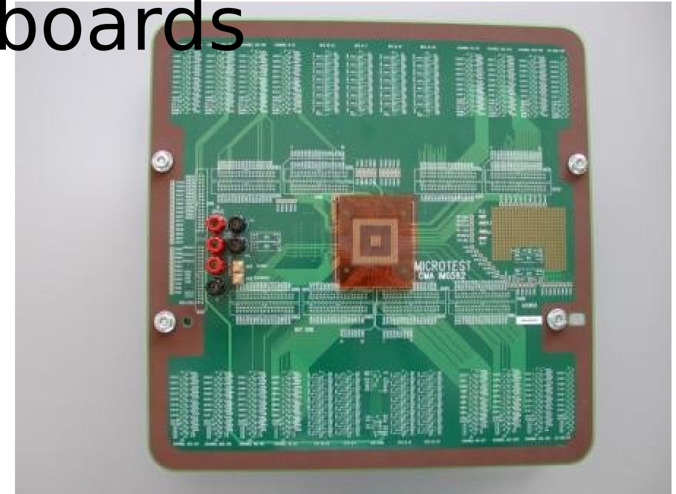
Large Test boards

Large dedicated test boards





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Wafer probing

Remove bad dies in early manufacturing stage

- Advantage Save packaging cost
- Failure due to functionality (electrical) or processing

Resources

- Tester & Test program
- Through channel stimuli & compare with expected response
- Generates data logs for analysis
- Binning; Classify the error VS test type
- Probe card
- interface between die and tester channels

Test flow

- Bad dies Inked for identification + Wafer maps
- Good dies After sawing packaging

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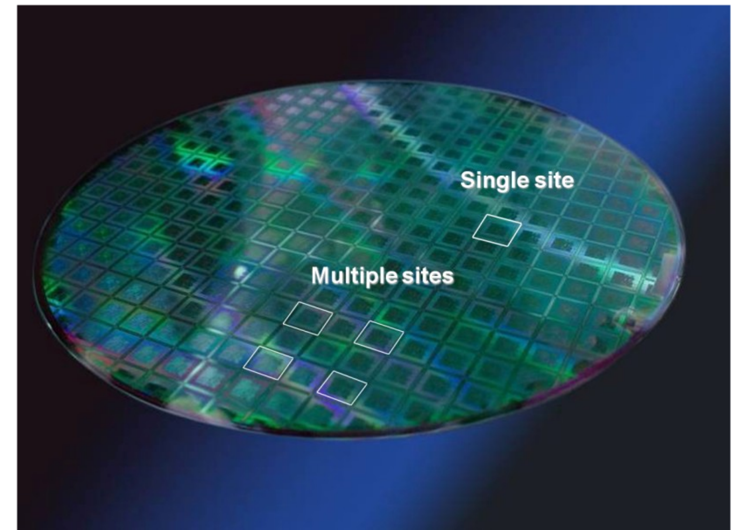
Wafer probe cards

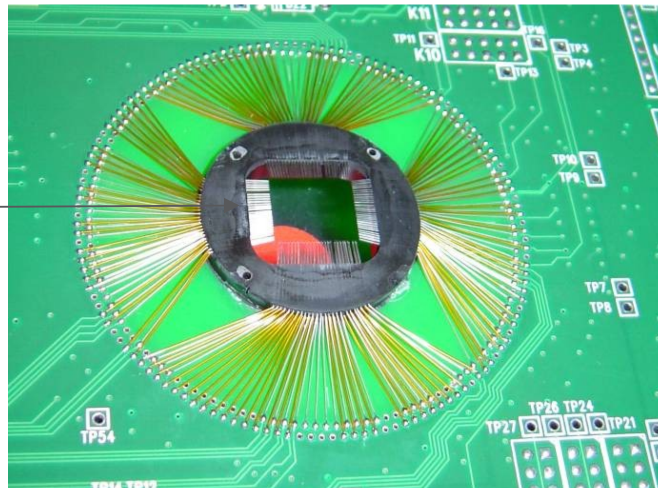
Probe cards

Wafer



Connection to tester channels

Needles to probe on the die(s)



(Courtesy of Microtest)

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asic test service

- Test facility and capabilities
- Test flow
- Failure Analysis

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Failure analysis

- Subcontractor Maser Engineering
- Offered services:
- Decapsulation
- SEM, SAM, X-ray, EMI imaging
- Bond pull test
- Die shear
- Plasma etching
- Probe bench & curve tracer…….

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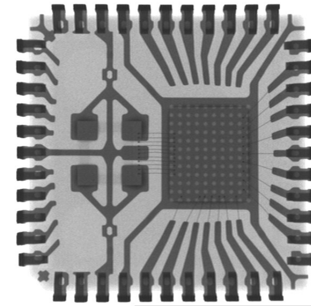
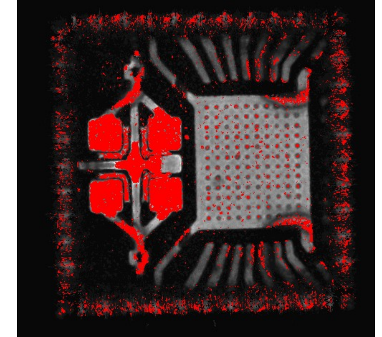
Failure analysis

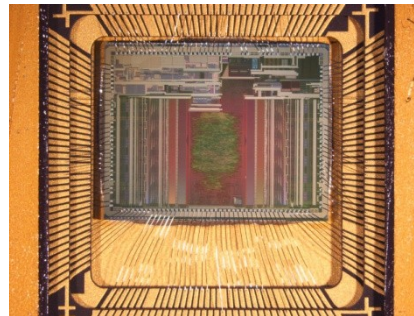
Non destructive analysis

- X-ray microscopy

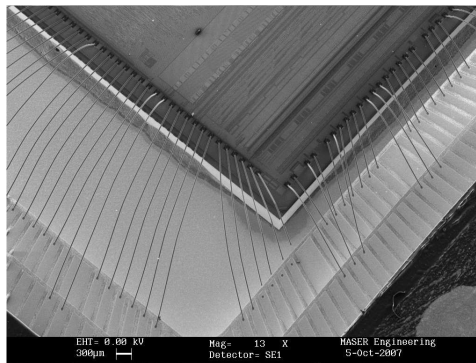


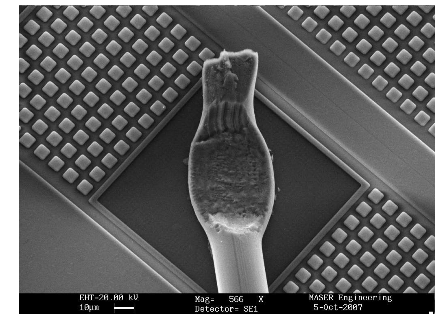


- Scanning Acoustic Microscopy (SAM/SCAT)
- Visual inspection



- SEM





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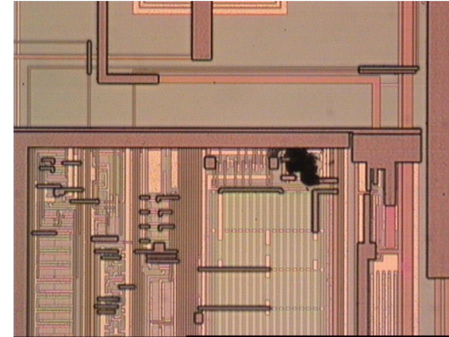
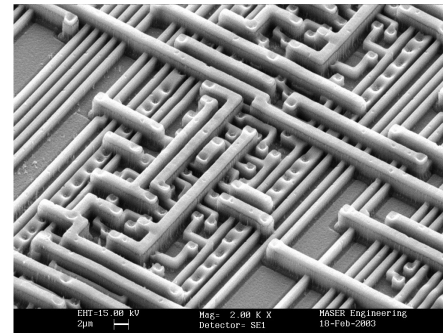
Failure analysis

Liquid Crystal

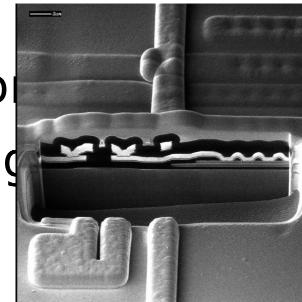


Construction analysis



Focused Ion Beam

- Fib assist etching and depositio
- Side specific cross section, imag



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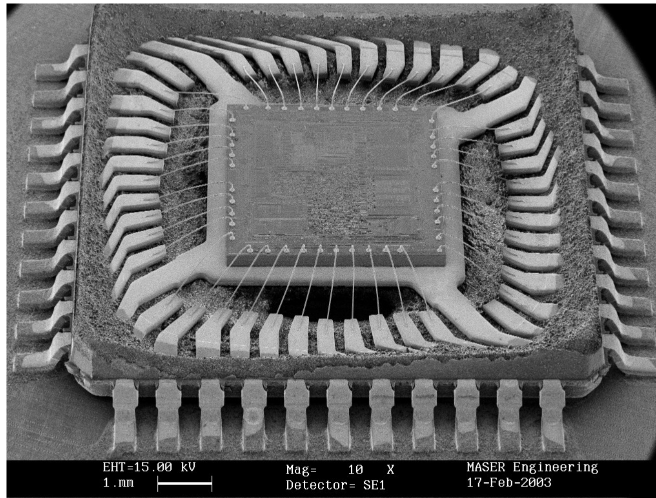
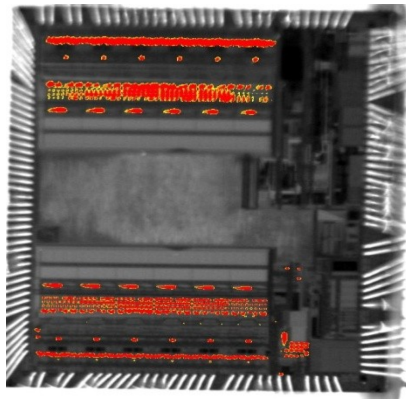
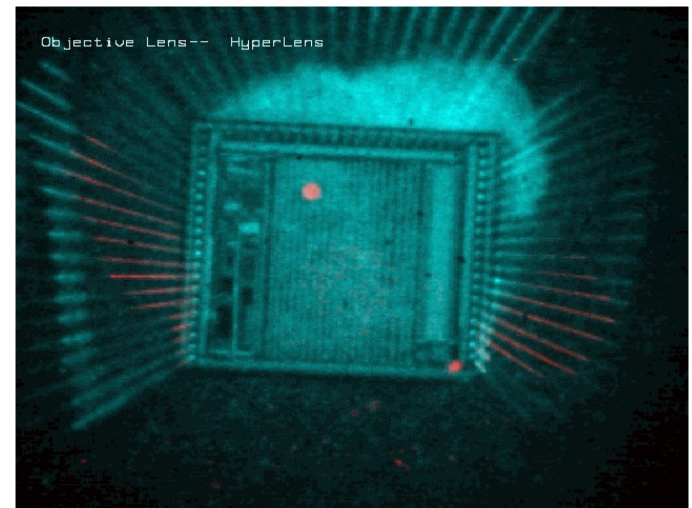
Failure analysis



Decapsulation
of
plastic packages



EMI imaging



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FM qualification of a dare 180 NM Mixed signal asic

Prototyping

Assembly

Test service

FM qualification according to ESCC9000

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subcontractors

- Test house
- Microtest – Italy

- Assembly
- Tooling of Ceramic packages: Kyocera
- Assembly: HCM – France

- Reliability tests
- Maser Engineering – The Netherlands

- Radiation tests
- supported by Maprad – Italy
  - SEE tests : INFN facility - Catania
  - Tid tests: LLN, Turkye

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Space qualification flow – ESCC9000

- Production Control – Chart F2
- Screening tests – Chart F3
- Lot Validation Testing (Qualification) – Chart F4
- Delivery Flight Modules (only Chart F2 &3)

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Space qualification flow – ESCC9000

- Production Control – Chart F2
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- Delivery Flight Modules (only Chart F2 &3)

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Detailed ESCC9000 flow

- Production Control – Chart F2
  - Internal Visual inspection
  - Bond strength, die shear
  - Encapsulation, serialization
  - Dimension check, weight
- SEM: Scanning Electron Microscope
- PVM review

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Electrical WAFER SORT

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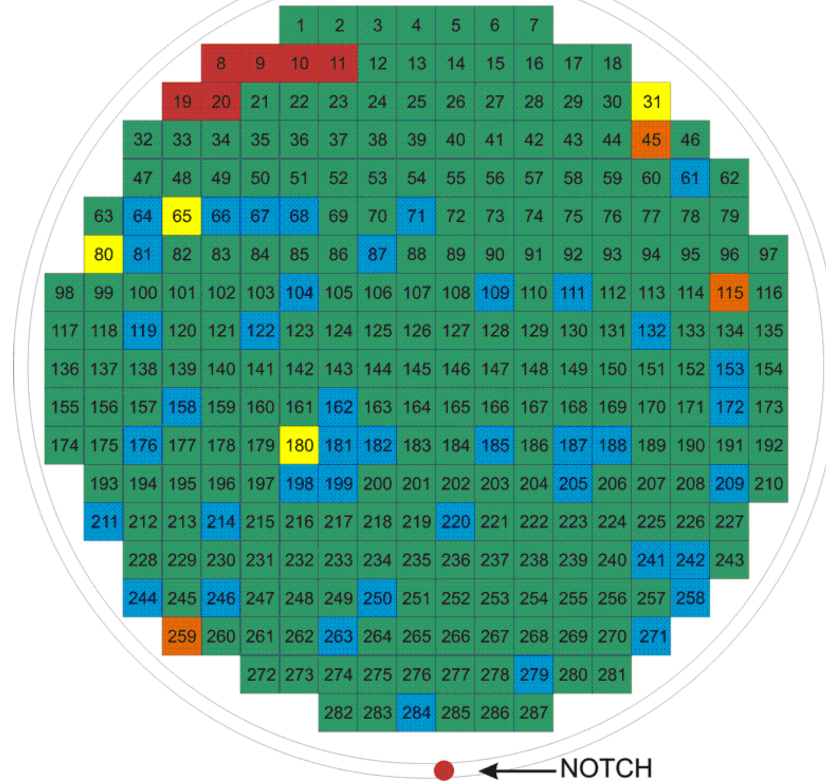

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Chart F2 - SEM

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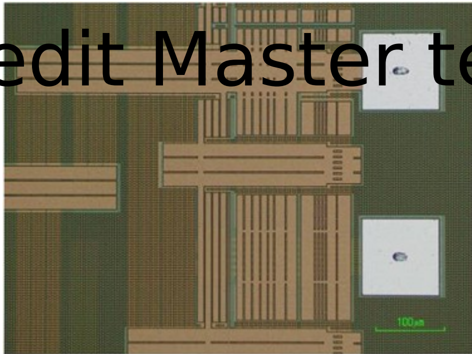

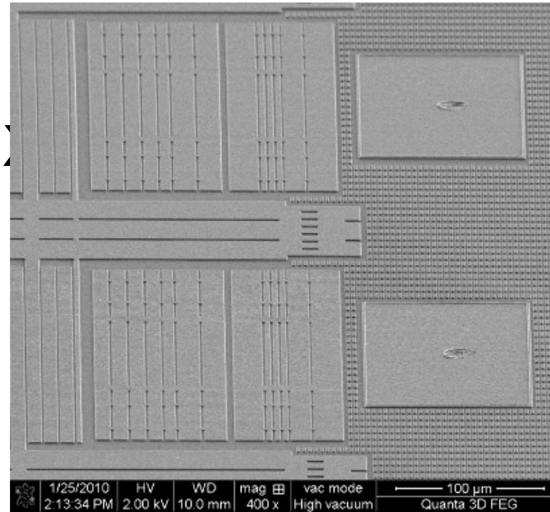

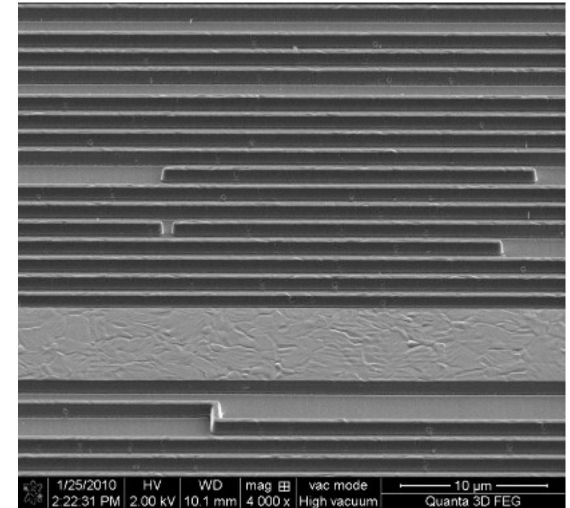

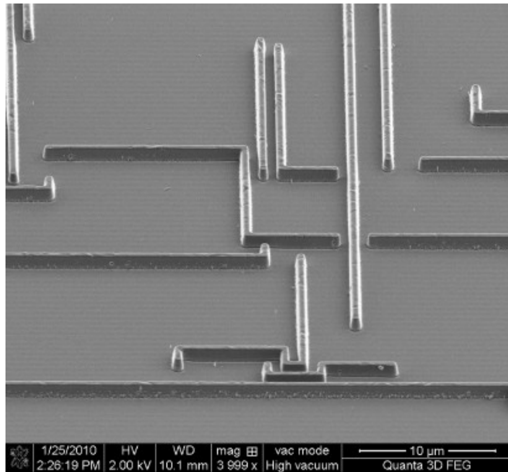

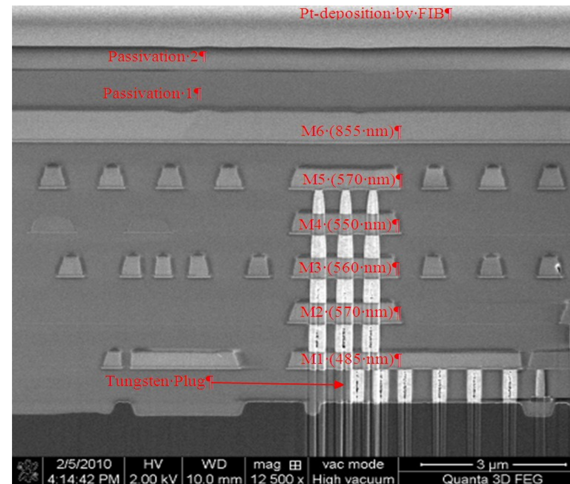

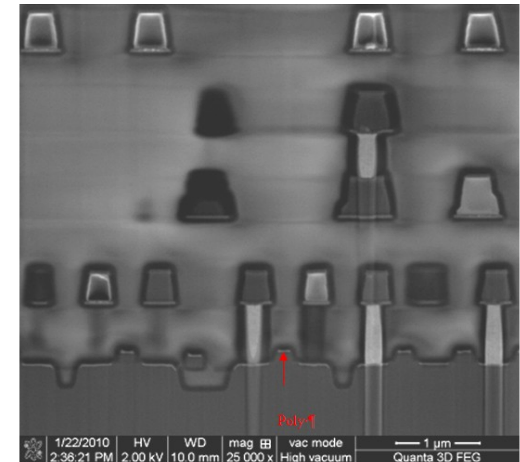

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Space qualification flow – ESCC9000

- Production Control – Chart F2
- Screening tests – Chart F3
- Lot Validation Testing (Qualification) – Chart F4
- Delivery Flight Modules (only Chart F2 &3)

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Detailed ESCC9000 flow

- Screening tests – Chart F3
- Electrical test @ HT, RT, LT
  - HTS (24 hrs @ 150 degrees)
  - TCT (-65/150 degrees, 10 cycles)
  - PIND (MIL STD-883, meth 2020, cond A)
- Functional test @ HT, RT, LT – Parameter Drift Analysis
  - Power Burn-in (240 hrs @ 125 degrees)
- Functional test @ HT, RT, LT - Parameter Drift Analysis
  - Fine & gross leak
  - Ext Vis inspection
  - Solderability

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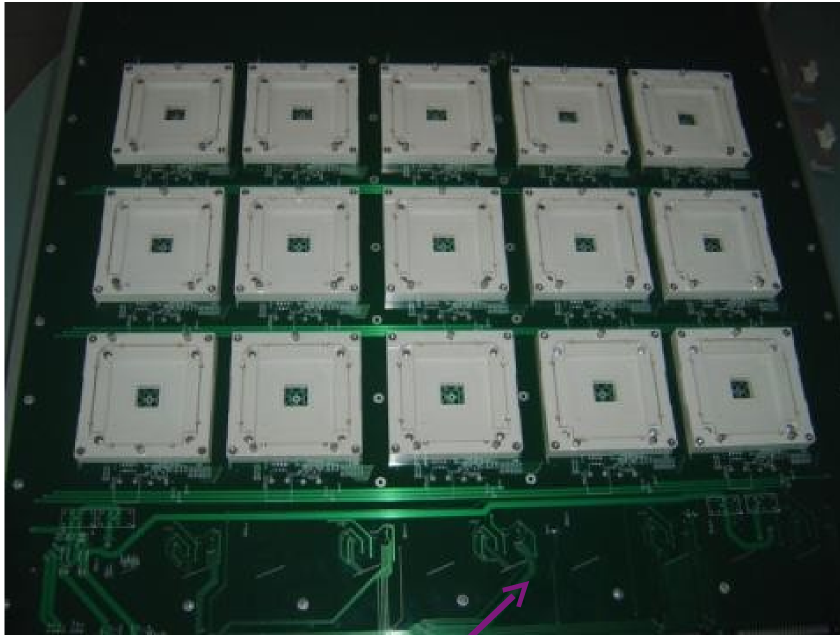
HTOL/Power Burn-in hardware



Top side

Bottom side,
External comp's
@RT

Burn-in
oven

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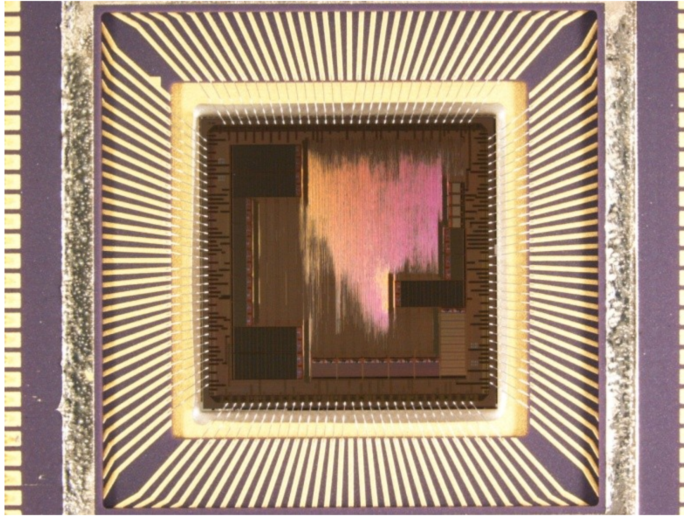
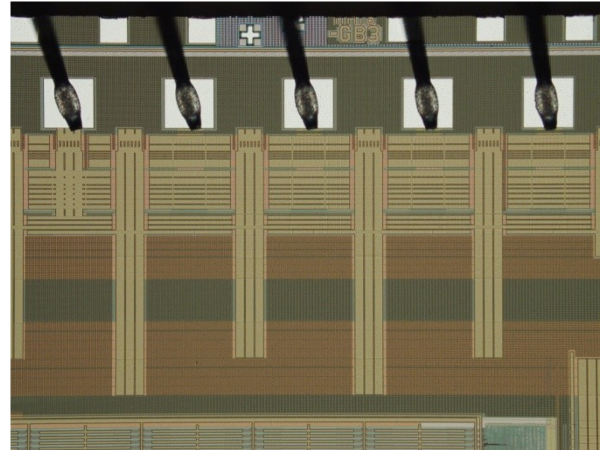
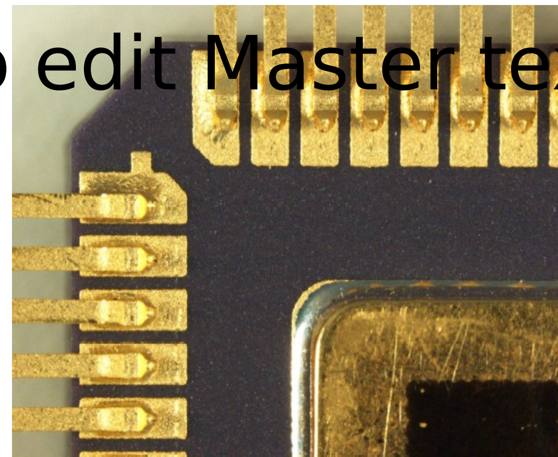
Ext/int Visual inspection







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Space qualification flow – ESCC9000

- Production Control – Chart F2
- Screening tests – Chart F3
- Lot Validation Testing (Qualification) – Chart F4
- Delivery Flight Modules (only Chart F2 &3)

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Detailed ESCC9000 flow

- Lot Validation testing – Chart F4
- Endurance test 1, on 15 devices
  - HTOL – 2000 hrs, with intermediate tests @500, 1000 hrs
  - Fine & gross leak
  - Test @RT, HT, LT- Ext Visp
- Environmental test 1, 15 devices
  - Mechanical shock, Vibration
  - Constant acceleration, fine& gross leak
  - Test @RT, EXT visp
- Environmental test 2, 15 devices
  - Thermal shock
  - Moisture resistance
  - Fine & gross leak,
  - Test @RT, Ext Vis Insp

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Detailed ESCC9000 flow

- Assembly tests
  - Permanence of marking
  - Terminal strength, Internal Visp
  - Die shear
  - bond pull, bond shear
- Rad test boards
  - Tid tests (Total Ionizing Dose)
    - Tid test board
    - Func test board on Hatina test system
  - SEE tests (Single Event Effects)
    - SEE test board (3 sockets)
    - Func test board on Hatina test system

HTOL – 2000 hrs

Dedicated burn in oven (Microtest)

- External components @ RT
- FM @ 125 degrees
- ASIC is running
- Functional mode
- Data log of some sig

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Radiation tests -tid

Example of test plan (5krad/hr)

- Irradiation
- Irradiation up to 50 krad
  - intermediate test @RT
- Irradiation up to 100 krad
  - intermediate test @RT
- ....
- Irradiation up to 300 krad
  - intermediate test @RT

- Annealing of 24 hrs @ RT
- Aging of 168 hrs @ 100 degrees

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Radiation tests - Tid

- Some pictures of Tid test set-up

Dosimeters

Tid load board, 10 devices

Intermediate test set-up, Hatina

Radiation tests - SEE

Example of test plan (3 devices)

- Total irradiation up to 107 Ions/cm2
- rate ranging from 103 Ions/s cm2 up to 104 Ions/s cm2
- Func testpatterns running under control of [illegible]atina test system

Ion	Kinetic Energy/nuc. (MeV)	Angle (deg)	Air (cm)	Range (µm)	LET (MeV/mg/cm^2)
Ne-20	20	0	10	430	3.55
Ar-40	20	0	20	222	11
Kr-84	20	0	20	108	32.3
Kr-84	20	60	15	75	61.4
Xe-129	20	60	15	63	100.7

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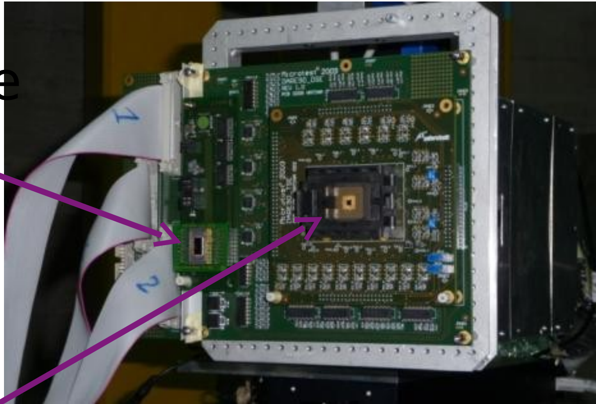
Radiation tests - SEE

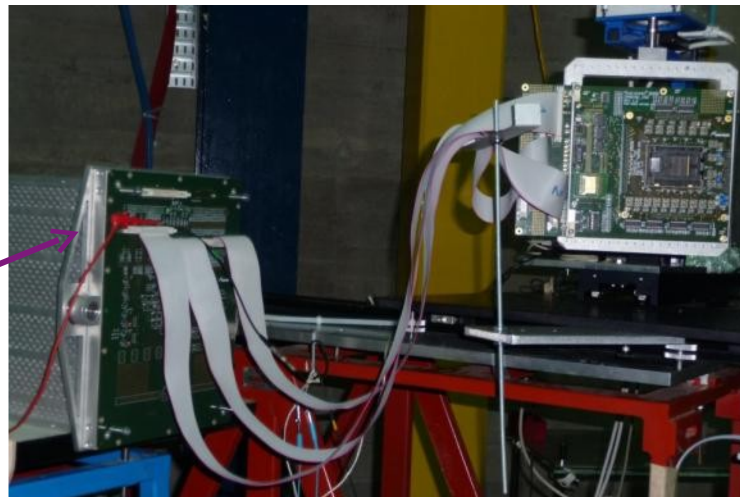
- Some pictures of SEE test-up

ESA reference device



DUT

Beam alignment



Hatina test set-up

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Space qualification flow – ESCC9000

- Production Control – Chart F2
- Screening tests – Chart F3
- Lot Validation Testing (Qualification) – Chart F4
- Delivery Flight Modules (only Chart F2 &3)

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FM's delivery

All devices for FM's will be screened

- Assembly according chart F2
- Electrical test and reliability tests according to chart F3.

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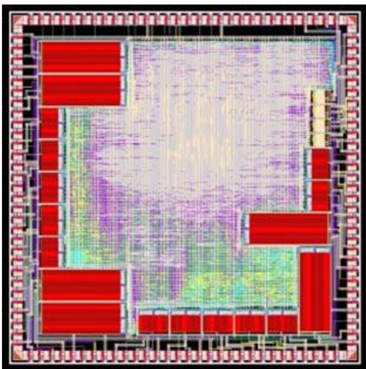
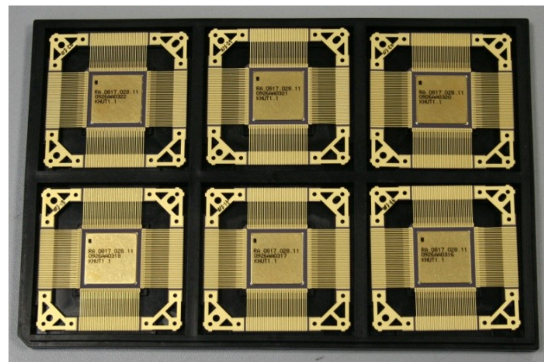
Imec delivers 43 FM'S for tesat

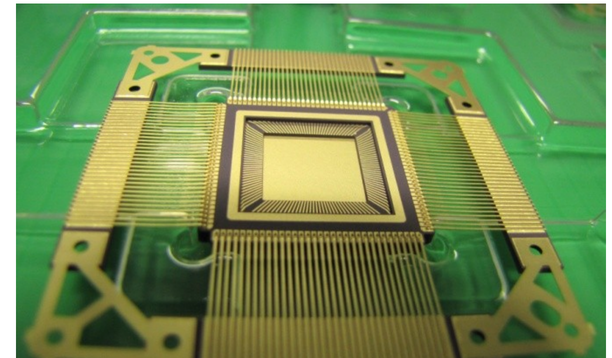
First batch of 43 flight modules for space application have been designed and delivered using the DARE180 library (Design Against Radiation Effects – Based on UMC 180 µm technology)

Full screening and qualification for space has been done according to the ESCC 9000 spec (ESA Requirements)

- SEL free up to 111.4 MeV
- SEU free up to 55.7 MeV







Extra order for FM's delivery

TESAT has placed new order for 160 extra FM's to be delivered in 2011!!

- Assembly according chart F2
- Electrical test and reliability tests according to chart F3.
- Lot Qualification chart F4

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statements

Design in 90, 65, 40nm is becoming increasingly complex : GDS prep and check crucial for error-free tape out

Design within corners to assure first-time right success

Test and qualification: increasingly important

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