Agenda

1. REDSAT ASICs
2. Cosmic Vision Instrumentation ASICs

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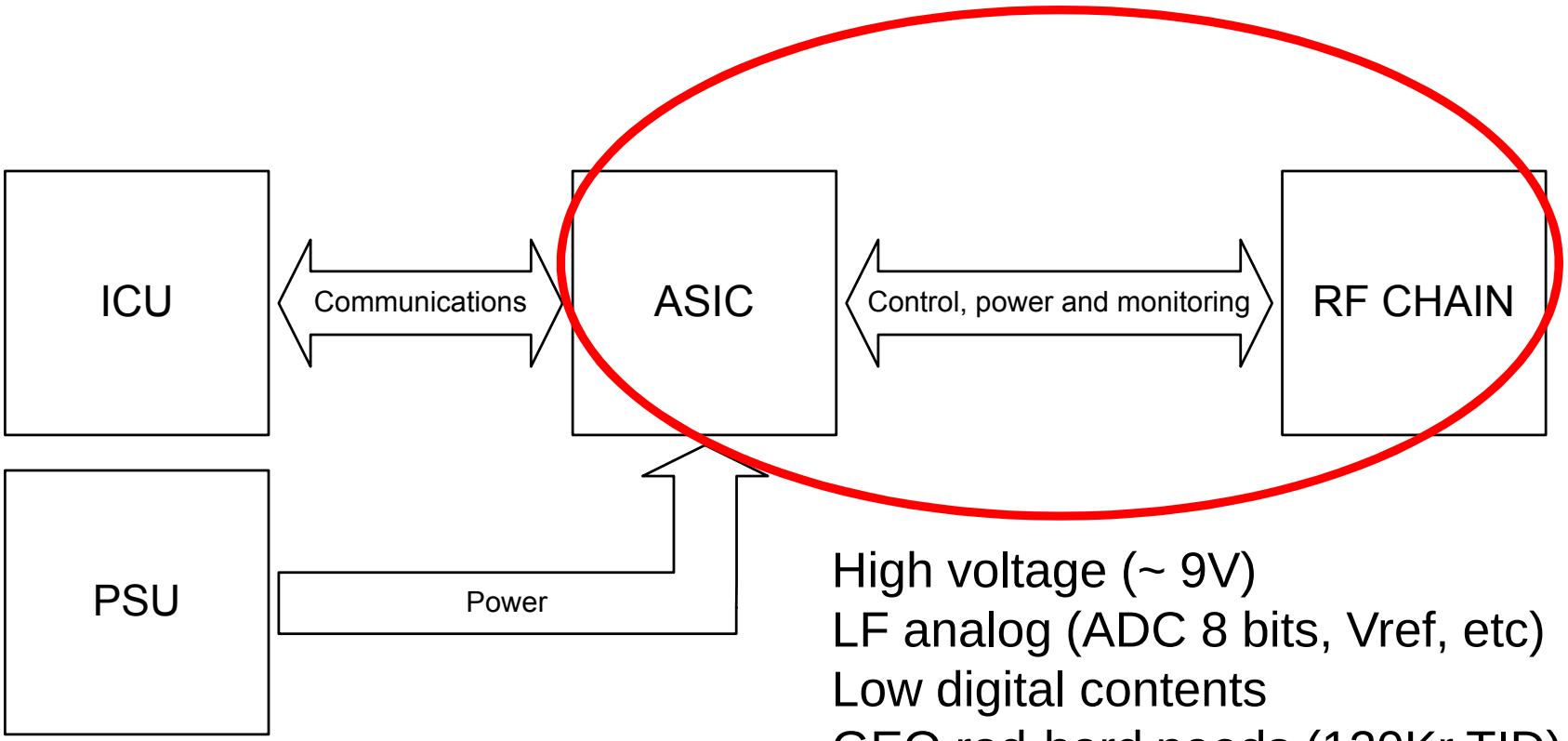
The REDSAT ASICs

Why we selected DARE

Direct Radiating Antenna REDSAT ASIC

- Project: REDSAT
- System: Direct Radiating Antenna
- Designer: Arquimea & UC3M
- Customer: EADS CASA ESPACIO
- Final Customer: Hispasat

Direct Radiating Antenna REDSAT ASIC



High voltage (~ 9V)
LF analog (ADC 8 bits, Vref, etc)
Low digital contents
GEO rad-hard needs (120Kr TID)
Die assembly in hybrid module

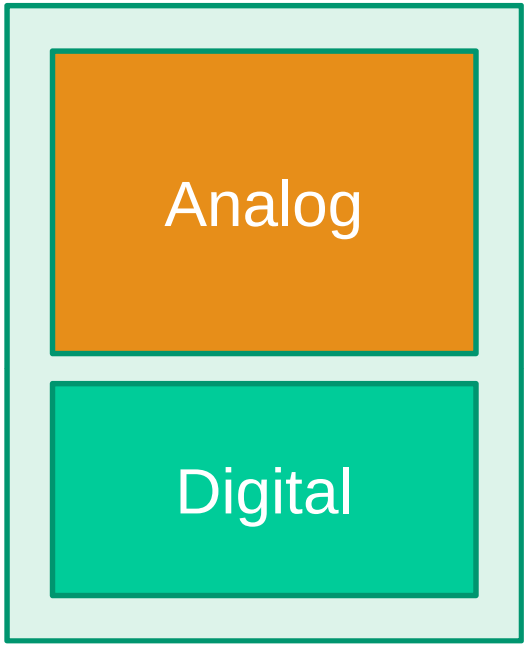
Tight developement schedule

Initial Technology Selection

- IT380 On-Semi BCD
  - Supported by Europractice
  - Rad-hard heritage from SPADA project (SODERN)
  - MLM capability
  - High voltage (up to 80V)

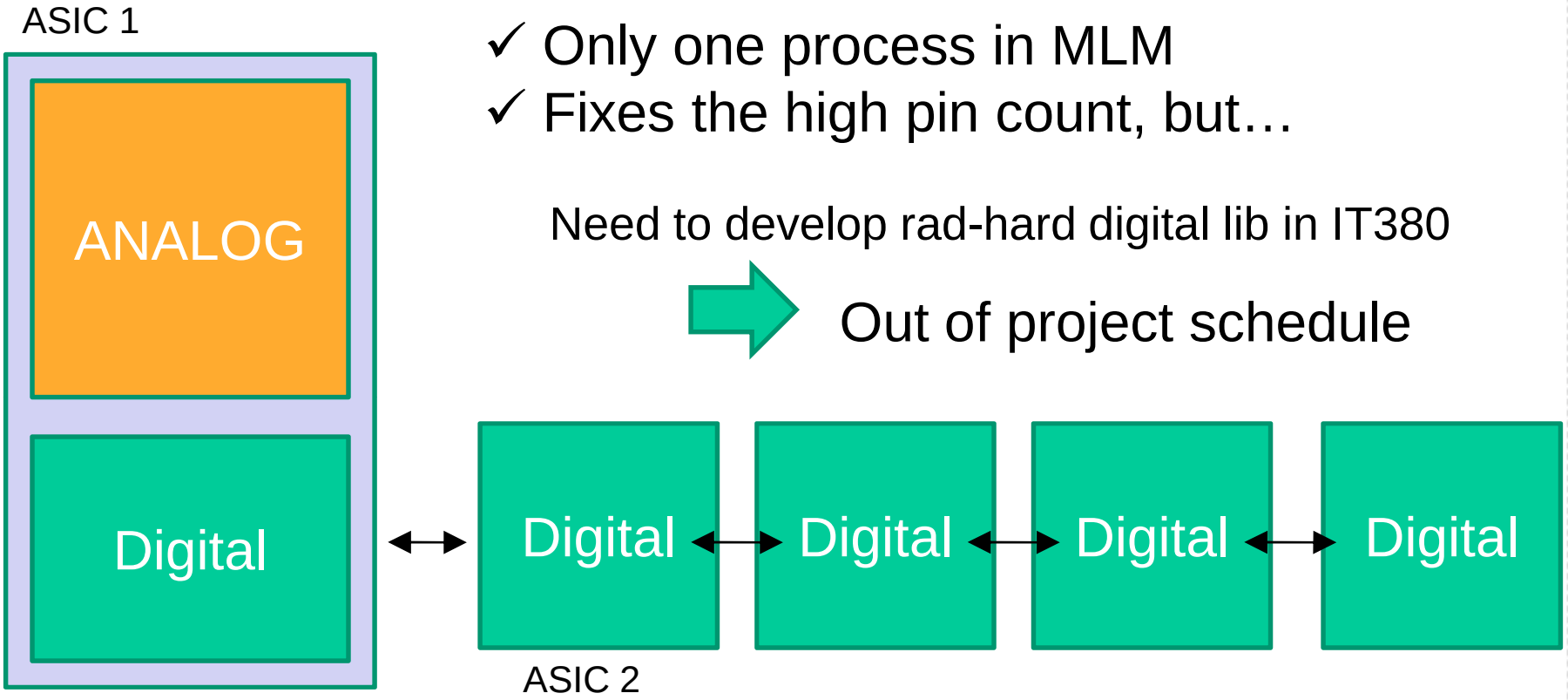
- UMC 180nm CMOS
  - Supported by Europractice
  - DARE
  - High voltage option (but not available for low volume)

Design Alternative 1
A single ASIC in either UMC / IT380



- Die size too big (180 pins, pad limited)
- No analog lib in UMC 180nm
- No HV option in UMC 180nm
- No rad-hard digital lib in I3T80

Design Alternative 2
Two ASICs in IT380

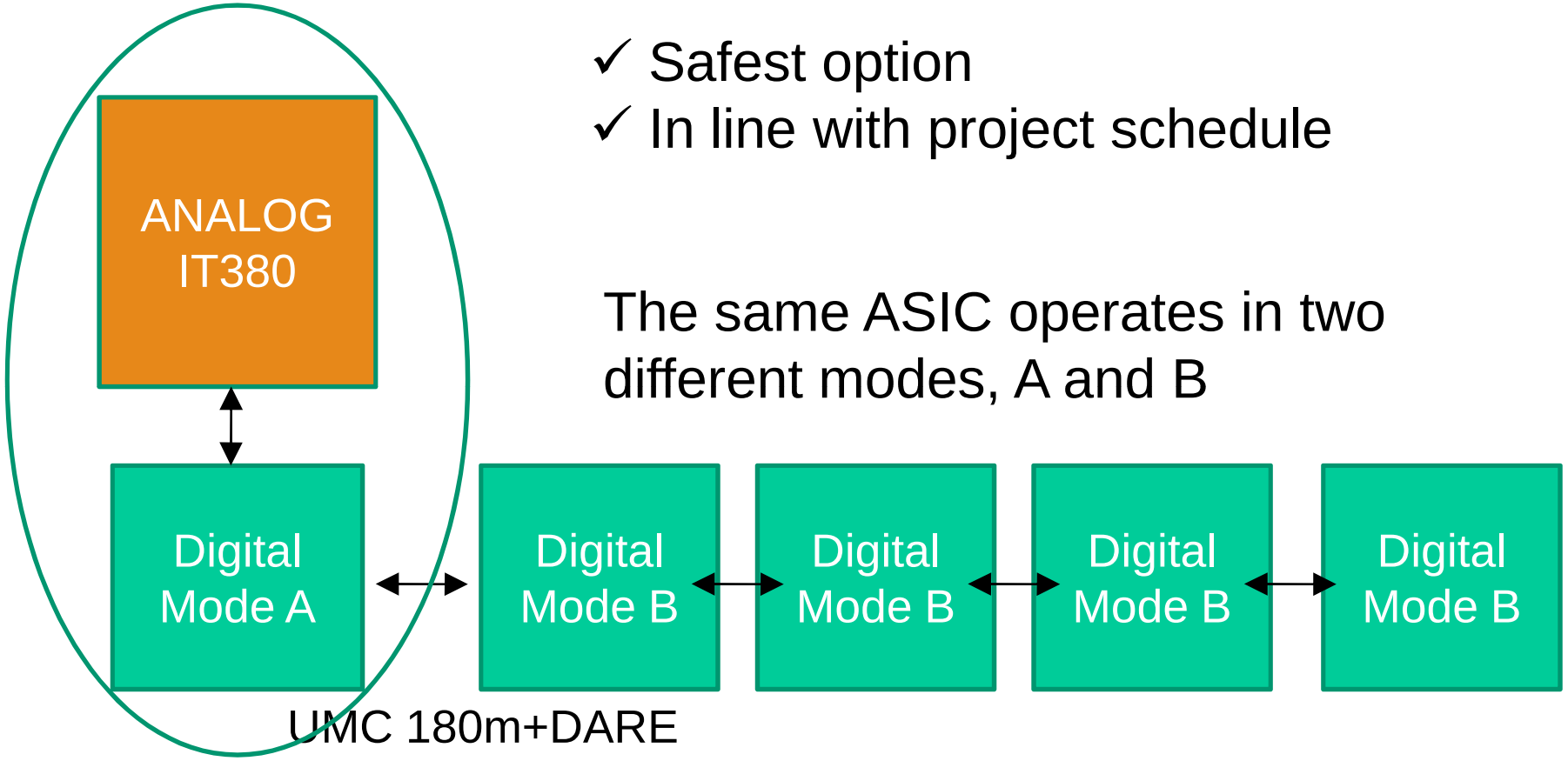


- ✓ Only one process in MLM
- ✓ Fixes the high pin count, but…

Need to develop rad-hard digital lib in IT380

Out of project schedule

Design Alternative 3
Two ASICs in IT380 + DARE



- ✓ Safest option
- ✓ In line with project schedule

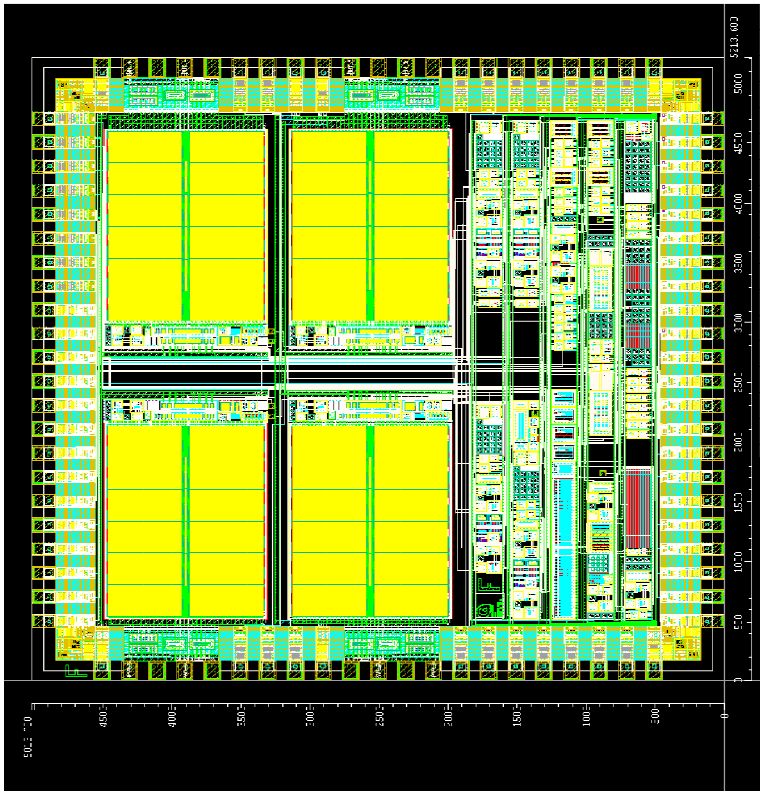
The same ASIC operates in two different modes, A and B

Design Summary

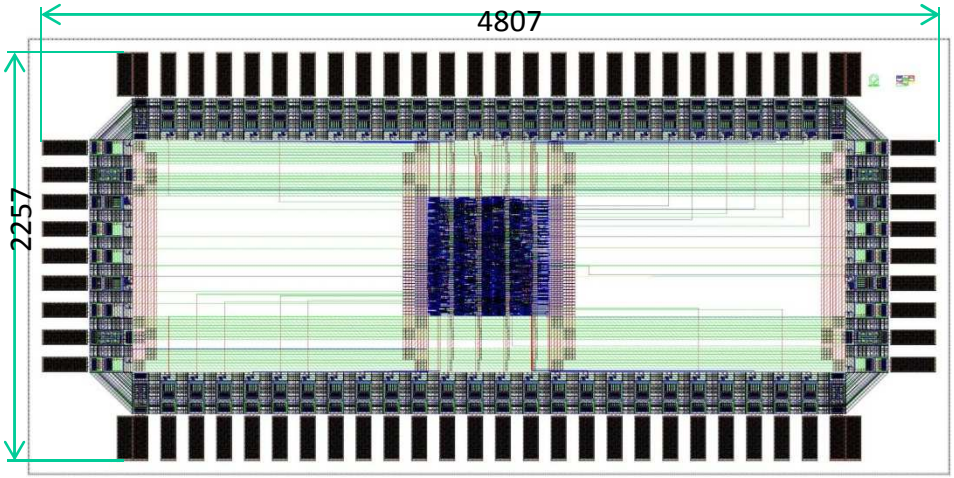
- Analog ASIC (IT380)
  - o HV 150mΩ power switches (x4)
  - o PT-1000 based temperature measurement (x4)
  - o 8 bits ADC
  - o Bandgap reference
  - o Staus: silicon expected by wk 9

- Digital “DARE” ASIC. Mode A/B selected by pin
  - Mode A
    - o SPI interface
    - o ADC Succesive Approximations logic
    - o CRC computation for error detection
  - Mode B
    - o SPI interface
    - o 24 bits shift register
  - Status: ready for electrical wafer sorting

Design Summary (layout)



IT380 chip

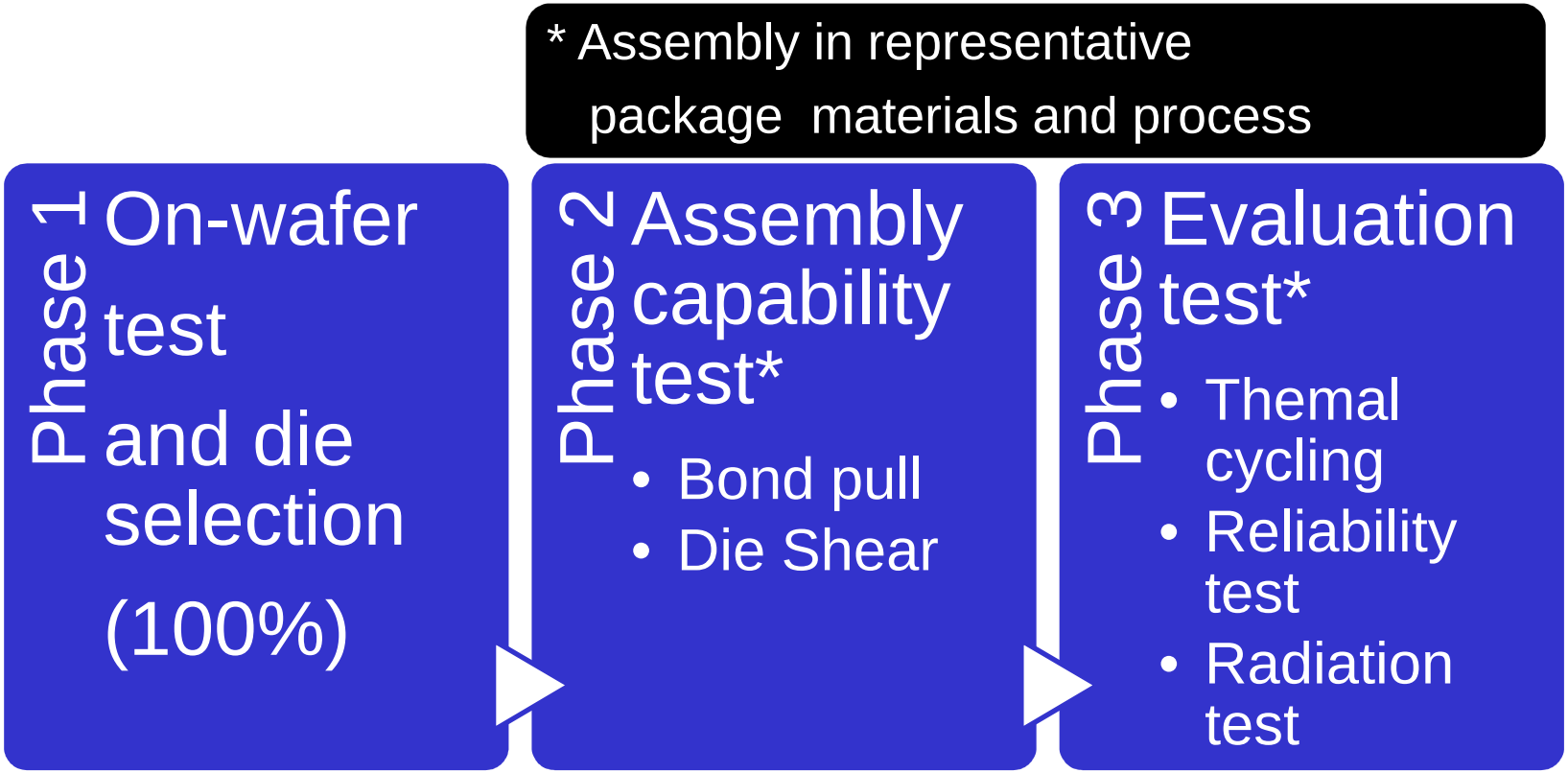


DARE chip

~10K gates

Thanks for the excellent support from IMEC !

ASIC PROJECT QUALIFICATION FOR ASSEMBLY IN A HYBRID



Cosmic Vision Instrumentation ASICs

What we need from DARE

Cosmic Vision ASICs
ESA project partners

- Prime contractor: Arquimea (Madrid)

- Subcontractors:
  - CNM (Spanish National Microelectronics Center, Sevilla, Barcelona)
  - UC3M (University Carlos III, Madrid)
  - UPC (Technical University of Catalonia, Barcelona)

- Project status: architecture definition (pre–ADR)

The ESA Cosmic Vision Programme

2015 - 2025

A set of missions with top scientific contents:

- What are the conditions for life and planetary formation?
- How does the Solar System work?
- What are the fundamental laws of the Universe?
- How did the Universe begin and what is it made of?

Source: ESA website

The ESA Cosmic Vision Programme

…calls for sophisticated measurements:

The Sun's magnetic field
Laser interferometer to detect gravitational waves (LISA)
Ultra-high energy cosmic-rays
Radiation from matter near black holes
Near-infrared interferometer
Gamma-ray imaging
etc.....

…in a very harsh conditions:

Jupiter strong magnetic field

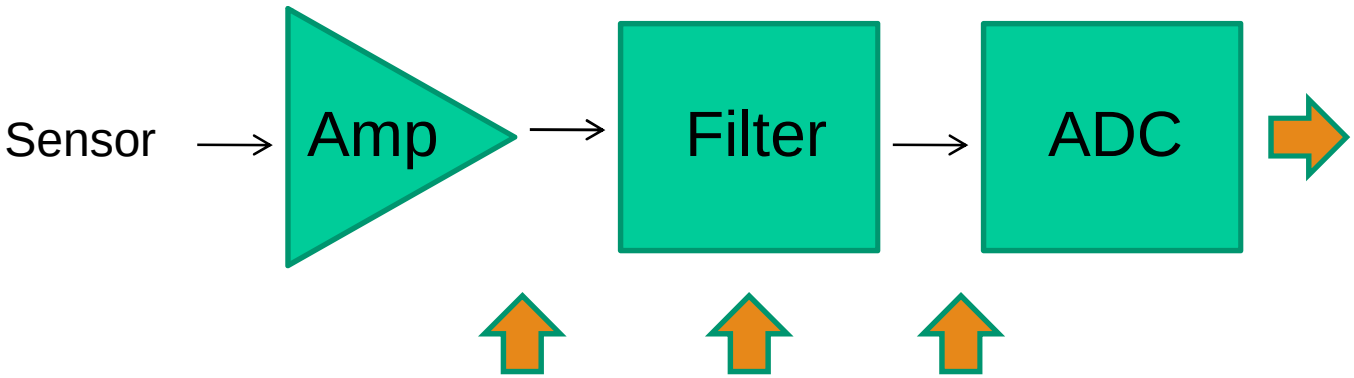
Need of challenging sensors & electronics payload

Source: ESA website

Two ESA TRP projects were launched

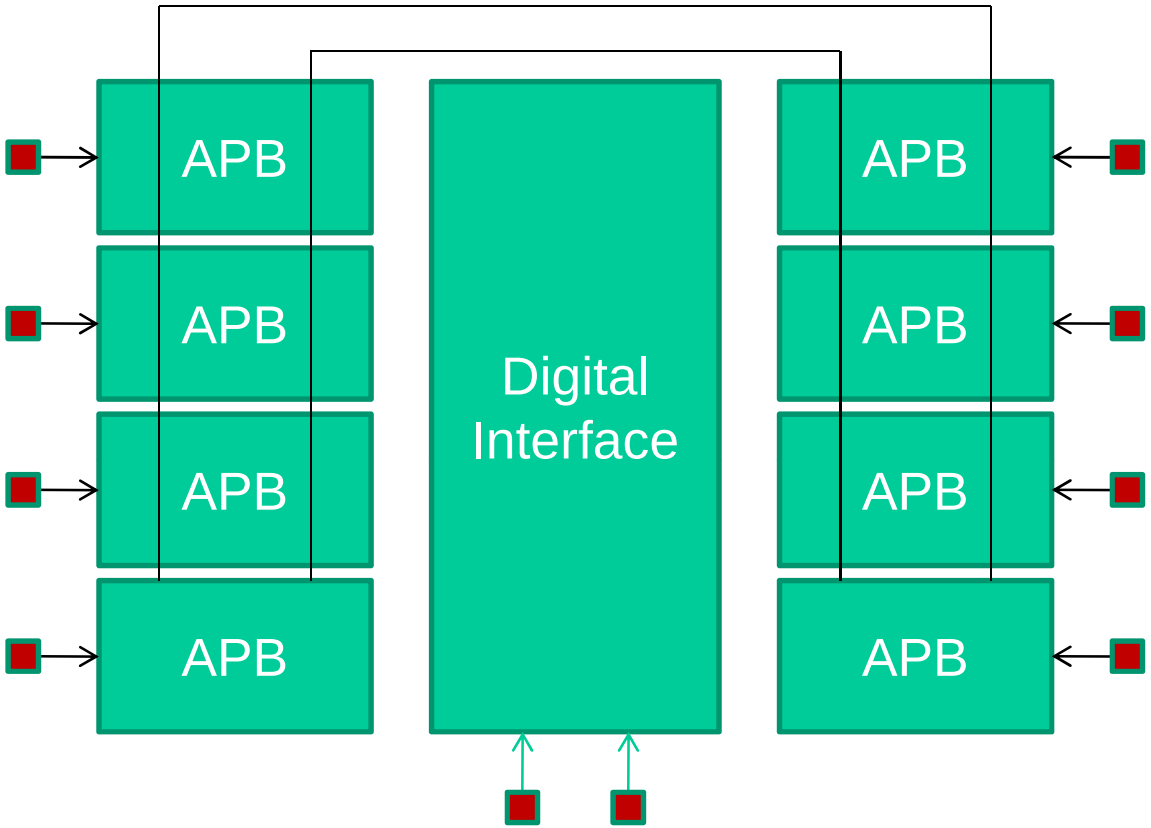
"Front-end readout ASIC technology study and development test vehicles for frontend readout ASICs"

1. Medium frequency front-end (up to 10Mz)
2. High frequency front-end (up to 100 MHz)



High reusability / reconfigurability

Cosmic Vision ASICs
ESA target



APB: Analog Processing Block

Analog Processing Block
Specs in the state-of-the art limits!

Some examples…

Block	Parameter	Value
ADC HF (pipeline)	ENOB	10bits @ 100MHz
ADC MF (∑Δ)	ENOB	19 bits @ 100KHz
Input amplifier (MF)	Noise	2nv/√Hz
Configurable filter (MF)	SFDR	114dB @ 100KHz

+ 300KRad TID !

Cosmic Vision ASICs
Selected Technology: UMC 180nm

- Europractice support
- Availability of radiation reports (digital vehicles)
- Use of DARE for the digital part
  - SPI interface for APB configuration
  - LVDS for HS parallel readout
  - DSP functions (TBC: decimator for ∑Δ,…)
- Power supply debate: 1.8V? 3.3V? 2.5V?
- Initial decision: 1.8V based-design except I/Os at 3.3V
  - DARE cells compatibility
  - Probably no ELT needed (?)

Cosmic Vision ASICs
DARE needs, wish list, open questions...

- Analog oriented radiation tests
- Will ELT be needed?
- Will existing DARE digital oriented ELT be good for analog?
- Will existing ESD structures be valid? (charge amplifier)
- Layout toolkit
- ELT toolkit (P-Cells, DRC/LVS)
- Transistor models of existing cells
- 2.5V LVDS ?
- What process options are available? (low Vth transistors)
- Low power Xtal oscillator