ASICs for Space Fabricated with Radiation Hardened by Design Library

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Ref : LEONDARE-ETCA-EDR-0132
Date : 15 February 2011

- Project Overview
- LEON3-FT IP
- ASIC Development
- *Coffee break*
- ASIC Production
- Evaluation tests results
- FM Procurement flow
- Leondare performance
- Lesson Learnt
- Questions

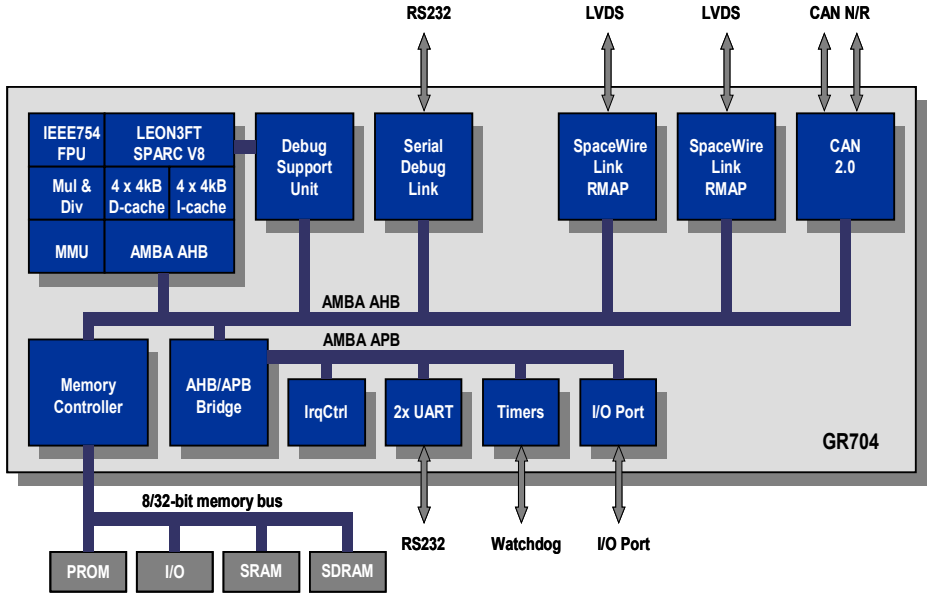
Project overview

Ref : LEONDARE-ETCA-EDR-0132
Date : 15 February 2011

- **Study objectives**
  - Develop, manufacture and produce a digital ASIC in a fabless approach, using a commercially available technology (UMC 0.18 µm CMOS) & the DARE180 library
  - Evaluate the technology according to a dedicated production and evaluation flow complying with the ESCC standards
  - DARE180 library improvements
- **The 2 main outputs of the project**
  - An evaluation plan summarizing the results of all the tests
  - An ASIC procurement & Qualification flow defining the tests to perform for guaranteeing highest space quality and reliability requirements for future DARE180 chips.

- **DARE = Design Against Radiation Effects**
- **Developed by IMEC under ESA contracts**
- **Technology**
  - UMC L180 CMOS Logic 1P6M (1.8V/3.3V)
- **Hardened using layout techniques**
  - Enclosed transistors & guard bands
- **86 Core Cells**
  - 50 combinatorial cells
  - 2 x 18 flip-flop & latch cells included (18 HIT cell–based SEU hard)
- **23 In-line IO Pad Cells (+ P/G + Corners + Fillers)**
  - 3.3V & 2.5V I/O's
  - Includes LVDS (driver, receiver & bias)
  - Several pull-up/down options
  - >4KV HBM ESD performance
  - 5V tolerance & cold spare possibility proven
- **Single Port SRAM Compiler (standard 6 transistor RAM cell)**
- **PLL**
- **Maximum gate density: 25Kgates/mm^2**

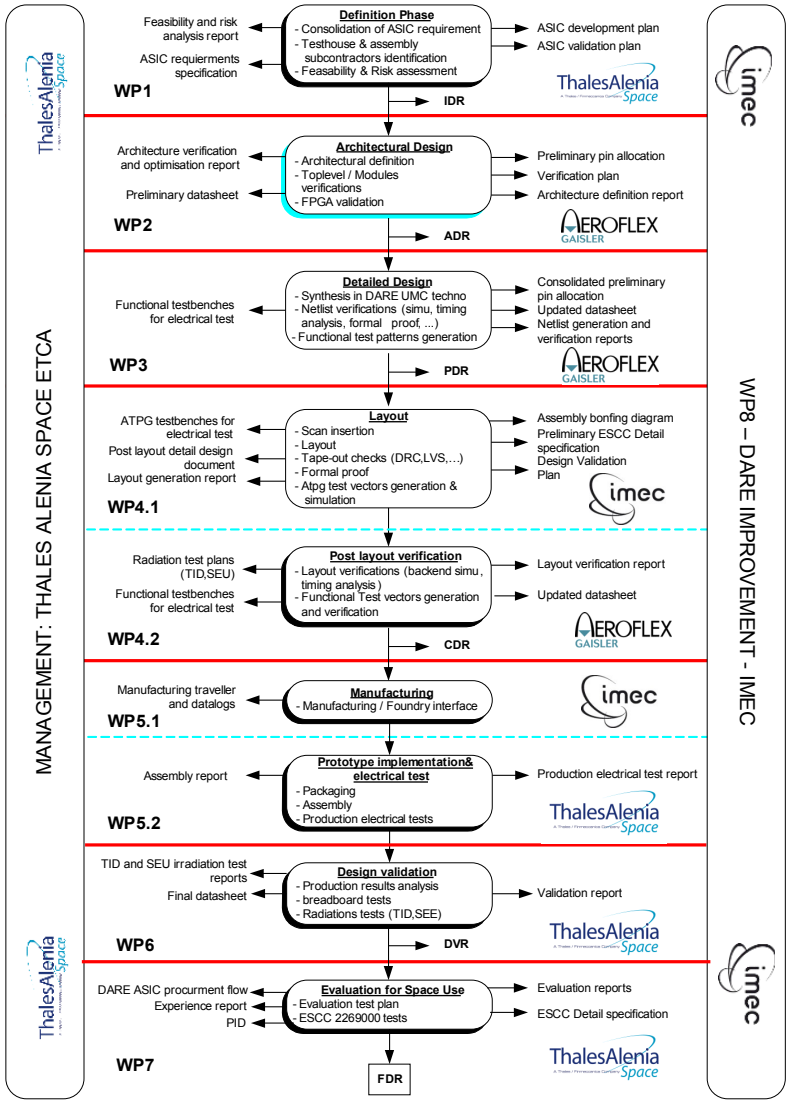
- **Design selected is the Aeroflex-Gaisler LEON3-FT IP + IP Peripherals**
  - Appropriate complexity for evaluating a technology (SRAM, PLL, LVDS,…)
  - More flexibility for the testability
  - High-performance processor for the space domain



=> LEON-DARE Architecture

Project structure

- **Thales Alenia Space ETCA (B) - Prime**
  - Project management
  - Validation and evaluation testing
- **Aeroflex Gaisler (SE)**
  - LEON3-FT processor design and synthesis
- **IMEC (B)**
  - Layout generation and DARE library
  - Interface with ASIC wafer fab via MPW EUROPRACTICE run
- **Subcontractors**
  - Assembly : HCM (Fr)
  - Test house: SERMA (Fr) technologies
  - Package: Kyocera (J)
  - Radiation Facilities: UCL (B)
- **8 Work Packages (WP)**



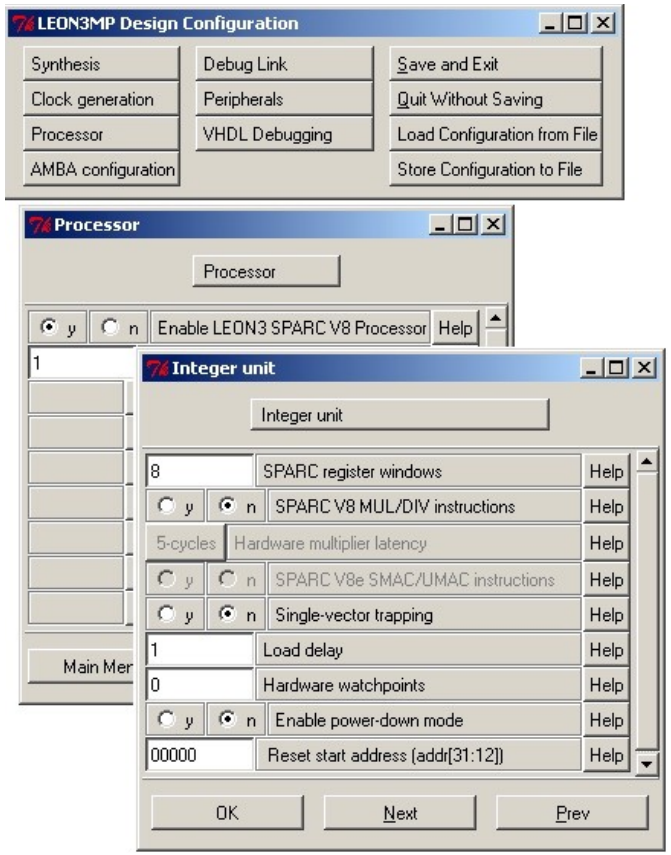
- **Under IMEC responsibilities**
- **Multi-Project-Wafer (MPW) runs**
  - Reservation of 1,2 or 4 silicon blocks of 5x5 mm^2
  - Wafer thickness option : 11 or 29 mils
  - ± 5 runs / year
  - ± 40 dice / wafer
  - Reduce cost : ± 16k€ / block
- **Full wafer run possibility**
- **NDA to sign for accessing technology information**

LEON3-FT IP

GRLIB Library

- **GRLIB is a complete design environment:**
  - Processors
  - Peripherals
  - Serial interfaces
  - Parallel interfaces
  - Memory controllers
  - AMBA on-chip bus with Plug & Play support
  - Fault tolerant and standard versions

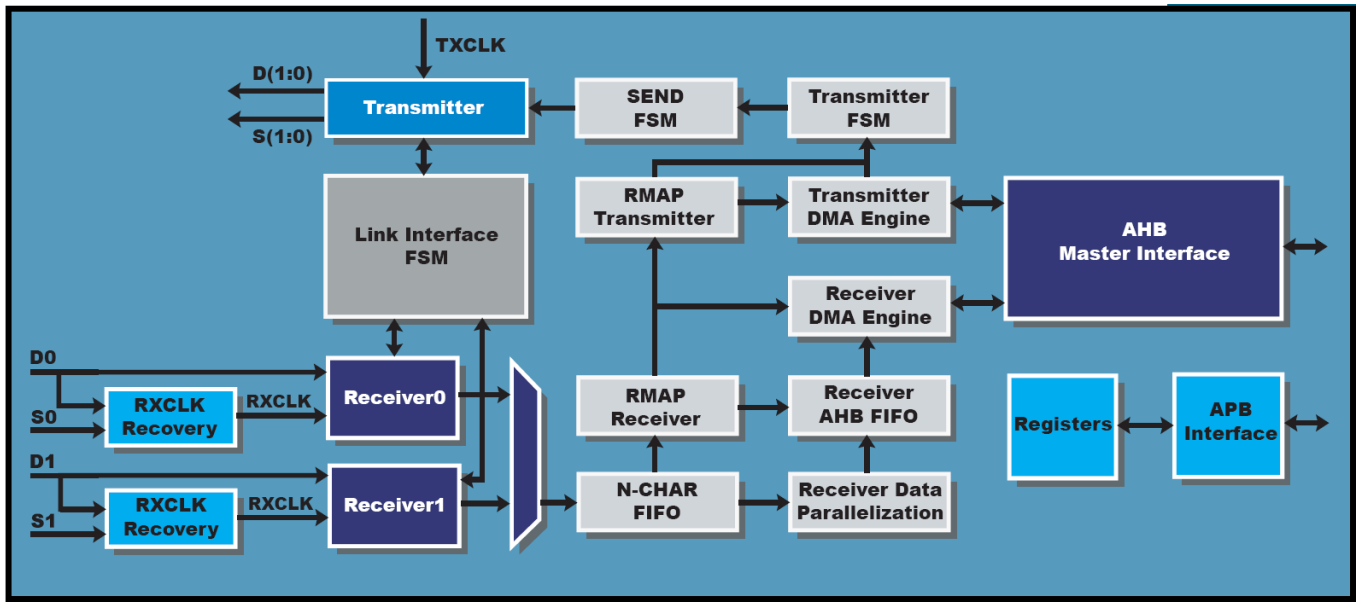
- **Support for tools & prototyping boards**
- **Portability between technologies**



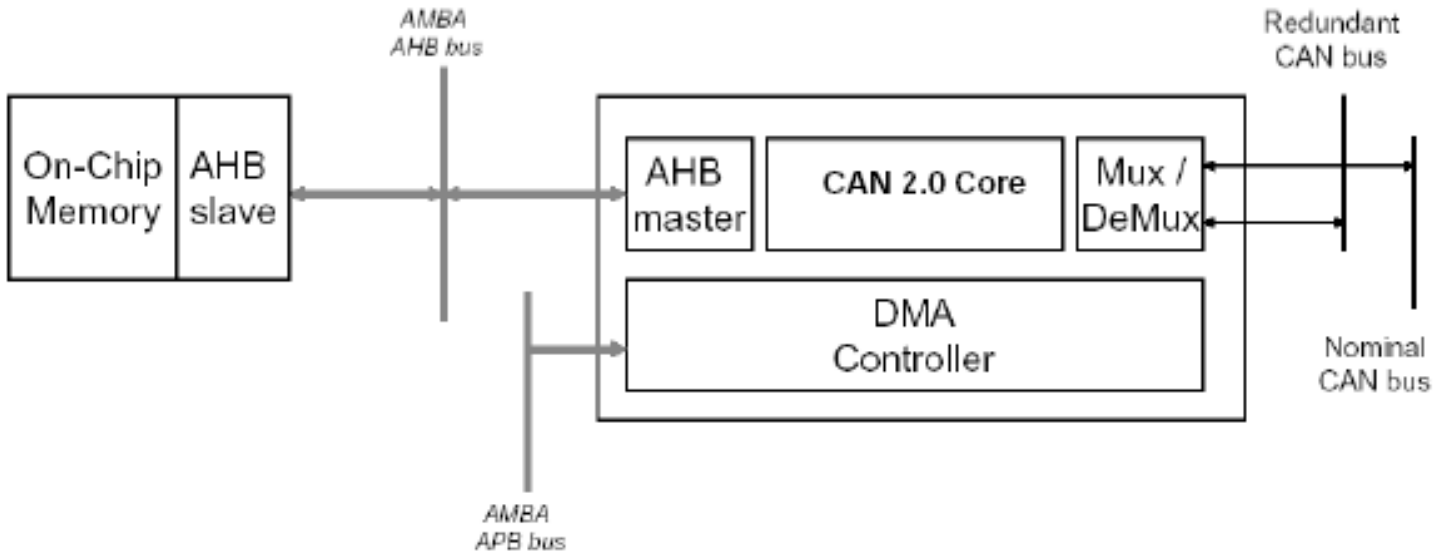
- **IEEE-1754 SPARC V8 compliant 32-bit processor:**
  - 7-stage pipeline, multi-processor support
  - Separate multi-set caches with LRU/LRR/RND
  - On-chip debug support unit with trace buffer
  - Highly configurable:
    - Cache size 1-256 kByte, 1-4 ways, LRU/LRR/RND
    - Hardware Multiply/Divide/MAC options
  - SPARC Reference Memory Management Unit (SRMMU)
  - Floating Point Unit (high-performance or small-size)
  - Pipeline optimization for specific target technologies
  - Fault tolerance optimization for specific target technologies

- **Certified SPARC V8 by SPARC International**
- **Suitable for space and military applications**
- **Baseline processor for space projects in US, Europe, Asia**

- **ECSS compliant SpaceWire interface:**
  - The GRSPW core implements an AMBA interface with DMA and RMAP in hardware.
  - The core is optimized for system-on-chip integration, fault tolerance and portability.



- **CAN 2.0 interface:**
  - The GRCAN core implements an AMBA interface with DMA
  - Software compatible with the CAN core in the AT9713E (SpW-RTC) device
  - The core is optimized for system-on-chip integration and portability



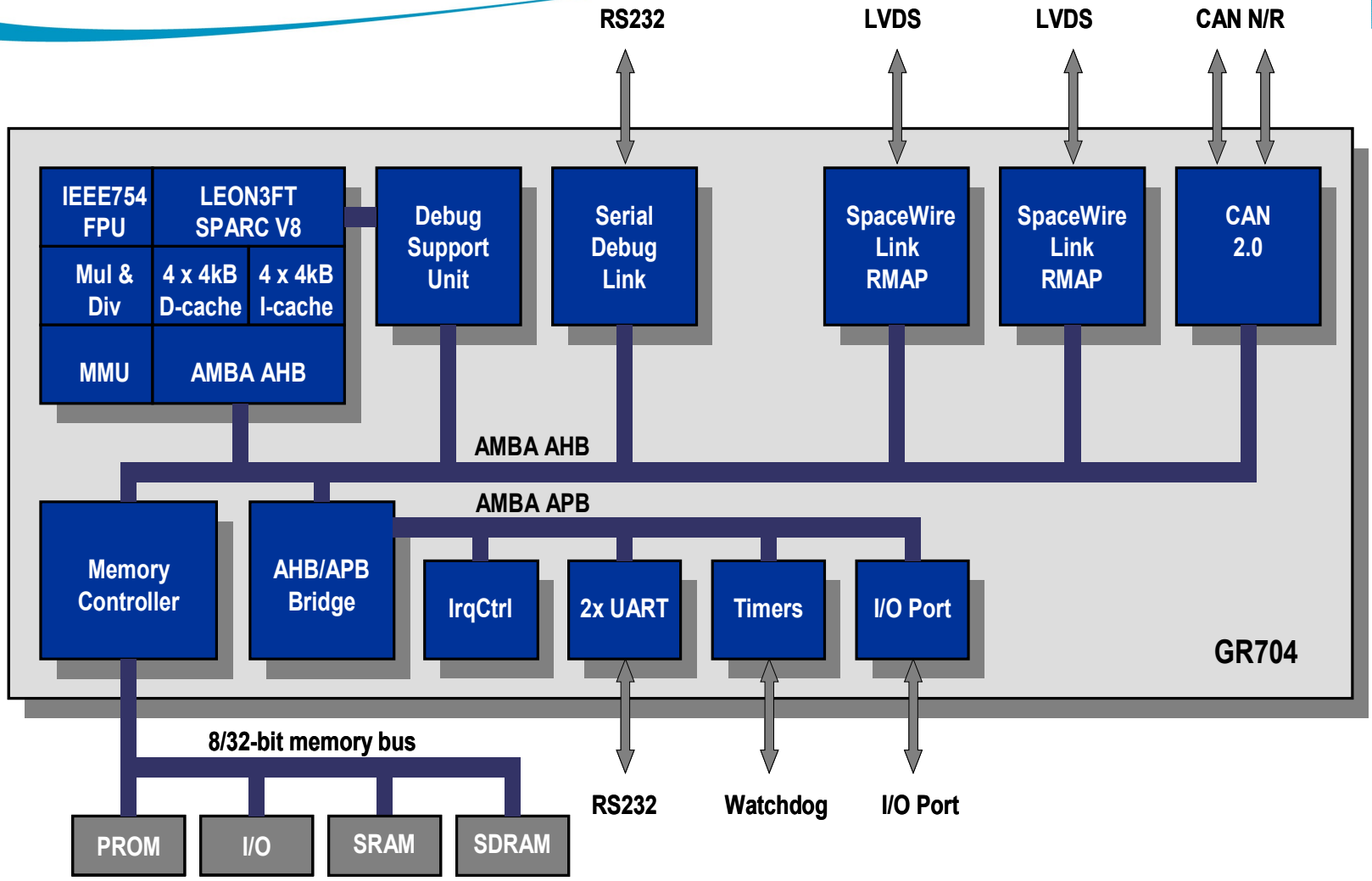
- **GR704 configuration**
  - LEON3 SPARC V8 32-bit Integer Unit
    - 4x4 kByte instruction cache, 4x4 kByte data cache
    - Hardware multiplier and divider
    - Power down mode
  - GRFPU-FT IEEE-754 Floating Point Unit
  - SPARC Reference Memory Management Unit
  - Debug Support Unit with UART Debug Links
  - Memory controller with EDAC: PROM/SRAM/SDRAM/I/O
  - Timer unit with 3x 32-bit timers and watchdog
  - Interrupt controller for 15 interrupts in two priority levels
  - Two UARTs with FIFO and separate baud rate generators
  - 16-bit general purpose input output port
  - 2 x SpaceWire links with RMAP support
  - 1 x CAN interface with DMA support
  - PLL: 1x, 2x, 4x, separate clocks for processor and SpaceWire links

Performance

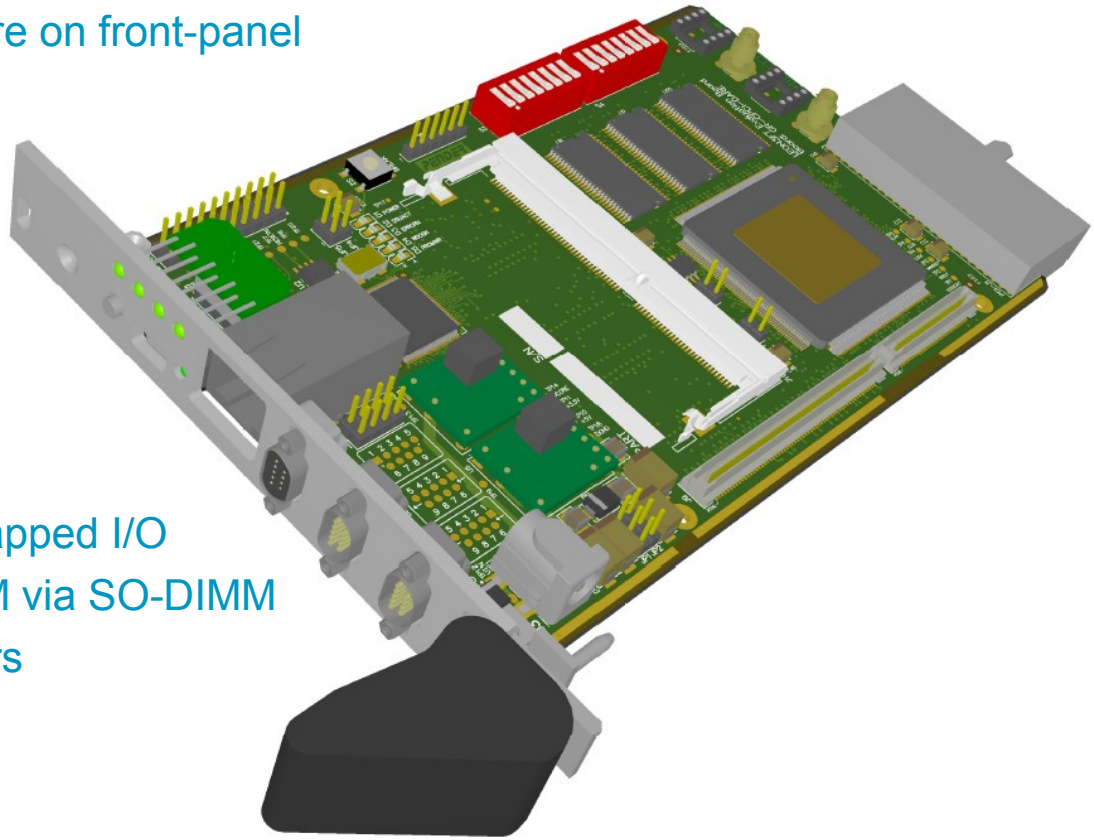
- **GR704 performance expectations (data sheet values):**
  - 100 MHz system frequency
  - 200 MBPS SpaceWire links, full duplex
  - 1 MBPS CAN link

  - > 100 DMIPS (compiler dependent)
  - 100 MFLOPS (assembler)

GR704 block diagram



- **RASTA compatible GR704 CPCI board:**
  - Goal to be compatible with RASTA
  - Communication via SpaceWire on front-panel
  - Full RTEMS support:
    - Drivers, BSP
    - RMAP initiator stack
- **Features**
  - 2 x SpaceWire on MDM-9
  - Redundant CAN on MDM-9
  - Debug UART via USB
  - Ethernet MAC as memory mapped I/O
  - SRAM, Flash PROM, SDRAM via SO-DIMM
  - Memory expansion connectors
  - Power via CPCI connector
- **Development stopped**

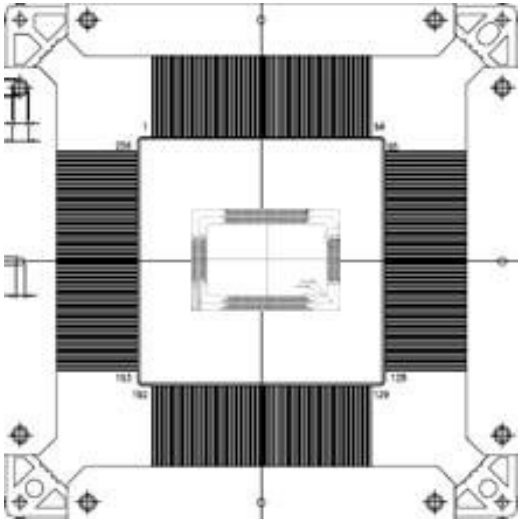


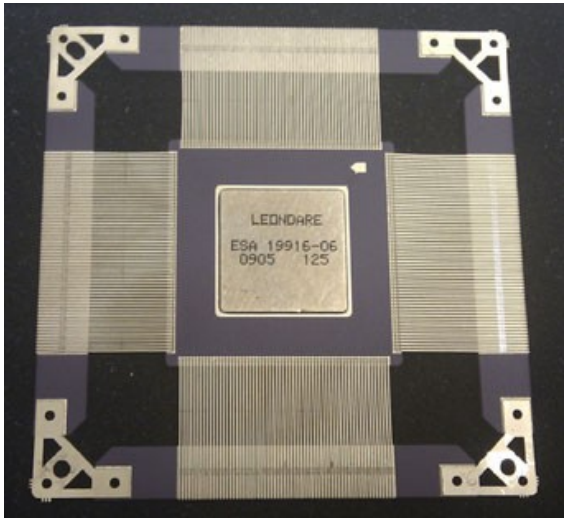
ASIC Development (ESCC-Q-60-02)

- **Initial design didn't fit the initial 5x5mm² silicon square**
  => Design update with bigger die size (10x5 mm²)

	Initial	Final
Die	5x5 mm²	10x5mm²
Core	LEON3-FT	LEON3-FT
IU	1	1
Caches	4+4	16+16
MMU	-	1
SpaceWire	1	2
CAN	-	GRCAN-FT
FPU	GRFPU-FT Lite	GRFPU-FT
Package	CQFP172	CQFP256

- **No standard package for the die shape and IO count:**
  - Manufacturer: Kyocera (J)
  - Development of a full-custom CQFP-256 package with tie-bar
  - Rectangular cavity
  - Gold thickness : 100 µinch
  - Antibleeding process





Design test means

- Internal temperature diode for junction temperature monitoring
- Ring Oscillator for timing drift analysis
- PLL Bypass
- Scan insertion & ATPG
- No memory BIST but specific test software
- Dedicated test software
  - IU test, Paranoia, dhrystone, SpaceWire test, test float,…

- **Netlist + constraints file from Gaisler**
  - Insertion of scan
  - Place & Route
  - ATPG
  - Sign-off checks
  - Tapeout
  - Manufacturing in MPW

- **Possible issue with larger RAMS was known, but not understood yet.**

Script

Dont’use non-HIT flops
Read in NL
Configure test insertion
Assign scan in/out ports
Apply timing constraints
Create & write NL with scan

NL without scan

Verilog

```
module shifter ( s_in, clk, p_load, set, p_in, p_out );
  input [15:0] p_in;
  output [15:0] p_out;
  input s_in, clk, p_load, set;
  wire   n57, n58;

  INV01 U33 ( .I(set), .ZN(n57) );
  SDFCNQ01 shift16_reg_15 ( .D(p_in[15]), .SI(s_in), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[15]) );
  SDFCNQ01 shift16_reg_14 ( .D(p_in[14]), .SI(p_out[15]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[14]) );
  SDFCNQ01 shift16_reg_13 ( .D(p_in[13]), .SI(p_out[14]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[13]) );
  SDFCNQ01 shift16_reg_12 ( .D(p_in[12]), .SI(p_out[13]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[12]) );
  SDFCNQ01 shift16_reg_11 ( .D(p_in[11]), .SI(p_out[12]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[11]) );
  SDFCNQ01 shift16_reg_10 ( .D(p_in[10]), .SI(p_out[11]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[10]) );
  SDFCNQ01 shift16_reg_9_ ( .D(p_in[9]), .SI(p_out[10]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[9]) );
  SDFCNQ01 shift16_reg_8_ ( .D(p_in[8]), .SI(p_out[9]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[8]) );
  SDFCNQ01 shift16_reg_7_ ( .D(p_in[7]), .SI(p_out[8]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[7]) );
  SDFCNQ01 shift16_reg_6_ ( .D(p_in[6]), .SI(p_out[7]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[6]) );
  SDFCNQ01 shift16_reg_5_ ( .D(p_in[5]), .SI(p_out[6]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[5]) );
  SDFCNQ01 shift16_reg_4_ ( .D(p_in[4]), .SI(p_out[5]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[4]) );
  SDFCNQ01 shift16_reg_3_ ( .D(p_in[3]), .SI(p_out[4]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[3]) );
  SDFCNQ01 shift16_reg_2_ ( .D(p_in[2]), .SI(p_out[3]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[2]) );
  SDFCNQ01 shift16_reg_1_ ( .D(p_in[1]), .SI(p_out[2]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[1]) );
  SDFCNQ01 shift16_reg_0_ ( .D(p_in[0]), .SI(p_out[1]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[0]) );
  INV01 U51 ( .I(p_load), .ZN(n58) );
endmodule
```

Synopsys
Test Compiler
1007.03-SP1

NL with scan

Verilog

```
module shifter ( s_in, clk, p_load, set, p_in, p_out );
  input [15:0] p_in;
  output [15:0] p_out;
  input s_in, clk, p_load, set;
  wire   n57, n58;

  INV01 U33 ( .I(set), .ZN(n57) );
  SDFCNQ01 shift16_reg_15 ( .D(p_in[15]), .SI(s_in), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[15]) );
  SDFCNQ01 shift16_reg_14 ( .D(p_in[14]), .SI(p_out[15]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[14]) );
  SDFCNQ01 shift16_reg_13 ( .D(p_in[13]), .SI(p_out[14]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[13]) );
  SDFCNQ01 shift16_reg_12 ( .D(p_in[12]), .SI(p_out[13]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[12]) );
  SDFCNQ01 shift16_reg_11 ( .D(p_in[11]), .SI(p_out[12]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[11]) );
  SDFCNQ01 shift16_reg_10 ( .D(p_in[10]), .SI(p_out[11]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[10]) );
  SDFCNQ01 shift16_reg_9_ ( .D(p_in[9]), .SI(p_out[10]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[9]) );
  SDFCNQ01 shift16_reg_8_ ( .D(p_in[8]), .SI(p_out[9]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[8]) );
  SDFCNQ01 shift16_reg_7_ ( .D(p_in[7]), .SI(p_out[8]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[7]) );
  SDFCNQ01 shift16_reg_6_ ( .D(p_in[6]), .SI(p_out[7]), .SE(n58), .CP(clk),
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        .CDN(n57), .Q(p_out[4]) );
  SDFCNQ01 shift16_reg_3_ ( .D(p_in[3]), .SI(p_out[4]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[3]) );
  SDFCNQ01 shift16_reg_2_ ( .D(p_in[2]), .SI(p_out[3]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[2]) );
  SDFCNQ01 shift16_reg_1_ ( .D(p_in[1]), .SI(p_out[2]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[1]) );
  SDFCNQ01 shift16_reg_0_ ( .D(p_in[0]), .SI(p_out[1]), .SE(n58), .CP(clk),
        .CDN(n57), .Q(p_out[0]) );
  INV01 U51 ( .I(p_load), .ZN(n58) );
endmodule
```
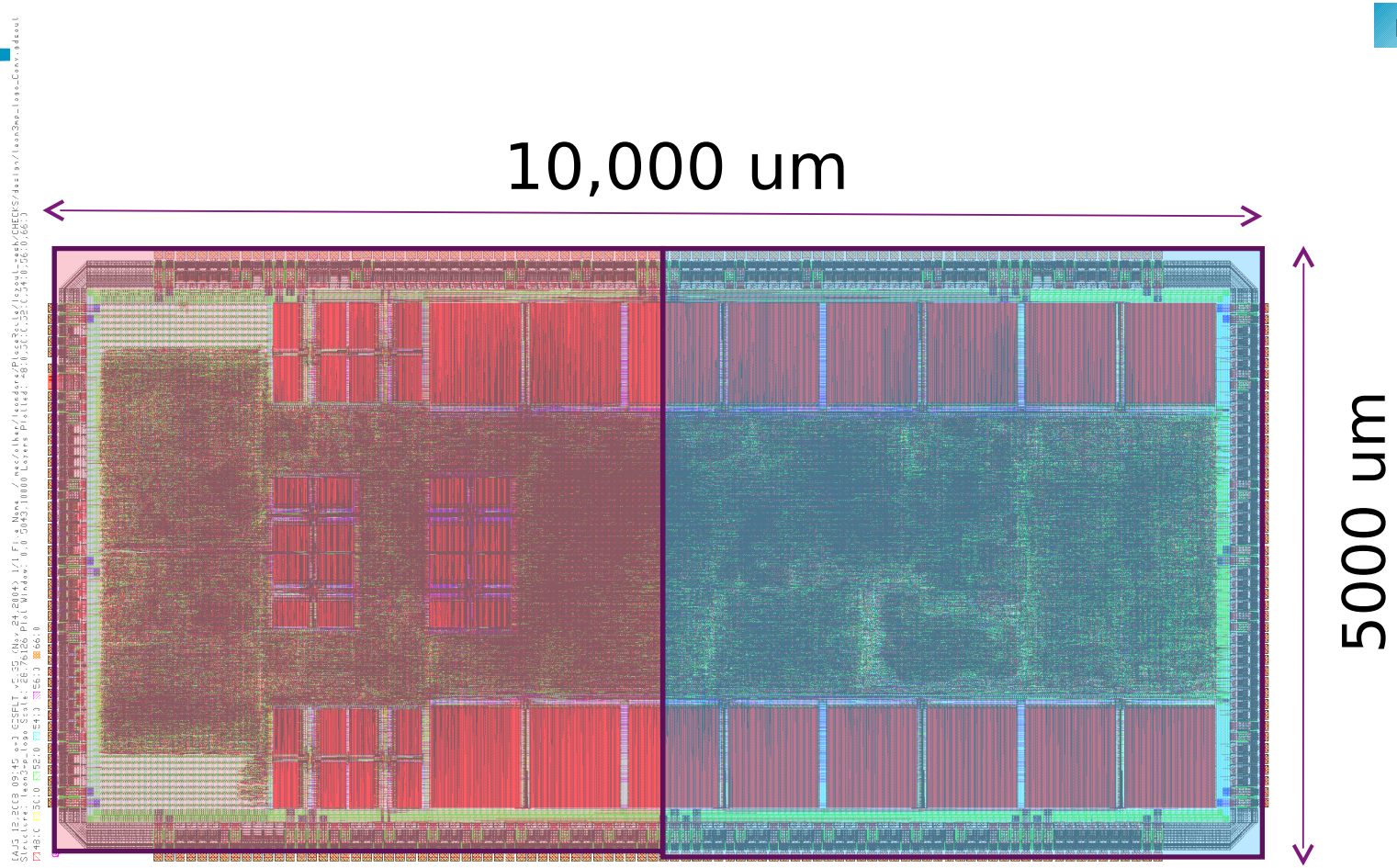

Timing Constraints

SDC

Final NL with scan

LAYOUT : 2 MPW BLOCKS



Tool: Synopsys Astro, version Z-2007.03-SP5

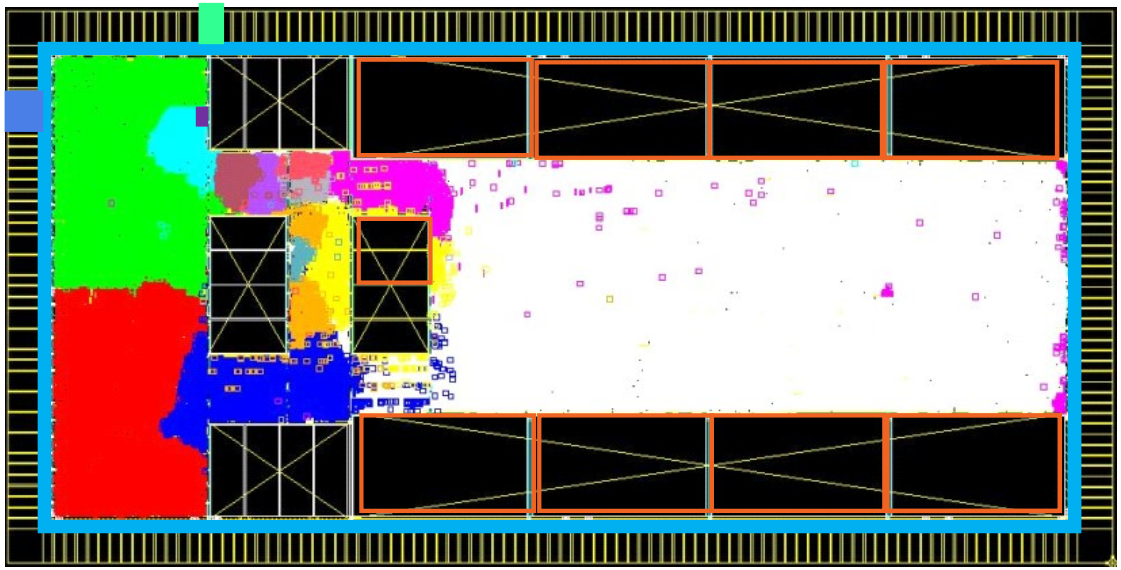
Note: Migrated to Cadence Encounter since

≠ automatic

- Region for SpaceWire 1
- Region for SpaceWire 2
- Ring Oscillator

Other cells = automatic placement

- Power Ring M6
- RAM Power Rings M4/5
- RAMS
- I/O
- Thermal diode
- PLL



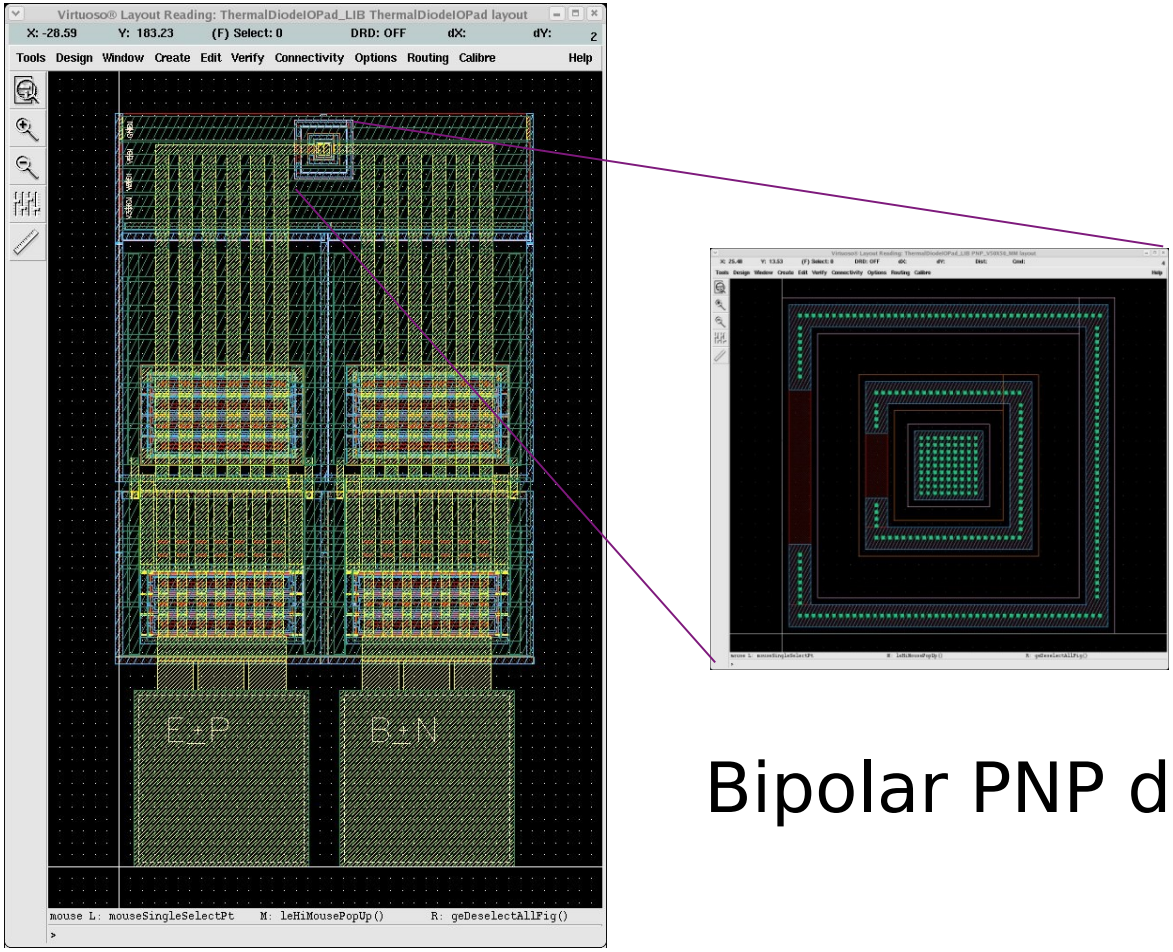
264 IO's

- **Timing constraints**
  - Adaptations to tool flow
  - Missing constraints added (normal)
  - Constraints for
    - Functional Mode
    - Test Mode

- **Optimization for setup (no hold)**
  - 174548 instances
  - 24 macros (rams)
  - 264 IO's

- **4 clocks to be handled in backend**
  - 125Mhz/200Mhz/2x150MHz
- **2 SpaceWire receiver clocks = XOR of 2 inputs**
  - Length from pads to gate equal
  - Each input = defined as clock
  - XOR gate inputs = synchronization points
- **1 post-CTS timing optimization was necessary to meet timing**
  - Core ultilization : 81%

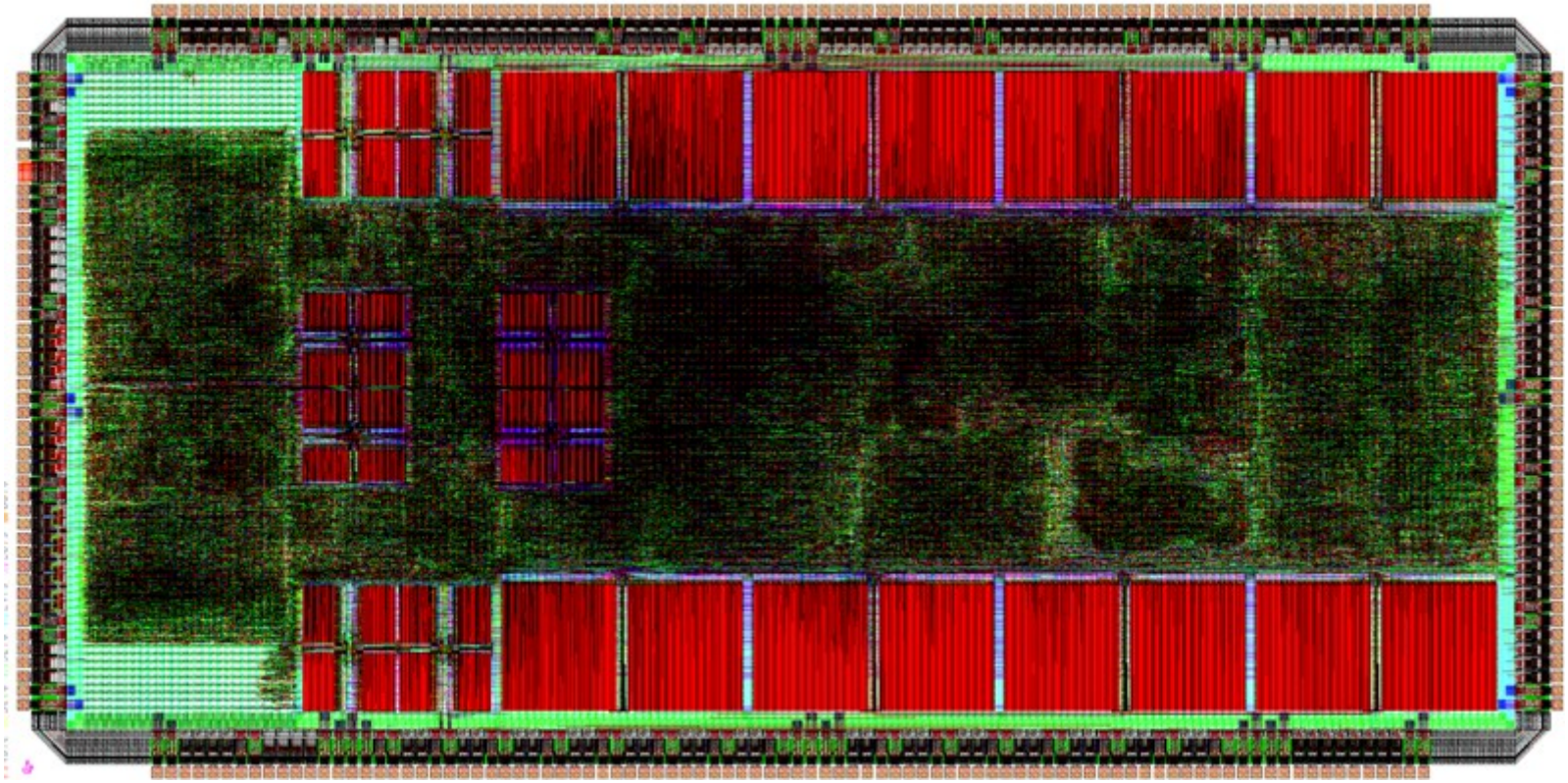
- **After routing 2 timing optimization iterations were necessary to meet post –layout timing**
  - Setup & finally hold
- **2 pairs of shorted nets needed minor manual fixing (no impact on timing)**
- **Layout finishing**
  - Adding IO filler cells
  - Adding core filler cells
  - GDSII generation
  - Replace placeholder with Thermal Diode (was under design)

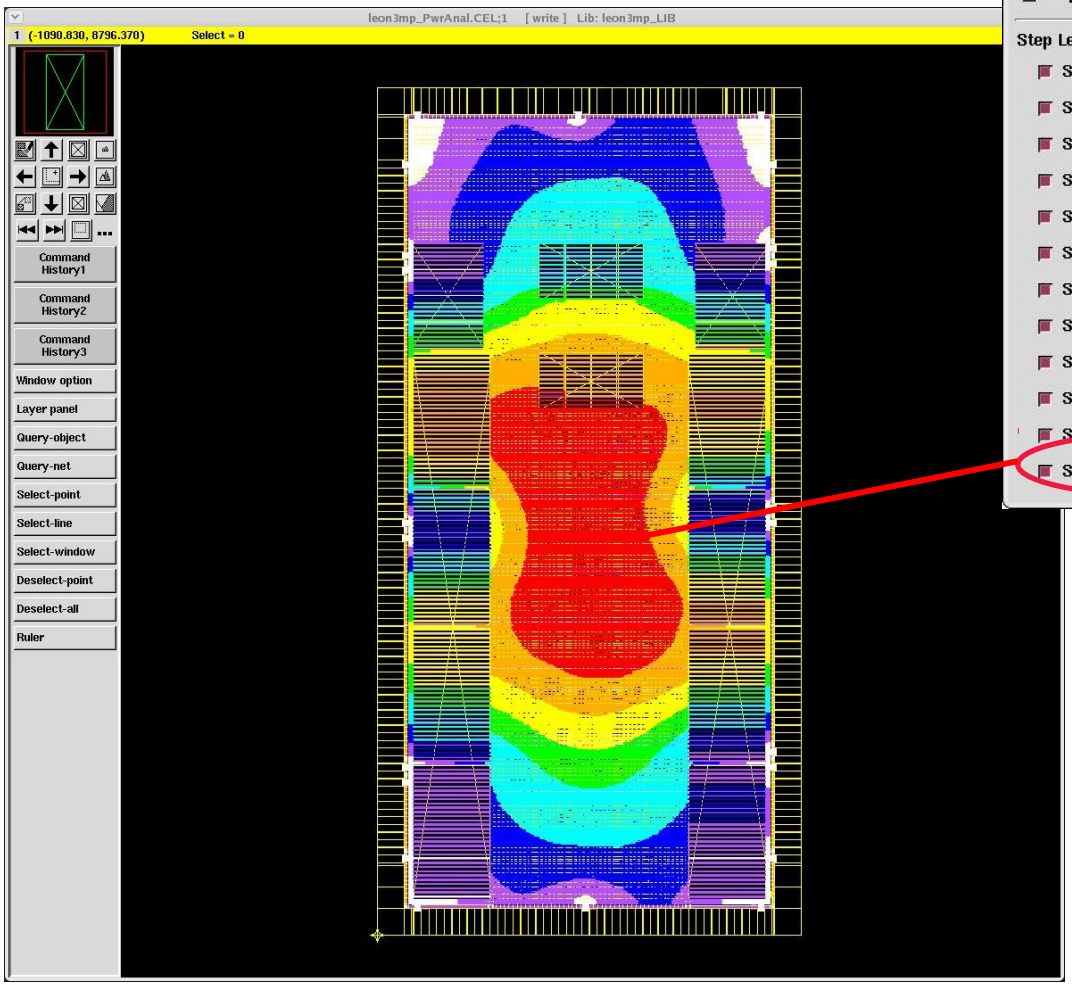


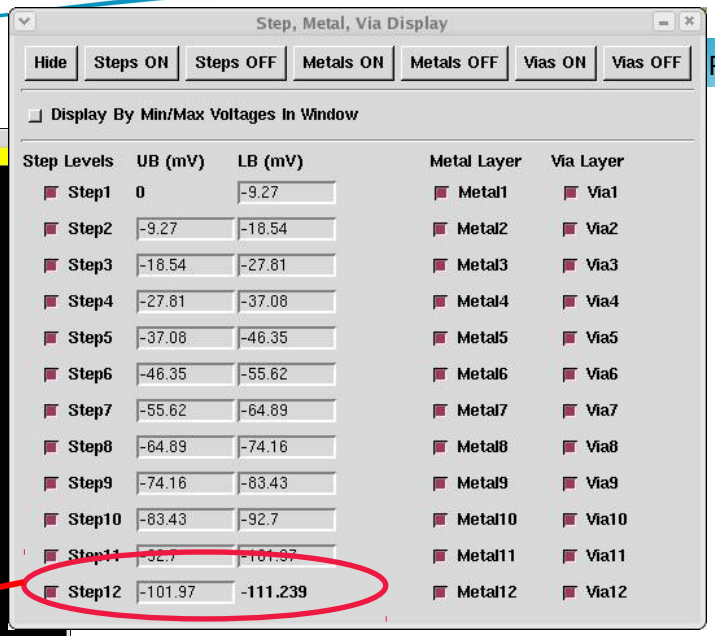
Bipolar PNP device

- **Extraction**
  - Synopsys STAR_RCXT 2007.06-SP1
- **Timing analysis**
  - Synopsys PrimeTime 2007.12-SP1
- **Formal Verification**
  - Pre- vs post-layout netlist (Cadence Conformal 7.1-isr)
- **Layout verification checks**
  - DRC
  - LVS (adapted from UMC deck)
  - ANT
  - ERC
  - SUB

Final Layout

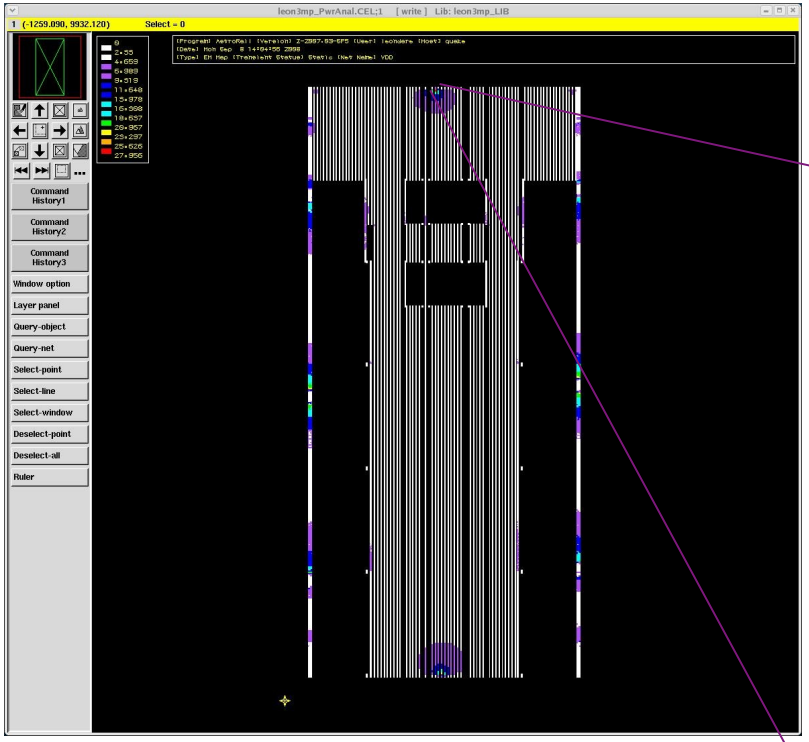




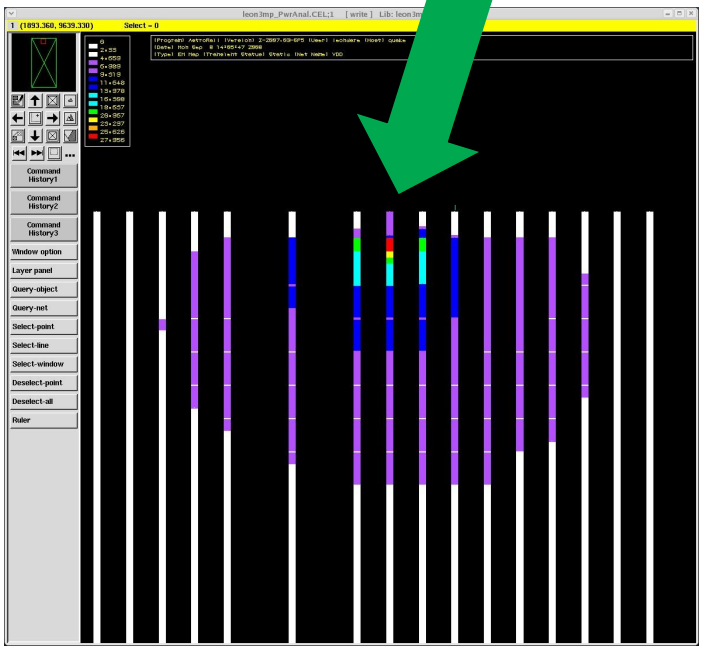


WC Mil conditions

Note: Some fixes were necessary on the power figures & rail allocations of some DARE cells.



WC EM point M4 (ok!)



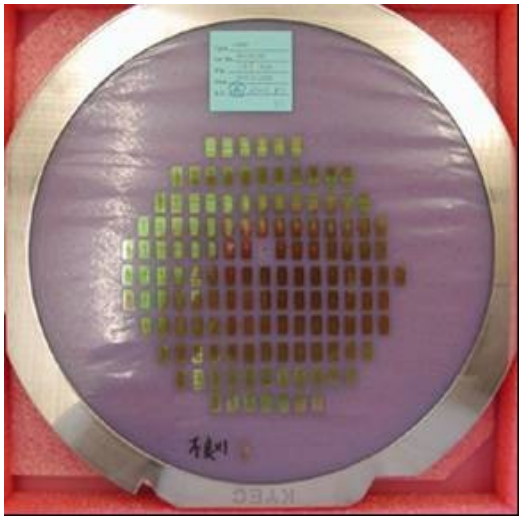
WCMil conditions
M4 = worst case

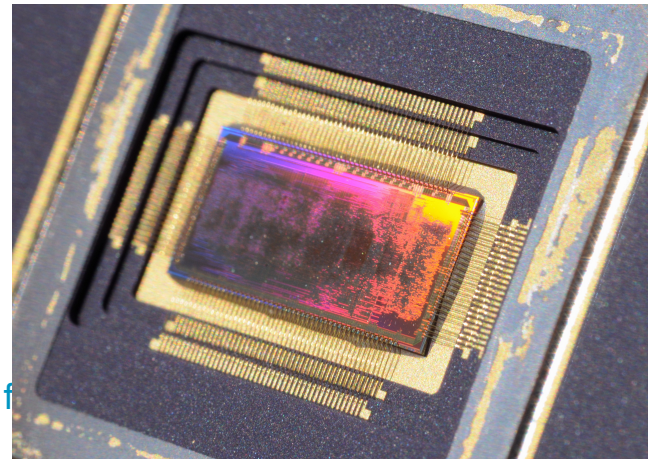
- **Synopsys Tetramax v2007.03-SP1**

- **Run on post-layout netlist**
  - Read netlist
  - Set RAMs & PLL as black boxes
  - Set test constraints
  - Define clocks
  - Define asynch reset
  - Define chains
  - Define scan enable
  - Check, generate & write reports & wgl/verilog
  - Simulate

ASIC Production

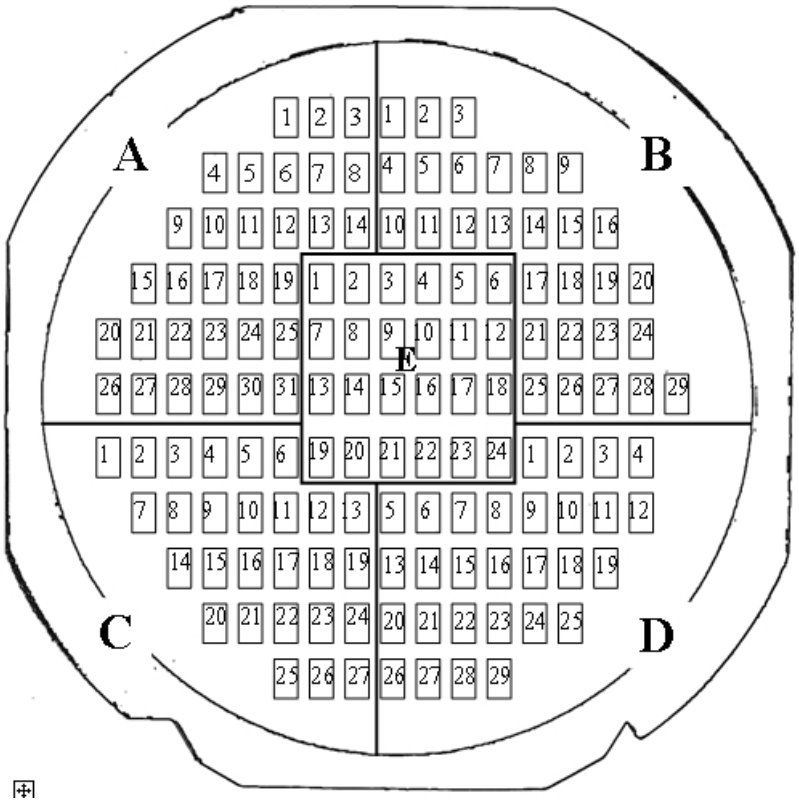
- **Ordering of 4 wafers - 11 mils thickness option – 2 diffusion lots, 160 dice initial objective**
- **Received**
  - 4 wafers – pre-sawn dice on blue foil support
  - 560 dice (only customer of the MPW run)
  - 1 diffusion lot
  - 11 mil thickness
  - Process Control Monitor
  - Certificate of Conformance
- **Not delivered, inherent to MPW run**
  - Outgoing Quality Assurance Report
  - Detailed process information (other than PCM)



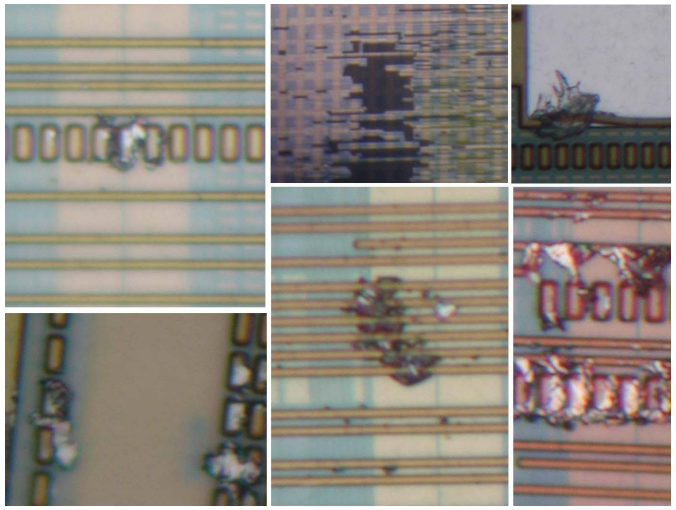


- **By HCM (Fr)**
- **Inputs**
  - 4 pre-sawn wafers on blue foil
  - 149 CQFP256 packages and lids
- **Requirements**
  - Full visual inspection of the 4 wafers and dices
  - 149 dice randomly selected through the 4 wafers f
  - Gold on Alu ball wire bonding
  - 25 µm diameter gold wires because of die pad size
  - Screening tests
    - Thermo-mechanical tests (stab bake, cycling, PIND, seal)
    - Visual inspection
- **Outputs**
  - 139 accepted units out of 149
  - Assembly yield = 93.3%

- **Internal visual inspection**
  - Necessity of traceability organization to make a link between die wafer position and assembled unit (evaluation context)



- **Internal visual inspection (continued)**
  - No die position effect observed
  - Failing parts are mainly embedded or surface particles (cleanliness) or metallization bridging

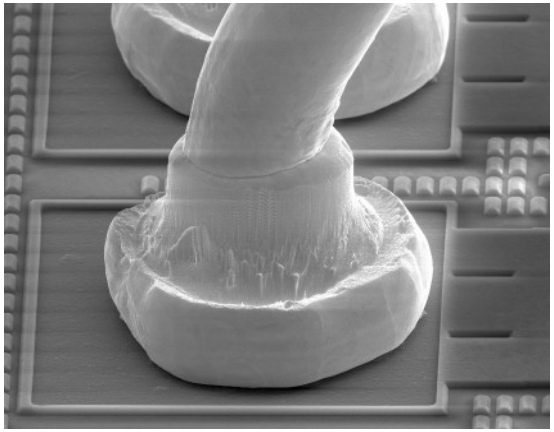


  - Package leadframe fragility : to handle with caution and dedicated tooling

- **PIND test**
  - Excessive high-level vibrations due to the package shape
    - Necessity to use a dedicated clamp for preventing it
  - All units passed the test

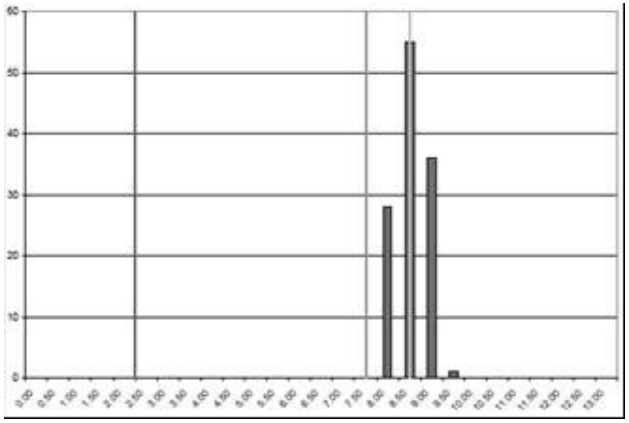
- **Seal test**
  - Required tool compatible with package size
  - All units passed the test

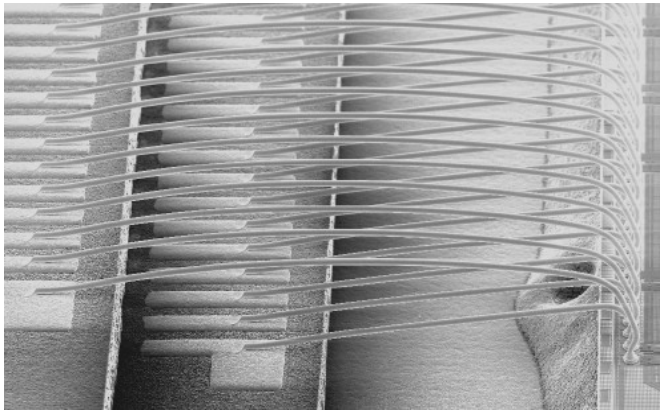
- **Performed on 3 parts**



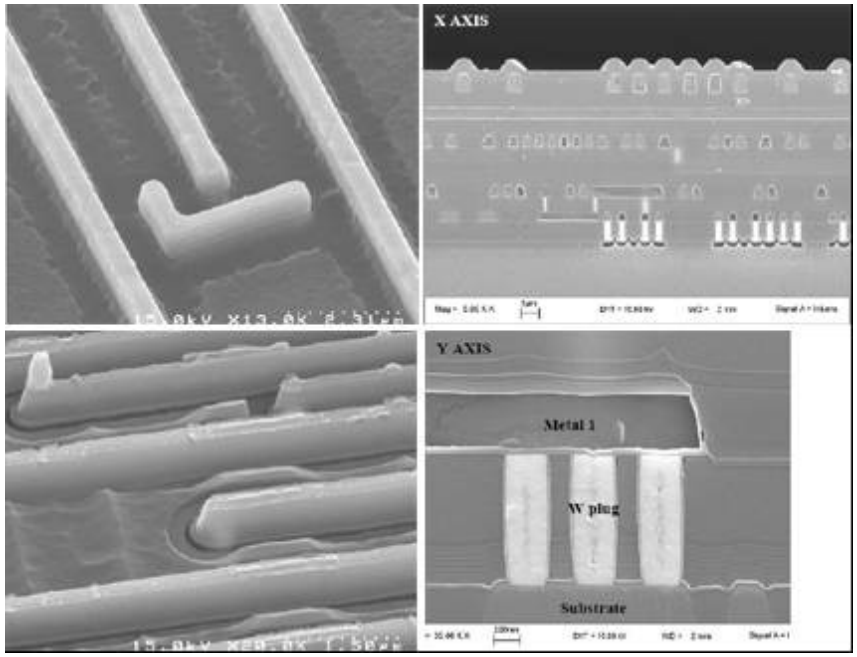
- **Results :**
  - No assembly defect was revealed
  - Internal connection were good
  - Wire pull & die shear test were correct

=> Good process control

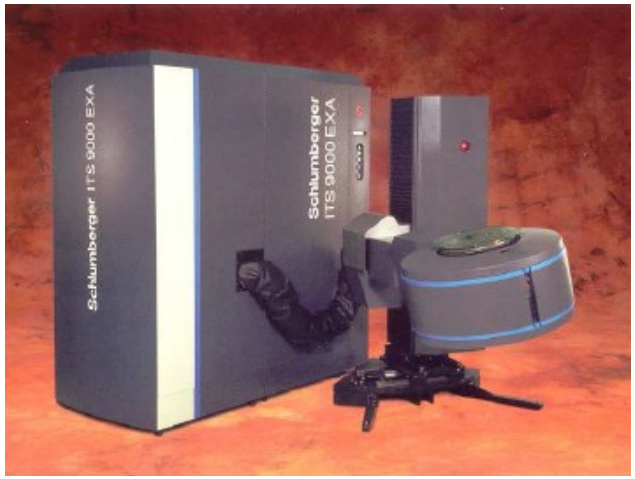




- **Internal analysis and cross-section : process geometries seem correct (visual, qualitative assessment)**



- Performed at 3 temperature (-55°C / +25°C / +125 °C)
- IO continuity tests.
- Supply currents measurement (Iccsb, Iccop)
- Static and dynamic parameters measurement (Vol/Voh/Vil/Vih,tplh,tphl)
- LVDS parameters measurements
- Scan (ATPG) and functional tests
- Equipment: Schlumberger ITS9000EXA at SERMA Fontenay-aux-Roses



- **Large RAMs for caches on LEONDARE did not work correctly. Smaller ones did.**
  - Risk identified during feasibility study and confirmed during electrical test phase
  - Simulations of full RAMs showed problem. Solution identified.
  - Problem will be corrected in upcoming compiler version.
  - Workaround by not enabling the caches by software
    - Reduced processor performance but no impact on the technology evaluation
- **High current flow at power up when Vcc IO applied before Vcc Core**
  - Reversing the power sequence reduce drastically the in-rush current
  - Problem due to internal diode protection structure that will be updated for future design
- **Power consumption estimate complied with measurements after LVDS buffer consumption was taken into account**

Electrical test production

- **Inputs**
  - 139 assembled units
- **Outputs**
  - 121 accepted units

⇒ **Test yield : 87%**

- **Failures detail**
  - 14 fails at ambient t°
  - 3 fails at 125°C
  - 1 fails at -55°C

Critical test failures at ambient temperature

Parameter	5	18	24	33	44	56	59	72	84	102	120	127	137	140
Open/Shorts														
Functional			■		■	■	■	■	■	■	■	■	■	■
Iccsba	■			■										
Iccopa	■													■
Vil							■	■		■			■	■
Iil		■												
Vol		■												■
Voh													■	■
Vth, Schmitt trigger	■	■		■		■	■	■		■	■	■	■	■
Vin, SPW							■							■
Dynamic, gates							■							■
Dynamic, registers	■	■		■		■	■	■		■	■	■	■	■
Dynamic, SPW														

Critical test failures at high temperature (+125°C) : 3

Parameter	19	21	54
Open/Shorts			
Functional			
Iccsba	■	■	■
Iccopa			
Vil			
Iil			
Vol			
Voh			
Vth, Schmitt trigger			
Vin, SPW			
Dynamic, gates			
Dynamic, registers			
Dynamic, SPW			

Critical test failures at low temperature (-55°C) : 1

Parameter	107
Open/Shorts	
Functional	■

- **Focus on current consumption parameters**

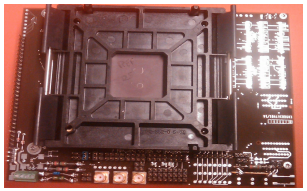
Symbol	description	Maximum value
Iccsba	Stand-by current of the core	3.7 mA
Iccsbb	Stand-by current of the IO	68 mA*
Iccopa	Dynamic consumption of the core at 50 MHz	400 mA
iil / iih	Input leakage current	338 nA

*Dominated by static consumption of LVDS buffer

Evaluation Test Results (ESCC2269000)

- **Functional tests performed in application-representative conditions on Aeroflex GAISLER GR-PCI-XC2V LEON PCI development board**

+ or



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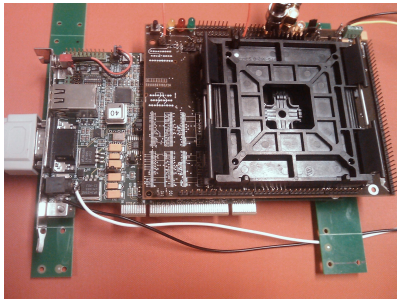
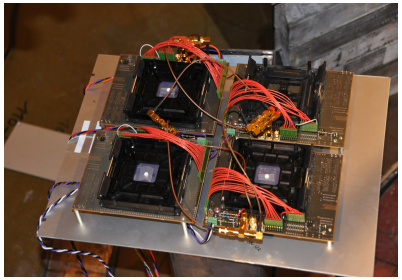
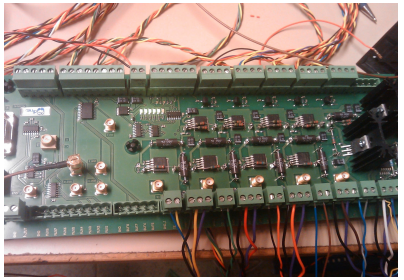


- **Schlumberger ITS9000EXA tester for post test measurements and drift calculation**

- **Dedicated test boards**





- **Power and temperature step stress test merged in one single test**
- **Performed on 5 DUT's**
  - One 168h run at 150°C: 0 defects – no significant drift
  - One 168h run at 175°C: 0 defects – no significant drift

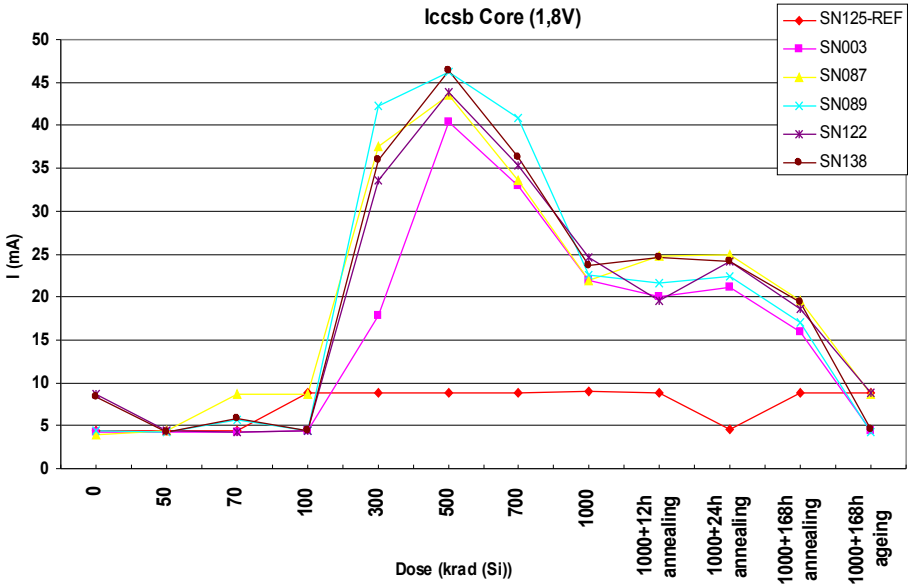
- **Thermal resistance assessment**

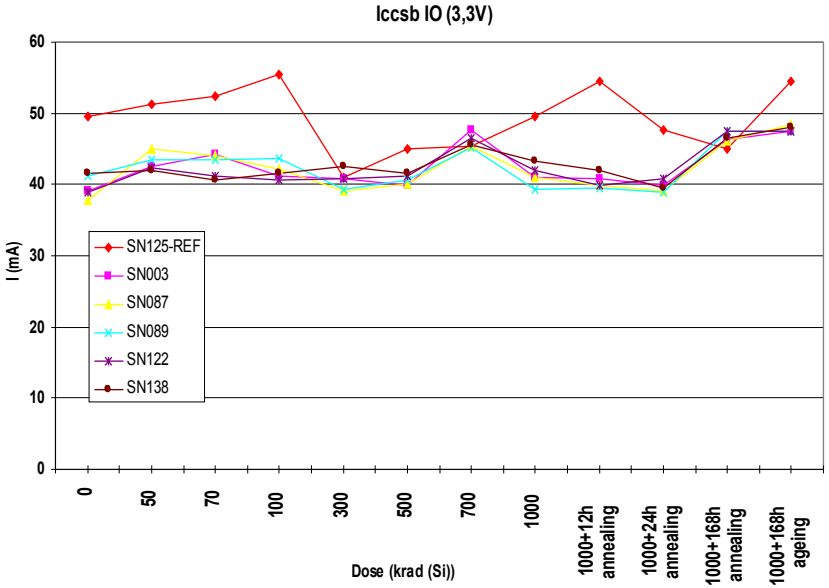
Symbol	Description	Value
Rja	thermal resistance between the semiconductor and the ambient environment	**18,73 °C/W**
Rjc	thermal resistance between the semiconductor and the top case (cover side)	**6,07 °C/W**
Rjs	thermal resistance between the semiconductor and the bottom case (substrate side)	**2,074 °C/W**

  - For space use, main parameter is junction to substrate value (drain dissipation to PBA) : 2°C/W

TID - Icc Stand-by

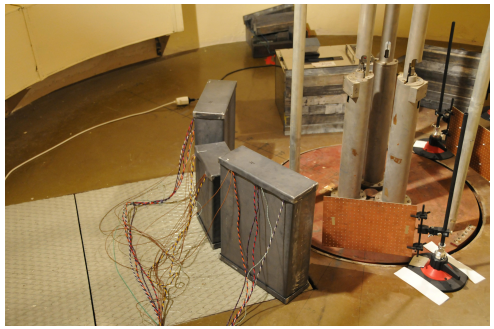
- **Icc stand-by of the core :**
  - Stable until 100 krad(Si)
  - Increase until 500 krad (Si)
  - To decrease until 1 Mrad (Si)
  - Fully recovery & functional after accelerated ageing at 100 °C

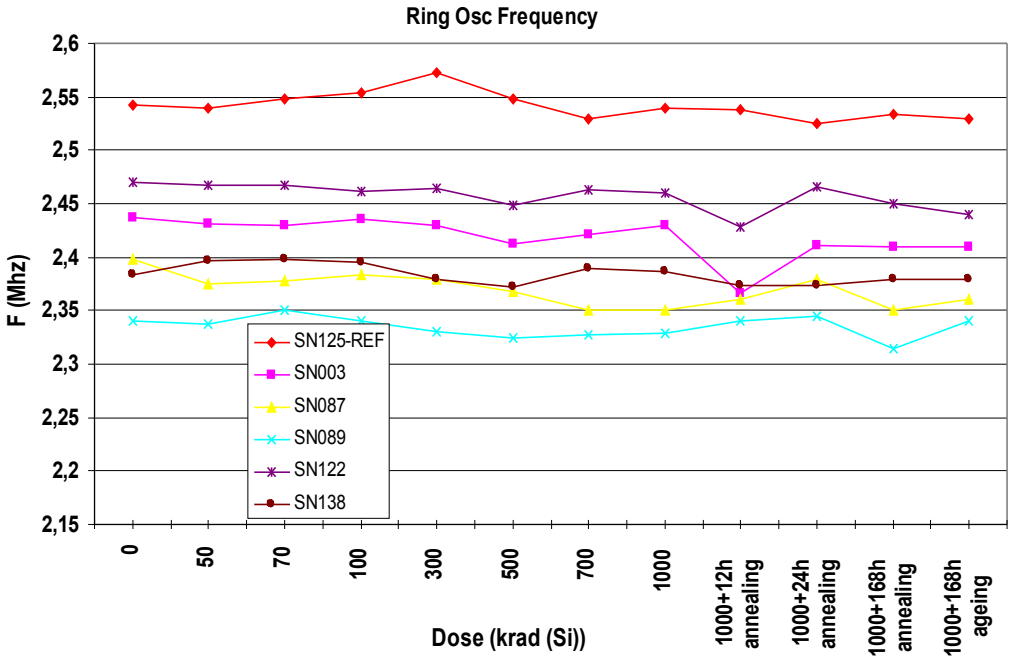




- **Icc stand-by of the IO :**
  - Dominated by the LVDS buffers consumptions
  - No significant evolution during the irradiation

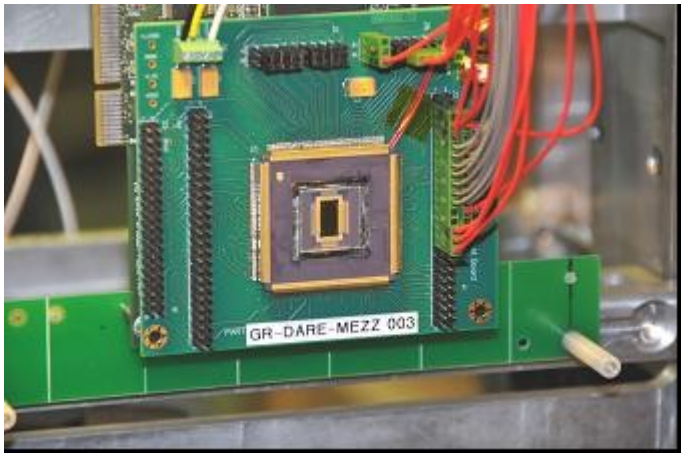
- **Timing drift :**
  - Measure of an embedded ring oscillator
  - No significant variations during and after irradiation





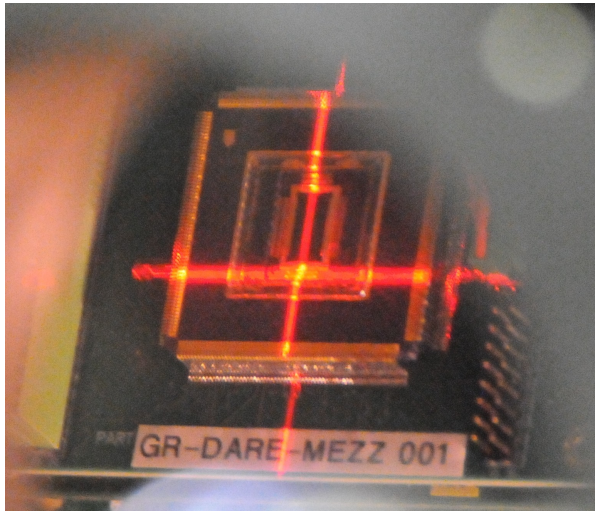
- **Cyclotron of Louvain-la-Neuve (B)**
- **Static & dynamic tests**
- **ETCA software for static test**
  - Load / unload scan chain
  - Compare the results
  - Report differences

Ion type	M/Q	Energy (MeV)	LET (MeV/mg/cm²)	Range (µm)
$^{15}N^{3+}$	5	62	**3.3**	64
$^{20}Ne^{4+}$	5	78	**6.2**	45
$^{40}Ar^{8+}$	5	150	**15.9**	42
$^{84}Kr^{17+}$	4.94	316	**40.1**	43
$^{132}Xe^{26+}$	5.07	459	**67.7**	43



- **Aeroflex Gaisler SEU32 test software for monitoring the events in dynamic mode**
  - IU Test
  - FPU test (PARANOIA)
  - GTB test : typical space application
  - SpaceWire test

- **No events detected up to 46 Mev/mg/cm2**
  - HIT cells cross-section = 1.46^{E-9} cm²/bit
- **Above 46 Mev/mg/cm2**
  - No latchup effect seen, up to 135.4 Mev/mg/cm² for a fluence = $1.10^{E}07$ ions/cm² at 125°C
  - SET effects observed and dominating

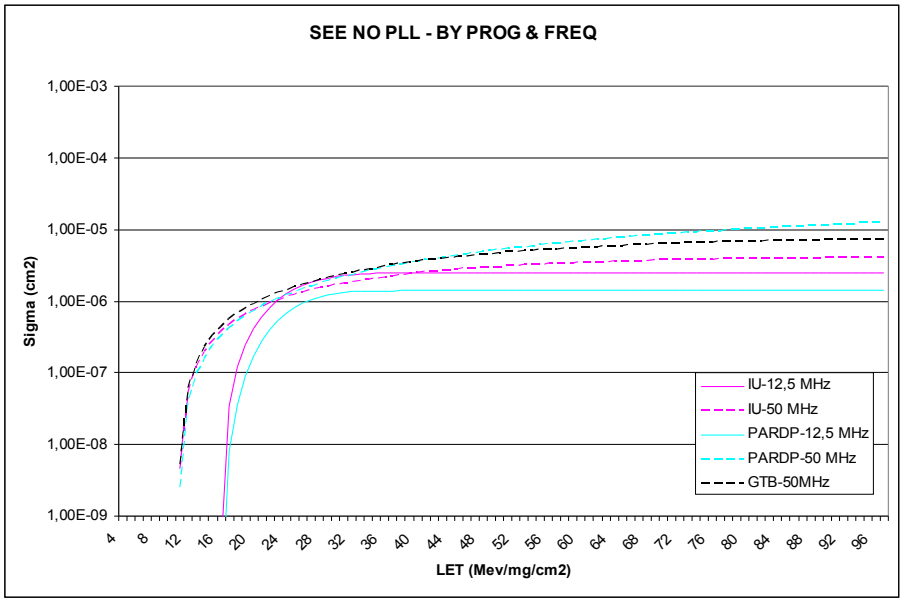


- **Tested at different frequencies**

External clock	PLL multiplication	System clock	SpaceWire clock	UART Baud Rates
50 Mhz	Bypassed	50 Mhz	50 Mhz	38400 bauds
75 Mhz	Bypassed	75 Mhz	75 Mhz	57600 bauds
12,5 Mhz	Bypassed	12,5 Mhz	12,5 Mhz	9600 bauds
12.5 Mhz	X4	50 Mhz	50 Mhz	38400 bauds
3.125 Mhz	X4	12,5 Mhz	12,5 Mhz	9600 bauds

SEE test - PLL

- **PLL Enabled**
  - Higher sensitivity to SEE



- **PLL Disabled**
  - Better behavior against SEE
  - SET dependence demonstrated

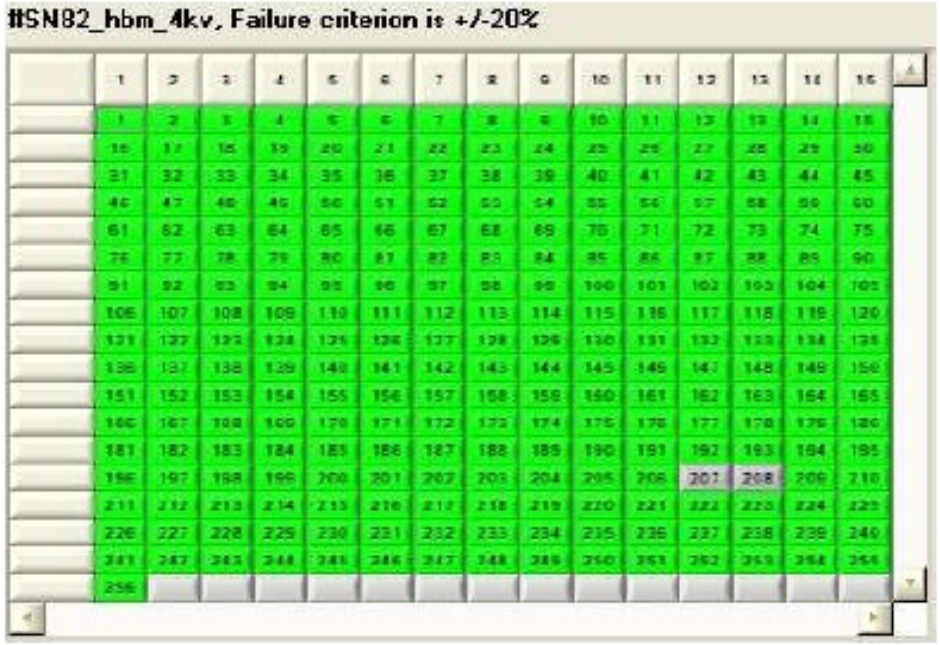
- **Upset rate calculation example**
  - Geostationary orbit (CRÈME model, m=3)

Test	Conditions	Upset rate	
		Upsets/day	Upsets/year
Static	SEL cross section	1.28E-9	1.26E-06
Static	SEU cross section	7.31E-12	2.67E-09
Dynamic	PLL enabled	5.43E-04	1.98E-01
Dynamic	PLL disabled-12.5 Mhz worst case	2.97E-07	1.07E-04
Dynamic	PLL disabled-50 Mhz worst case	4.39E-06	1.60E-03

  - 3 orders of magnitude between PLL enabled & disabled
  - 1 order of magnitude between relative low frequency & high frequency

- **Solderability & permanent marking**
  - OK
- **Mechanical shock**
  - 1500g during 0.5 ms of 3 directions (x,y,z)
  - OK – No drifts observed
- **Vibrations**
  - Frequencies from 20 Hz to 2000 Hz with 20g acceleration
  - OK – No drifts observed
- **Temperature cycling**
  - 100 cycles : -65°C/+150°C – 15 min dwell time
  - OK – No drifts observed
- **Temperature shocks**
  - 100 cycles : -65°C/+150°C – 15s transistion
  - OK – No drifts observed

- Performed on 3 DUT's
- DARE IO ESD protection embedded
- Human Body Model passed at 1 KV 2KV & 4 KV
- Post electrical tests performed after 1 KV 2KV & 4 KV stress
- Failing at 4kV (one I/O, lil)

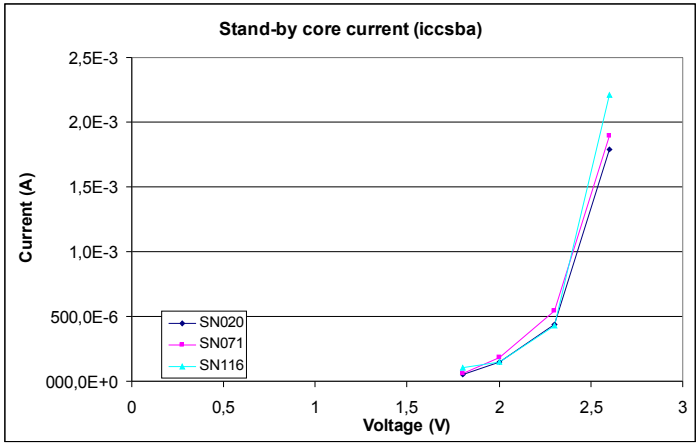


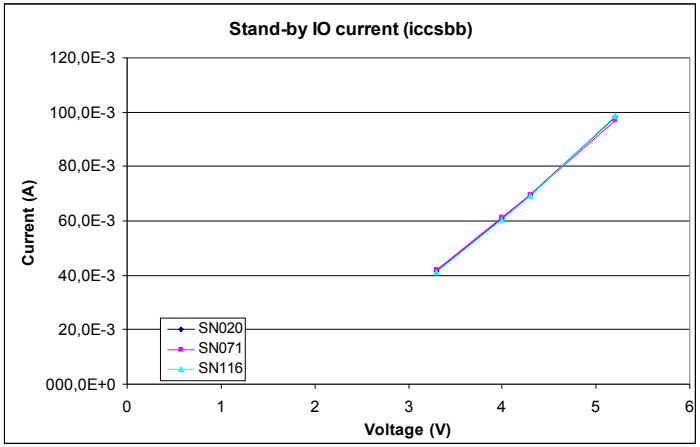
Dev SN82: HBM Test Result at 4kV

⇒ **ESD Class 3A (>4kV) device !**

Electrical Tests – Breakdown voltage

- **Maximum absolute voltage conditions**
  - Vcc core : -0.5V < Vcc core < 2.6V
  - Vcc IO : -0.5V < Vcc IO < 5.2V
- **All IO tested**
  - No damage observed at maximum rating
  - Exponential current variation for core, linear for IO





Endurance test – Conditions

- **Performed on 30 DUT's**
  - divided in 3 subgroups
  - Intermediate full electrical test with drift computation
  - Temperature of junction fixed at 150 °C according to step stress test results

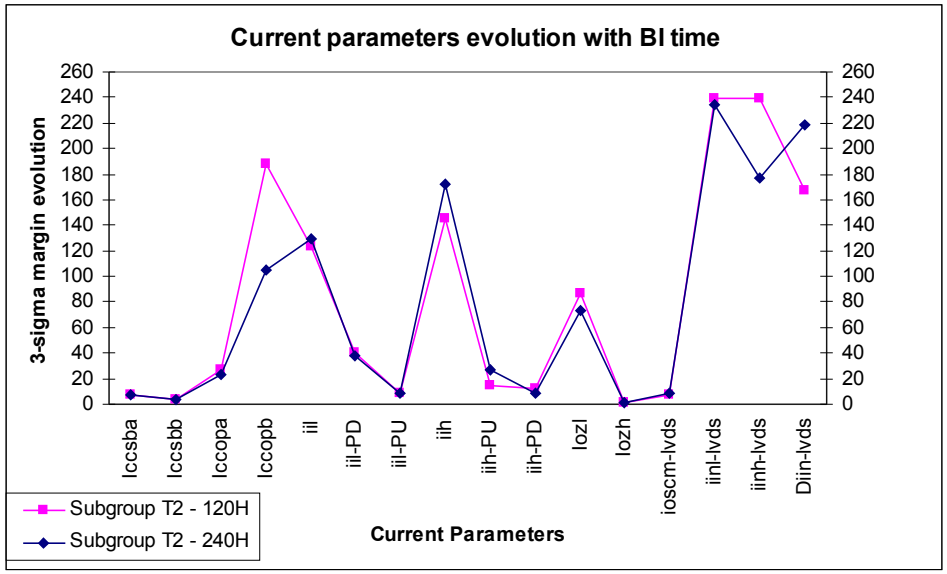
Subgroup T1 1800 hrs -150°C	Subgroup T2 240 hrs -150°C	Subgroup T3 120 hrs – 150°C
120 hrs	120 hrs	120 hrs
240 hrs	240 hrs	-
500 hrs	-	-
1000 hrs		
1800 hrs		

- **Early-life (infant mortality) failure study and long-term failures**

Endurance test – Burn-in

- **120 hrs or 240 hrs for Burn-in time?**
  - Both show parameter variation in the same range
  - All components were functional after BI
  - After 120 hrs, 3 units shown excessive σ on iozh/iil/iih in comparison with the population average.

  => 120 Hrs at 150°C is the recommended operating burn-in conditions



Endurance test – Drifts limits

- **After 1800 hrs:**
  - No functional fails
  - Maximum drift limits arbitrarily fixed
    - Minor update after statistical analysis

Parameters	Old Drift value	New Drift value	Unit
Iccsba	± 100,0E-6	± 250E-6	A
Iccsbb	± 3,0E-3	± -	A
Iccopa	± 200,0E-6	± 250E-6	A
Iccopb	± 2,0E-3	± 3,0E-3	A
iil	± 100,0E-9	± 300,0E-9	A
iil-PD	± 100,0E-9	± 1,0E-6	A
iil-PU	± 100,0E-9	± 1,0E-6	A
iih	± 100,0E-9	± 300,0E-9	A
iih-PU	± 100,0E-9	± 1,0E-6	A
iih-PD	± 100,0E-9	± 1,0E-6	A
Iozl	± 100,0E-9	± 500,0E-9	A
Iozh	± 100,0E-9	± 500,0E-9	A

Endurance test – Life prediction

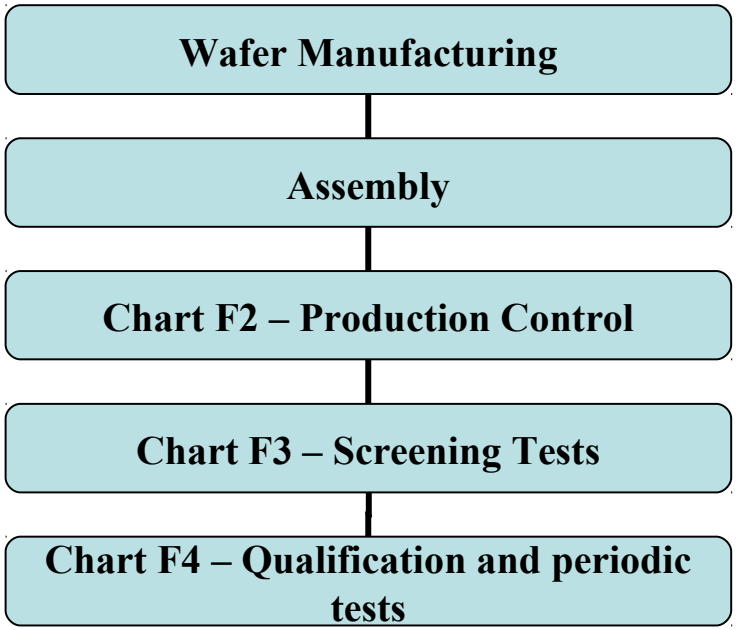
- **Conditions**
  - Vcc max operating conditions
    - IO 3.63V
    - Core 1.98V
  - Time-to-Failure prediction at 100°C
  - 60% confidence interval

MTTF > 15.3 years

- **Could be more representative by testing more components and during a longer time**

FM Procurement Flow

- **Follow the ECSS 9000 standard with few deviances**



- **Assembly flow includes some task of the Chart F2 process**
  - Internal visual inspection,
  - Bond strength
  - Die shear
  - Dimension check
  - Weight
- **Those tasks are not redone for Chart F2 – Special in-process controls**
- **Chart F3**
  - Considering the absence of wafer probe, the initial measurements (first electrical test) are also done at min/max temperatures.
- **Chart F4**
  - Power life-test at 150°C 2000 hrs on 15 units

LEON-DARE Perfomance

- **GR704 performance measurements:**
  - 112 MHz > 100 MHz system frequency
  - 236 MHz > 200 MBPS SpaceWire links, full duplex
  - 1 MBPS CAN link

  - 20 MIPS << 100 MIPS
  - The reason for the poor processor performance is the fact that the caches cannot be used due to memory cell failure.
  - The processor performance is in line with processors without caches, which are bound by the bandwidth to the external memory.
  - Comparable to an FPGA solution at 25 MHz system frequency.
  - Possible use in applications that do not permit cache usage, e.g. launchers.

Lessons learnt

- **Main improvements identified**
  - Updating the SRAM compiler for correcting the large memory generation
  - Adapting the PLL hardening against SEE
  - Improving the diode protection structures for avoiding power sequence
  - Adding a simple power consumption estimator for early in the ASIC design assesses the consumption of the chip.
  - Adding a LVDS buffer disabled pin to allow less static current consumption when not used.
  - For decreasing the SET sensitivity, designing a clock/reset tree with higher current buffers (layout recommendation) or modifying the HIT cell structure for adding SET filtering techniques.
  - Adding dual port ram generation in the SRAM compiler.

  …

- **Strong management**
  - Different companies involves in the production flow required good coordination and follow-up
- **MPW run limitation**
  - No guarantees of the compliance to customer's specific requests
  - Intend MPW ordering for prototyping, full-mask ordering for flight model and lot evaluation
- **Development of procurement of an appropriate protective antistatic packing**
- **Verifying the possibility to perform a burn-in and life test at temperature above 125°C in the used test house**
- **Increasing the life-test duration for assessing the behavior in longer space missions**

- **The project proved**
  - Excellent skills of the DARE180 library associated with the UMC 0.18µm library for space environments
    - Excellent production yield
    - Adequate radiation hardening
    - Latch-up free
    - No significant drifts after irradiation or life-test
    - Good timing performance
  - Possibility to take advantage of commercial technologies for the design of rad-hard ASICs.
  - Feasibility to produce high quality, space level ASICs using small assembly and test houses (fabless approach).

Questions ?

Thales Alenia Space in Belgium

www.thalesaleniaspace.com