CRISA Experience working with ESA IPs

- SpaceWire
- HurriCANe
SpaceWire

- **Deliverables**
  - IP configured with packets, not generics
  - Testbench defined with packets, not txt files

- **IP Interface**
  - Custom interface, not standard

- **IP Internal Structure Remarks**
  - 3 clock domains
  - Combinational logic in clock generation
  - Combinational logic inter clock domain paths
  - FPGA placing critical (Timing issues)
  - Altera Target
HurriCANe

- Deliverables
  - VHDL testbench, not compatible with VHDL source code
  - Testbench does not cover all IP functionality (Bugs Found!)

- Documentation
  - Poor description of interfaces and functionality.
  - No interfaces timing diagrams

- IP Interface
  - Custom Parallel interface
  - Data bus 2x82 signals, not optimized for physical implementation

- IP Internal Structure Remarks
  - 1 latch present in synthesis

- Bugs Found
  - Minor functional errors. (Already reported)
Proposed Improvements

• Work towards IP standard Documentation
  – Document types
  – Document contents
• Standard IP interfaces
• Follow synchronous design rules
• Minimize clock domains
• Testbench to cover all functionality
• Catalogue database