GRLIB plug&play IP library

Jiri Gaisler

Gaisler Research

jiri@gaisler.com

Background

- Gaisler Research (GR) has developed some of the larger ESA IP cores: LEON1/2, PTME, CTM, EVI32
- GR has re-used these cores in several ESA projects: HICDS, TOPNET, COLE, PROBA-2
- GR continues to develop new cores on both ESA and internal funding: GRFPU, MMU, PCI, SPW, AHBARB, LEON3
- The new cores are already being used in ESA projects: GRFPU : AGGA3/COLE, SRMMU : COLE ...
- The experience from these projects has shown that a new development and re-use method is needed

Experienced problems

- Reusing unrelated cores cause several problems:
  - Harmonisation of interfaces (on-chip buses, irq ...)
  - Merging of synthesis and simulation scripts
  - Mapping of technology specific cells (memory, pads)
  - Name space conflicts
  - Resolving CAD tool specific coding syntax
  - Licensing issues
- Problems for space applications
  - SEU hardening
  - Portability and long-term support

Proposed solution: GRLIB IP Library

- Common interfaces: AMBA + plug&play extensions
- Process portability: technology independent API
- CAD tool independent coding style
- Unified synthesis and simulation scripts
- Common H/W debug approach: GRMON + modules
- Common S/W simulation approach : GRSIM + modules
- Open and extensible format
- Multi-vendor support
- Support for FPGA prototyping
- **Open-source distribution (GPL)**