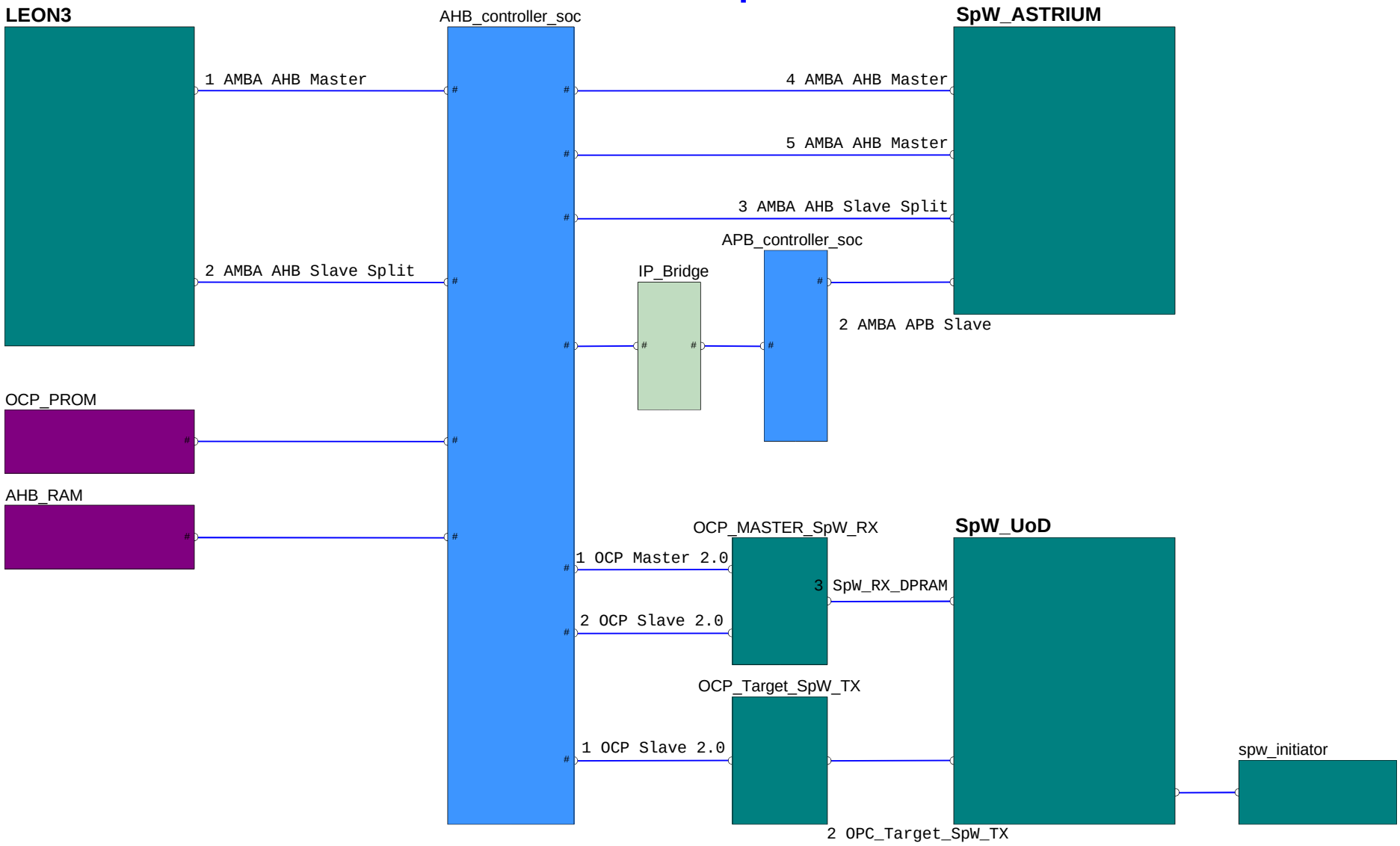
General SoC platform



Results and Conclusions

	XVC2000E	XC2V3000
System clk	**42 MHz**	**58 MHz**
SpW TX clk	**85 MHz**	**157 MHz**
SpW RX clk	**104 MHz**	**145 MHz**
BLOCKRAMs / RAMB16s	**26%**	**14%**
SLICEs	**31%**	**41%**

- SpaceWire ASTRIUM

  Very easy to integrate

- SpaceWire UoD

  Problem due to DPRAM management

- LEON3

  Many synthesis warnings

  Effects of not using AHB sideband signals