

1st ESA IP Cores Workshop

ESTEC/TEC-EDM

agustin.fernandez-leon@esa.int

AGENDA

(morning)

09.00 Welcome / presentations

09.10 The ESA IP Cores service: (ESA)

- Why , History , Steps to request, technical support, ESA IP Cores webpage

09.45 Overview of current ESA IP Cores (ESA)

- main functions, origin, use record, specific licence constraints.

10.30 *Coffee Break*

10.45 Ideas to improve the ESA IP Cores service (I: general administrative) (ALL)

- website / customer interface, IPRequest form, Licensing, Delivery of IP: lead-time / format, Fees, Collecting and sharing users feedback, Technical support.

11.30 Ideas to improve ESA IP Cores service (II: general technical) (ALL)

- technical documentation, source code, test benches, EDA tool support, precompiled simulation models, abstraction levels, bus system support.

12.30 *Lunch Break*

AGENDA

(afternoon)

13.30 ESA IP Cores user's experiences

13:30	Stephane Davy	OBSPM LESIA CNRS (France)
13:45	Franco Bigongiari	Aurelia Microelectronica (Italy)
14:00	Nicolas Renaud	Atmel (France)
14:15	Daniel Gonzalez	INTA (Spain)
14:30	Jiri Gaisler	Gaisler Research (Sweden)
14:45	Giuseppe Giachella	Laben (Italy)
15:00	Mattias Carlqvist	ESA/ESTEC (Netherlands)
15:15	Francisco Tortosa	ESA/ESTEC (Netherlands)

- feedback/experiences using ESA IP Cores
- Ideas to improve specific ESA IP Cores
- other IP Cores

16.30 Workshop conclusions / Future plans

- New IPs?, new IP versions?
- Topics not discussed this time: future workshops

ESA IP Cores Service

HISTORY

Some VHDL designs of high reuse potential were developed internally at ESA in the late 90's early 00's: CAN, LEON1/2, PTME, EDAC, etc

Some ESA contracts give IPRs to ESA to reuse and sublicense externally developed VHDL designs: OBDH, Space Wire, etc

ESA contractors started asking to re-use these IPs in ESA contracts. Also non-ESA customers.

Specific ownership/IPR, patents and ESA-third party agreements affect the use and transfer of several IPs

Growing number of requests...

2003: ESA Microelectronics section (TEC-EDM) and Electr. Eng. Contracts Service (RES-PTE) started to normalize and regulate the ESA IP Cores service: internal IP Policy, technical & admin databases, additional human resources, IP Request Form, Licence models, new web site, etc

ESA IP Cores Service

WHAT

- ① Maintain /License /Distribute several (13 now) Intellectual Property Cores (VHDL Designs + Simulation files + Documentation) frequently used in Space platforms and payloads.
- ① Collect users' feedback, communicate known problems.

WHY

achieve cheaper, faster multi-IP/S-o-C designs thanks to VHDL re-use

contribute to the availability of key digital functions (in “soft format”), mitigating ASSP/Standard ASIC components discontinuation/reluctance by foundries

promote use of standardised (ECSS) functions/communication protocols

promote the standardisation of platform and payload data communication and processing architectures

PROCUREMENT of ESA IP Cores: steps

1- Consult ESA **IP-Cores website**

(<http://www.estec.esa.nl/microelectronics/core/corepage.html>) to:

1.1 learn details on IP availability

1.2 download technical documentation (IP user's manuals, etc)

1.2 evaluate acceptance of ESA licence conditions

2 - download, fill-in and send **IP Core Request Form** (electronic copy to IPCoreRequest@esa.int, and signed fax copy to address stated inside IPRF)

3 - If all conditions are met, ESTEC/RES-PTE will send to the prospect licensee a **licence** document tailored for his/her case.

4 - TEC-EDM will send the IP Core **source-code files** to licensee upon reception at RES-PTE of accepted licensing document (i.e. bearing licensee's signatures).

ESA IP Cores ownership

AVAILABLE IP-CORES BASED ON:

- ESA-owned Intellectual Property (e.g. internal development/rights assigned to ESA)
 - ↳ ESA has full control on IP-core and how it is licensed
- Rights given to ESA through licences resulting from ESA contracts
 - ↳ ESA has the right to use/grant sub-licences;
Restrictions may apply

The above information is available on the TEC-EDM webpage.

ESA IP Cores Licence

2 TYPES OF LICENCE CURRENTLY AVAILABLE

Both types are based on the information supplied in the IP Request Form and standard licensing conditions which must be accepted by the Licensee

1 - “STANDALONE” LICENCE

- Issued for the Licensee’s “own purposes” as stated in the IP Request Form
- Issued for 2 years; renewable
- Handling fee per IP-core

2 - LICENCE ATTACHED TO AN ESA CONTRACT

- Issued limited to the objectives, scope and duration of the contract
- Free of charge

ESA IP Core Licence General conditions

http://www.estec.esa.nl/microelectronics/core/ipcore_licence_template_external.pdf

🕒 To whom:

“Non-exclusive

“Non-transferable (except explicitly agreed, i.e. sub-contractors)

“Within ESA member/participant states territory

🕒 For what:

“HDL modelling, HW manufacturing

“R&D and/or commercial

“Peaceful applications (in accordance with United Nations)

🕒 No technical support other than informing about known problems

Collecting Users' Feedback /

Reporting problems / Technical support

- ↑ All users have committed to report to ESA any errors found in the IP source code, testbenches and/or associated documentation. **PLEASE DO!!**
↳ THIS FEEDBACK IS CAPITAL TO IMPROVE THE QUALITY OF THE Ips
- ↑ This error reporting should be done directly to current “ESA IP Cores main focal point”: IPRequestForm@esa.int. ESA Technical Officers (if ESA contract) should be on copy
- ↑ Due to limited resources, ESA can NOT commit to systematic technical support. (Problems affecting ESA contracts will have priority).
- ↑ ESA commits to collect and independently assess/verify reported problems, and THEN, informing users through the ESA IP Core web site (“status notes” column in IP table).

ESA IP CORES Web site

<http://www.estec.esa.nl/microelectronics/core/corepage.html>



Microelectronics Section

Synthesizable IP-Cores Available from ESA

The following table lists the available synthesizable IP-Cores. The information is provided for general information only. For more information, please refer to the [Licencing of ESA Cores](#).

These cores are available from ESA with certain restrictions. For licensing conditions and other information, please refer to [Licencing of ESA Cores](#).

The following ESA cores are currently available or planned.

As the area depends on multiple factors (configuration of the IP, synthesis constraints etc), area figures given in the table are indicative only.

Name	Description	Status/Notes	Area
LEON2MT	The LEON2MT is the SEU fault tolerant version of the LEON2 processor. Up to 8 parallel processors of Triple Data Rate redundancy on 16 channels and stream memories are protected by TMR compatibility. Special licence restrictions apply to this IP. (more information on request).	Essence 1.0 2.0, 3.0 Y. Janssen 2.1.2 Special notes	LEON2MT area
EMV32	The EMV32 is a 32-bit VMEbus interface core designed to emulate the LEON2 processor. It is based on the VMEbus 3.0 standard and is compatible with the current set of VMEbus gate arrays. EMV32 is not a VMEbus core but a VMEbus interface core. It is designed to provide a high performance and low cost solution for high performance VMEbus applications.	available 1.0.0.0	area

Link to IP Request Form & licence conditions

Release notes, detected bugs, modifications log

IP Request Form , licence conditions

<http://www.estec.esa.nl/microelectronics/core/licensing.html>



IP Request Form

Licence text

IP Request Form

<http://www.estec.esa.nl/microelectronics/core/ESAIPRequestForm.pdf>



ESA IP Core Request Form

Fill in this form to request an IP core from the IP core library. The IP core library is a collection of IP cores that can be used in your designs. The IP core library is a collection of IP cores that can be used in your designs. The IP core library is a collection of IP cores that can be used in your designs.

II IP Core Request Information

Requester's Name		Company		The group you wish to join		Address (incl. zip)	
Title		Address		E-mail		Phone and public faxing	
Name of the IP core		Title of the core					
Version		Year		Date		IP core number	
Requester's e-mail		Requester's phone		Requester's fax		Requester's mobile	

III IP Core Description

For the name of the IP core, please refer to the IP core library. For the name of the IP core, please refer to the IP core library. For the name of the IP core, please refer to the IP core library.

IP core ID	Requester's name	IP core's name	Cost



IV IP Core Request Information

I am requesting an IP core from the IP core library. I am requesting an IP core from the IP core library. I am requesting an IP core from the IP core library.

V IP Core Request Information

I am requesting an IP core from the IP core library. I am requesting an IP core from the IP core library. I am requesting an IP core from the IP core library.

VI IP Core Request Information

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Name	Title	Signature

Overview of ESA IP Cores (I/III)

IP name	Main functions	IP origin	Licence special constraints	Requests(for ESA contracts)/Deliveries
SpaceWire (b)	ECSS-E-50-12 SpaceWire Encoder/Decoder	University of Dundee/AAE(tb)	Space applications/ STM patent notice	27(17)/17
SpaceWire- AMBA	ECSS-E-50-12 SpaceWire Encoder/Decoder with FIFOs and AMBA AHB master/slave interfaces	Astrium Velizy	STM patent notice	17(8)/12
CAN	HurriCANE: CAN core, controller, AMBA I/f	ESA internal development		16(9)/12
PTME	Complete CCSDS packet telemetry encoder, including VCM, VCA, TCE, R-S, APB, etc	ESA internal development/Ga isler Research		12(7)/10

Overview of ESA IP Cores (II/III)

IP name	Main functions	IP origin	Licence special constraints	Requests(for ESA contracts)/Deliveries
LEON2-FT	SPARC V8 32 bit microprocessor. TMR, EDAC and parity bits for SEU tolerance. No FPU, no PCI	ESA Internal development / Gaisler Research	Rad hard IC only with ATMEL	12(6)/7
CUC-CTM	CCSDS Unsegmented Code and Time Management, based on Elapsed Time services	ESA Internal development		8(7)/7
EDAC	Error Detection (double) and Correction (single) 4-64 bits codec	ESA Internal development		6(4)/4
PTCD	complete CCSDS packet telecommand decoder, based on MA28140 ASIC (GEC-Plessey)	Astrium Velizy	ESA activities only	4(3)/3

Overview of ESA IP Cores (III/III)

IP name	Main functions	IP origin	Licence special constraints	Requests(for ESA contracts)/Deliveries
PDEC	complete CCSDS packet telecommand decoder, including Command Pulse Selection and Distribution	Saab	ESA activities only	2(2)/2
OBDH	Data Handling System, PSS-04-255, On-board Communication Controller	Alcatel Espacio		2(1)/2
EVI32	ERC32 to VMEbus (IEEE 1014-1987) bus interface	ESA Internal development		2(1)/1
WIC	Wavelet Image Compression (lossy and lossless), based on Ocapi Flexwave IP	IMEC	Simulation models only, ESA activities only	1(1)/1

Ideas to improve general administration of ESA IP Cores Service

ESA IP Cores website

customer interface

IP Request form

Licensing scheme

Delivery of IP: lead-time / format

Fees

Collecting and sharing users feedback

News groups?

Technical support

Ideas to improve **general technical quality** of ESA IP Cores

Technical documentation

Source code

Test benches / simulation scripts

EDA tool support

precompiled models

Different abstraction levels (RTL, behavioral, transaction...)

Bus system support

Workshop conclusions / future plans (1/4)

Improving administrative aspects

-Website

-Lalal

Workshop conclusions / future plans (2/4)

Improving general technical aspects

-Source code

-EDA support

Workshop conclusions / future plans (3/4)

Improving IP specific technical aspects

- SpWb
- CAN
- LEON
- PTME
- PTCD
- PDEC
- EDAC
- CUC-CTM
- WIC

Workshop conclusions / future plans (4/4)

Next workshop

-Website

-Lalal