1st ESA IP Cores Workshop

ESTEC/TEC-EDM
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AGENDA
(morning)

09.00 Welcome / presentations

09.10 The ESA IP Cores service: (ESA)
- Why, History, Steps to request, technical support, ESA IP Cores webpage

09.45 Overview of current ESA IP Cores (ESA)
- main functions, origin, use record, specific licence constraints.

10.30 Coffee Break

10.45 Ideas to improve the ESA IP Cores service (I: general administrative) (ALL)
- website / customer interface, IPRequest form, Licensing, Delivery of IP: lead-time / format, Fees, Collecting and sharing users feedback, Technical support.

11.30 Ideas to improve ESA IP Cores service (II: general technical) (ALL)
- technical documentation, source code, test benches, EDA tool support, precompiled simulation models, abstraction levels, bus system support.

12.30 Lunch Break
13.30  ESA IP Cores user's experiences

13:30  Stephane Davy  OBSPM LESIA CNRS (France)
13:45  Franco Bigongiari  Aurelia Microelectronica (Italy)
14:00  Nicolas Renaud  Atmel (France)
14:15  Daniel Gonzalez  INTA (Spain)
14:30  Jiri Gaisler  Gaisler Research (Sweden)
14:45  Giuseppe Giachella  Laben (Italy)
15:00  Mattias Carlqvist  ESA/ESTEC (Netherlands)
15:15  Francisco Tortosa  ESA/ESTEC (Netherlands)

- feedback/experiences using ESA IP Cores
- Ideas to improve specific ESA IP Cores
- other IP Cores

16.30  Workshop conclusions / Future plans

- New IPs?, new IP versions?
- Topics not discussed this time: future workshops
Some VHDL designs of high reuse potential were developed internally at ESA in the late 90’s early 00’s: CAN, LEON1/2, PTME, EDAC, etc

Some ESA contracts give IPRs to ESA to reuse and sublicense externally developed VHDL designs: OBDH, Space Wire, etc

ESA contractors started asking to re-use these IPs in ESA contracts. Also non-ESA customers.

Specific ownership/IPR, patents and ESA-third party agreements affect the use and transfer of several IPs

Growing number of requests…

2003: ESA Microelectronics section (TEC-EDM) and Electr. Eng. Contracts Service (RES-PTE) started to normalize and regulate the ESA IP Cores service: internal IP Policy, technical & admin databases, additional human resources, IP Request Form, Licence models, new web site, etc
**ESA IP Cores Service**

**WHAT**

- Maintain /License /Distribute several (13 now) Intellectual Property Cores (VHDL Designs + Simulation files + Documentation) frequently used in Space platforms and payloads.
- Collect users’ feedback, communicate known problems.

**WHY**

Achieve cheaper, faster multi-IP/S-o-C designs thanks to VHDL re-use

Contribute to the availability of key digital functions (in “soft format”), mitigating ASSP/Standard ASIC components discontinuation/reluctance by foundries

Promote use of standardised (ECSS) functions/communication protocols

Promote the standardisation of platform and payload data communication and processing architectures
PROCUREMENT of ESA IP Cores: steps

1- Consult ESA IP-Cores website
(http://www.estec.esa.nl/microelectronics/core/corepage.html) to:
   1.1 learn details on IP availability
   1.2 download technical documentation (IP user’s manuals, etc)
   1.2 evaluate acceptance of ESA licence conditions

2 - download, fill-in and send IP Core Request Form (electronic copy to IPCoreRequest@esa.int, and signed fax copy to address stated inside IPRF)

3 - If all conditions are met, ESTEC/RES-PTE will send to the prospect licensee a licence document tailored for his/her case.

4 - TEC-EDM will send the IP Core source-code files to licensee upon reception at RES-PTE of accepted licensing document (i.e. bearing licensee’s signatures).
ESA IP Cores ownership

AVAILABLE IP-CORES BASED ON:

- ESA-owned Intellectual Property (e.g. internal development/rights assigned to ESA)
  - ESA has full control on IP-core and how it is licensed

- Rights given to ESA through licences resulting from ESA contracts
  - ESA has the right to use/grant sub-licences; Restrictions may apply

The above information is available on the TEC-EDM webpage.
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ESA IP Cores Licence

2 TYPES OF LICENCE CURRENTLY AVAILABLE

Both types are based on the information supplied in the IP Request Form and standard licensing conditions which must be accepted by the Licensee.

1 - “STANDALONE” LICENCE

• Issued for the Licensee’s “own purposes” as stated in the IP Request Form
• Issued for 2 years; renewable
• Handling fee per IP-core

2 - LICENCE ATTACHED TO AN ESA CONTRACT

• Issued limited to the objectives, scope and duration of the contract
• Free of charge
ESA IP Core Licence General conditions

http://www.estec.esa.nl/microelectronics/core/ipcore_licence_template_external.pdf

❖ To whom:
“Non-exclusive
“Non-transferable (except explicitly agreed, i.e. sub-contractors)
“Within ESA member/participant states territory

❖ For what:
“HDL modelling, HW manufacturing
“R&D and/or commercial
“Peaceful applications (in accordance with United Nations)

❖ No technical support other than informing about known problems
Collecting Users’ Feedback / Reporting problems / Technical support

☒ All users have committed to report to ESA any errors found in the IP source code, testbenches and/or associated documentation. PLEASE DO!!
☒ THIS FEEDBACK IS CAPITAL TO IMPROVE THE QUALITY OF THE Ips

☒ This error reporting should be done directly to current “ESA IP Cores main focal point”: IPRequestForm@esa.int. ESA Technical Officers (if ESA contract) should be on copy

☒ Due to limited resources, ESA can NOT commit to systematic technical support. (Problems affecting ESA contracts will have priority).

☒ ESA commits to collect and independently assess/verify reported problems, and THEN, informing users through the ESA IP Core web site (“status notes” column in IP table).
ESA IP CORES Web site

http://www.estec.esa.nl/microelectronics/core/corepage.html

Link to IP Request Form & licence conditions

Release notes, detected bugs, modifications log
IP Request Form, licence conditions

http://www.estec.esa.nl/microelectronics/core/licensing.html
IP Request Form

http://www.estec.esa.nl/microelectronics/core/ESAIPRequestForm.pdf
<table>
<thead>
<tr>
<th>IP name</th>
<th>Main functions</th>
<th>IP origin</th>
<th>Licence special constraints</th>
<th>Requests (for ESA contracts)/Deliveries</th>
</tr>
</thead>
<tbody>
<tr>
<td>SpaceWire (b)</td>
<td>ECSS-E-50-12 SpaceWire Encoder/Decoder</td>
<td>University of Dundee/AAE(tb)</td>
<td>Space applications/STM patent notice</td>
<td>27(17)/17</td>
</tr>
<tr>
<td>SpaceWire-AMBA</td>
<td>ECSS-E-50-12 SpaceWire Encoder/Decoder with FIFOs and AMBA AHB master/slave interfaces</td>
<td>Astrium Velizy</td>
<td>STM patent notice</td>
<td>17(8)/12</td>
</tr>
<tr>
<td>CAN</td>
<td>HurriCANe: CAN core, controller, AMBA I/f</td>
<td>ESA internal development</td>
<td></td>
<td>16(9)/12</td>
</tr>
<tr>
<td>PTME</td>
<td>Complete CCSDS packet telemetry encoder, including VCM, VCA, TCE, R-S, APB, etc</td>
<td>ESA internal development/Gaisler Research</td>
<td></td>
<td>12(7)/10</td>
</tr>
</tbody>
</table>
### Overview of ESA IP Cores (II/III)

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>LEON2-FT</td>
<td>SPARC V8 32 bit microprocessor. TMR, EDAC and parity bits for SEU tolerance. No FPU, no PCI</td>
<td>ESA Internal development / Gaisler Research</td>
<td>Rad hard IC only with ATMEL</td>
<td>12(6)/7</td>
</tr>
<tr>
<td>CUC-CTM</td>
<td>CCSDS Unsegmented Code and Time Management, based on Elapsed Time services</td>
<td>ESA Internal development</td>
<td></td>
<td>8(7)/7</td>
</tr>
<tr>
<td>EDAC</td>
<td>Error Detection (double) and Correction (single) 4-64 bits codec</td>
<td>ESA Internal development</td>
<td></td>
<td>6(4)/4</td>
</tr>
<tr>
<td>PTCD</td>
<td>complete CCSDS packet telecommand decoder, based on MA28140 ASIC (GEC-Plessey)</td>
<td>Astrium Velizy</td>
<td>ESA activities only</td>
<td>4(3)/3</td>
</tr>
</tbody>
</table>
## Overview of ESA IP Cores (III/III)

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</tr>
</thead>
<tbody>
<tr>
<td>PDEC</td>
<td>Complete CCSDS packet telecommand decoder, including Command Pulse Selection and Distribution</td>
<td>Saab</td>
<td>ESA activities only</td>
<td>2(2)/2</td>
</tr>
<tr>
<td>OBDH</td>
<td>Data Handling System, PSS-04-255, On-board Communication Controller</td>
<td>Alcatel Espacio</td>
<td></td>
<td>2(1)/2</td>
</tr>
<tr>
<td>EVI32</td>
<td>ERC32 to VMEbus (IEEE 1014-1987) bus interface</td>
<td>ESA Internal development</td>
<td></td>
<td>2(1)/1</td>
</tr>
<tr>
<td>WIC</td>
<td>Wavelet Image Compression (lossy and lossless), based on Ocap Flexwave IP</td>
<td>IMEC</td>
<td>Simulation models only, ESA activities only</td>
<td>1(1)/1</td>
</tr>
</tbody>
</table>
Ideas to improve general administration of ESA IP Cores Service

ESA IP Cores website
customer interface
IP Request form
Licensing scheme
Delivery of IP: lead-time / format
Fees
Collecting and sharing users feedback
News groups?
Technical support
Ideas to improve
general technical quality of
ESA IP Cores

Technical documentation
Source code
Test benches / simulation scripts
EDA tool support
precompiled models
Different abstraction levels (RTL, behavioral, transaction…)
Bus system support
Workshop conclusions / future plans (1/4)

Improving administrative aspects

- Website
- Lalal
Workshop conclusions / future plans (2/4)

Improving general technical aspects

- Source code
- EDA support
Workshop conclusions / future plans (3/4)

Improving IP specific technical aspects

- SpWb
- CAN
- LEON
- PTME
- PTCD
- PDEC
- EDAC
- CUC-CTM
- WIC
Workshop conclusions / future plans (4/4)

Next workshop

- Website
- Lalal