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from/*de* Roland Weigand	visa/*visa*	
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Subject/*objet* EDAC core overview release 0.6

Specification of the EDAC's

The package contains Error Detection And Correction encoders/decoders for various word lengths. All codecs have separate parity calculation for check bit generation and error detection/correction. All codes have a single correctable error indicator, a double correctable error indicator, and a multiple uncorrectable error indicator. However, only one of the codecs supports DEC (double error correction). Details concerning the algorithms can be found in the references below.

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0) Hamming EDAC codec, with SEC-DED capability over 4 bit
1) Hamming EDAC codec, with SEC-DED capability over 8 bit
2) Cyclic EDAC codec, with DEC-EED capability over 8 bit
3) Hamming EDAC codec, with SEC-DED capability over 16 bit
4) Hamming EDAC codec, with SEC-DED-SBD capability over 16 bit
5) Hamming EDAC codec, with SEC-DED capability over 24 bit
6) Hamming EDAC codec, with SEC-DED capability over 32 bit
7) Hamming EDAC codec, with SEC-DED-SBD capability over 32 bit
8) Hamming EDAC codec, with SEC-DED capability over 40 bit
9) Hamming EDAC codec, with SEC-DED capability over 48 bit
10) Hamming EDAC codec, with SEC-DED capability over 64 bit
11) Hamming EDAC codec, with SEC capability over 57 bit (also C-model)

DEC Double Error Correction
DED Double Error Detection
EED Extended Error Detection
SBD Single Bank-error Detection (Strong)
SEC Single Error Correction
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Content of the design package

The code is presented in form of a library of procedures and an entity, which instantiates one of the EDAC-procedures of the list above, depending on a generic parameter. The EDAC's are purely combinational; no flip-flops are implemented. It is the user's responsibility to embed them in the appropriate pipelining structure.

A test bench is part of the package, which simulates the different EDAC types using random data. The extent of the tests is configurable by the means of generic parameters.

As of version 0-6, a precompiled Modelsim simulation model is available for download. The package body is encrypted to protect the IP, but the package declaration is joined in VHDL to allow interfacing with user designs.

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