**ESA 13345/#3 : Building Block for System On a chip**

# PACKET TELECOMMANDE DECODER VHDL CORE
## SPECIFICATION ICD

| | Name and Function | Date | Signature |
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## TABLE OF CONTENTS

# 1 SCOPE

The goal of this document is not to provide the specification of the PTCD.

As the PTCD has been modified into an IP core, this document aims to specify the new I/O interface and to detail the added functions such as the AMBA interfaces and the MAP CPU interrupt.

# 2 DOCUMENTS AND ACRONYMS

## 2.1 APPLICABLE DOCUMENTS

| | | |
| --- | --- | --- |
| AD1 | *MA28140 Packet telecommand Decoder* | GEC Plessey Semiconductors<br>February 1995 |

## 2.2 REFERENCE DOCUMENTS

| | | |
| --- | --- | --- |
| RD1 | HKPF VHDL Core Description | R&D-SOC-NT-291-V-ASTR |

## 2.3 ACRONYMS

AD Applicable Document
ASIC : Application Specific Integrated Circuit
ASSP : Application Specific Standard Product
AU : Authentication Unit
CPDU : Command Pulse Distribution Unit
DFF : D-Type Flip Flop
DMA Direct Memory Access
DSR : Data Signal Ready
DTR : Data Transmission Ready
ESA European Space Agency
ESTEC European Space Research and Technology Centre
FAR : Frame Analysis Report
FPGA Field Programmable Gate Array
FSM Finite State Machine
HiRel : High Reliability
HKPF : HouseKeePing Function
IP Intellectual Property
IT Interrupt
ITT : Invitation To Tender
LAC : Logical Authentication Channel
LAC1 : Logical Authentication Channel number 1
LAC2 : Logical Authentication Channel number 2
LFSR : Linear Feedback Shift Register
MAP : Multiplexed Access Point
PCB : Printed Circuit Board
PTCD : Packet Telecommand Decoder ASIC.
PTD : Packet Telecommand Decoder ASIC.
RD Reference Document
SOC System-On-a-Chip
SCoC Spacecraft Controller on a Chip
TC : Telecommand
TM : Telemetry
VLSI : Very Large Scale Integration (component)
WP : Work Package

# 3 DESCRIPTION OF THE PTCD MODIFICATIONS

## 3.1 FUNCTIONAL MODIFICATIONS SPECIFIED IN THE PTD TO PTCD TRANSFER

The use of the PTD by Astrium in their equipments did not put in evidence any bugs. Nevertheless in 1998, the opportunity to make the portation of the PTD into a new technology leads Astrium to propose to ESA the following modifications.

In some cases it is necessary to start the PTD with the Authentication Unit disable, and then after receipt of frames to switch on the internal Authentication Unit (AU). Is such operational mode is used, the LAC1 and LAC2 counters are not initialized and in an unknown state when switching to internal AU enable mode. It is not a major problem, since the value of these LAC counters can be obtained by an AU status telemetry report when the internal AU is operational, and since it is always possible to run the PTD with the recovery LAC counter.

Modification 1 is thus : the PTCD shall initialize the LAC1 and LAC2 counters when AU is disabled.

When the PTD is operating in parallel mode, the MAP output is delivered on the PBUS 16 bit parallel bus. But the number of words in not known a priori by the microprocessor. A DMA transfer is possible but the number of words must be defined as the maximum number of words of the transfer, and the transfer has to be stopped when MAPDSR is deactivated. Providing the MAP number of words in parallel mode is an improvement.

Modification 2 is thus : The PTCD shall provide on the 8 MSB bits of the MAP status, the number of words that will be output by the MAP interface in parallel mode. This number of words shall be valid only when MAPDSR is active, i.e. when bit 0 of the MAP status is active, otherwise it will be set to FFFF or 00000 (TBC).

Some project requirements arise asking a higher TC rate of the PTD. It is very difficult to change the internal PTD structure to improve the TC rate. But by changing the technology, and since synthesis tools are improved, a higher operating frequency of the PTCD shall be achieved. The PTD was running at 4 MHz. Pre Layout Synopsys synthesis results show that the PTCD runs at about 10 MHz with MITEL technology. As expressed above, the increase of speed of the PTCD is not obtained by architectural modifcations but only by technology changes.

Modification 3 : The PTCD shall be designed and simulated at about 9 MHz. The PTCD shall be compliant with the PTD when running at PTD specified frequencies.

### 3.2 OTHER MODIFICATIONS SPECIFIED IN THE PTD TO PTCD TRANSFER

MITEL requests the implementation of a nand tree to test the ASIC inputs, and of a test of the output buffers.

The internal tri-state buffers are replaced by nand structures since implementing internal tri-state buffers is not easy in MITEL technology.

The VHDL code of the PTCD changed also compared to the PTD, since the PTD was synthetized with Autologic, and the PTCD is synthetized with Synopsys.

### 3.3 MODIFICATION BETWEEN THE PTCD AND THE DATABASE DELIVERED IN COO3

Astrium made the following modifications in order to make the PTCD database easier to use, either in a new ASIC design or as IP core in a SOC.

- The NAND tree asked by MITEL to test the I/O pads is removed,
- The internal BIST and test modes activated only in the foundry test program for fault coverage are removed,
- The extra protocols PSS45 and SVE are removed,
- The MITEL pads are replaced by generic pads provided with their VHDL models.

It must be noticed that the general reset of the circuit is unchanged. It is a synchronous reset chosen for foundry constraints. Synchronous reset has its advantages and drawbacks.

The operating frequency depends on the technology chosen for manufacturing. It can be expected more than 20 MHz in MG2RT ATMEL technology for example.

### 3.4 MODIFICATION OF THE PTCD IP TO BE INTEGRATED IN THE SCOC MODULE

The following modifications have been performed.

### 3.4.1 The I/O Memory interface

The access to the memory is performed through the following AHB interface:

- ahb_mst_in : AHB master inputs
- ahb_mst_out : AHB master outputs

The data bus is 8 bits in width. The address bus is 11 bits in width.
The memory mapping is shown hereafter:

| **RAM** | **Start Address**<br>000 | **End Address**<br>7FF |
|---|---|---|
| Buffer0-(front end/back end) (see note 1) | 000 | 0FF |
| Buffer1-(back end/front end) (see note 1) | 100 | 1FF |
| Programmable key - Knapsack | 200 | 367 |
| Programmable key - Hashing | 368 | 36F |
| Internal use (reserved) | 370 | 373 |
| Free | 374 | 3FF |
| 8 LSB of Recovery LAC | 400 | 400 |
| Internal use (reserved) | 401 | 401 |
| Auxiliary LAC Counter - octet 4 LSB | 402 | 402 |
| Auxiliary LAC Counter - octet 3 | 403 | 403 |
| Auxiliary LAC Counter - octet 2 | 404 | 404 |
| Auxiliary LAC Counter - octet 1 MSB | 405 | 405 |
| Primary LAC Counter - octet 4 LSB | 406 | 406 |
| Primary LAC Counter - octet 3 | 407 | 407 |
| Primary LAC Counter - octet 2 | 408 | 408 |
| Primary LAC Counter - octet 1 MSB | 409 | 409 |
| Free | 40A | 40F |
| AUS octet 10 - buffer 0 | 410 | 410 |
| AUS octet 9 - buffer 0 | 411 | 411 |
| AUS octet 8 - buffer 0 | 412 | 412 |
| AUS octet 7 - buffer 0 | 413 | 413 |

| **RAM** (continued) | **Start Address** | **End Address** |
|---|---|---|
| AUS octet 6 - buffer 0 | 414 | 414 |
| AUS octet 5 - buffer 0 | 415 | 415 |
| AUS octet 4 - buffer 0 | 416 | 416 |
| AUS octet 3 - buffer 0 | 417 | 417 |
| AUS octet 2 - buffer 0 | 418 | 418 |
| AUS octet 1 - buffer 0 | 419 | 419 |
| FAR octet 4 - buffer 0 | 41A | 41A |
| FAR octet 3 - buffer 0 | 41B | 41B |
| FAR octet 2 - buffer 0 | 41C | 41C |
| FAR octet 1 - buffer 0 | 41D | 41D |
| Free | 41E | 42F |
| AUS octet 10 - buffer 1 | 430 | 430 |
| AUS octet 9 - buffer 1 | 431 | 431 |
| AUS octet 8 - buffer 1 | 432 | 432 |
| AUS octet 7 - buffer 1 | 433 | 433 |
| AUS octet 6 - buffer 1 | 434 | 434 |
| AUS octet 5 - buffer 1 | 435 | 435 |
| AUS octet 4 - buffer 1 | 436 | 436 |
| AUS octet 3 - buffer 1 | 437 | 437 |
| AUS octet 2 - buffer 1 | 438 | 438 |
| AUS octet 1 - buffer 1 | 439 | 439 |
| FAR octet 4 - buffer 1 | 43A | 43A |
| FAR octet 3 - buffer 1 | 43B | 43B |
| FAR octet 2 - buffer 1 | 43C | 43C |
| FAR octet 1 - buffer 1 | 43D | 43D |
| Free | 43E | 5FF |
| CPDU buffer (see note 2) | 600 | 6FF |
| Free | 700 | 7FF |

**Figure 1: RAM mapping**

Note 1 : The addresses 000 and 100 contain the buffer length (X) and the first word of the frame are stored at address X, respectively 100+X; the last word is stored at address 001, respectively 101.

Note 2 : The address 600 contains the CPDU buffer length (X) and the first word of the frame is stored at address 600+X; the last word is stored at address 601.

| **ROM** | **Start Address**<br>000 | **End Address**<br>3FF |
|---|---|---|
| Frame Header octet 1(see note 3) | 000 | 000 |
| Frame Header octet 2(see note 3) | 001 | 001 |
| Frame Header octet 3(see note 3) | 002 | 002 |
| FARM PW' = PW - 1(see note 4) | 003 | 003 |
| FARM NW' = 255 - NW(see note 4) | 004 | 004 |
| Authenticated MAP ID pointer (see note 5) | 005 | 005 |
| CPDU Packet Header octet 1 and 2 (see note 6) | 006 | 007 |
| Free | 008 | 0FF |
| MAP frequency table as defined in section 5.1.2 | 100 | 13F |
| Free | 140 | 1FF |
| Fixed key - Knapsack (see note 7) | 200 | 367 |
| Fixed key- Hashing (see note 8) | 368 | 36F |
| Free | 370 | 3FF |

**Figure 2: ROM mapping**

Note 3 : These 3 octets contain all the fields of the Frame Header including reserved bits and version bits. Bypass and Control flags (in Frame Header octet 1) form the only field that is not a fixed value : the value of these 2 bits in PROM has no influence on the PTD operation (default value = 00).

Note 4 :

In order to facilitate the implementation of the FARM Sliding Window Concept in the PTD, the values stores in the PROM are not PW and NW but :

- PW' = PW - 1
- NW' = 255 - NW

The PW' and NW' numbers can be any value between 0 and 255.

Note 5 : Bits 7 and 6 are not used.

Note 6 : These 2 octets contain all the field of the Packet Header including version and type bits.

Note 7 : Knapsack Key mapping

The Knapsack key mapping is given in Figure 4.3.5. Address 200 contains the least significant octet of the first Knapsack coefficient W0. Address 201 contains octet 1 of the first Knapsack coefficient W0 ....(see example below )

Note8 : Hashing Key mapping :

The Hashing key mapping is given in Figure 4.3.5. Address 368 contains the 4 LSBs of the Hashing Key stored at the right of the memory octet in the reverse order. Address 369 contains the 8 following bits in the reverse order. Caution : if the Hashing key is read bit by bit starting from the MSB, the memory must be filled from right to left.( see example below )

### 3.4.2 The CLCW interface

The PTCD sends updated CLCW to the PTME block through an APB interface.

- apbi_clcw : APB master inputs
- apbo_clcw : APB master outputs

The transfer is performed if one of the following conditions is met:

- End of the TC frame decoding in the TR block
- RFAvail signal change
- Bitlock signal change

The write is made at the address 0x0000.

### 3.4.3 The HKPF interface

The HKPF block can retrieve AU, CPDU or FAR status through an APB interface.

- apbi_hkp : APB slave inputs
- apbo_hkp : APB slave outputs

To fetch a status, the HKPF block shall make a first read access to the corresponding status register to launch the status retrieval mechanism. The status is available when the corresponding bit in the TC Ready register is high.

The HKPF block can make a second read access to the status register to retrieve the status information only when the corresponding Ready register bit is high.

The 80-bit AU status shall be completely retrieved in the following mandatory order: AU1 (32 bits), AU2 (32 bits) then AU3 (16 bits).

Refer to the RD1 for more details.

### 3.4.4 The configuration interface

The configuration of the MAP CPU (MAP ID, MAP CPU IT) can be performed through an APB interface. The MAP CPU status can be retrieved through the same APB interface.

- apbi : APB slave inputs
- apbo : APB slave outputs

### 3.4.5 The MAP CPU interrupt

The PTCD generates an MAP interrupt to warn the CPU to handle it.

- MAPCPU_IT : interrupt

The CPU shall perform the following tasks when the MAP CPU interrupt occurs:

1. MAP CPU IT register read access (optional)
2. MAP CPU BUFFER Status register read access
3. Clear of the MAP CPU interrupt
4. MAP CPU ABORT Status register read access (mandatory)

# 4 DESCRIPTION OF THE INTERNAL REGISTERS

## 4.1 REGISTERS ACCESSIBLE THROUGH THE APB CONFIGURATION INTERFACE

**Configuration Register: address 00H**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-9 | Unused | 0 | | |
| 8 | TEST3 | 0 | Test3 mode activation | r/w |
| 7 | TEST2 | 0 | Test2 mode activation | r/w |
| 6 | TEST1 | 0 | Test1 mode activation | r/w |
| 5 | TEST | 0 | General test mode activation | r/w |
| 4 | AUTSL | 0 | AU tail length selection | r/w |
| 3 | AUEXT | 0 | External AU use indication | r/w |
| 2 | AUDIS | 0 | Internal AU disable signal | r/w |
| 1 | CPDUDIV | 0 | CPDU clock dividing signal | r/w |
| 0 | PRIOR | 0 | Priority mode configuration | r/w |

**Status Register: address 04H**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-6 | Unused | 0 | | |
| 5 - 3 | SELTC | 111 | Selected channel number MTC | r |
| 5 - 3 | SELTC | 111 | Selected channel number MTC | r |
| 2 | AUSBUF | 0 | Number of the AU status buffer | r |
| 1 | FARBUF | 0 | Number of the FAR status buffer | r |
| 0 | AUBUF | 1 | Flip-flop data buffer indication signal | r |

**CLCW & CPDU Register: address 08H**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-16 | CPDUT | | CPDU status | r |
| 15-0 | CLCWT | | CLCW status | r |

**MAP CPU IT Register: address 0CH**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-1 | Unused | 0 | | |
| 0 | MAP CPU IT | 0 | Interrupt | r |

**MAP CPU IT SET Register: address 10H**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| None | SET | 0 | A write access sets the MAP CPU IT | w |

**MAP CPU IT RESET Register: address 14H**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| None | RESET | 0 | A write access resets the MAP CPU IT | w |

**MAP CPU IT MASK Register: address 18H**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-1 | Unused | 0 | | |
| 0 | MASK | 0 | '0' : MAP CPU IT not masked<br>'1' : MAP CPU IT masked | r/w |

**MAP CPU BUFFER STATUS Register: address 1CH**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-1 | Unused | 0 | | |
| 0 | MAPCPU_BUF_STS | 0 | Indicates the buffer containing the MAP data<br>'0': buffer 0<br>'1': buffer 1 | r |

**MAP CPU ABORT STATUS Register: address 20H**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-1 | Unused | 0 | | |
| 0 | MAPCPU_ABT_STS | 0 | asserted if a BD frame is received when the Segment Layer is not idle.<br>A read access releases the backend buffer. | r |

**MAP CPU ID Register: address 24H**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-15 | Unused | 0 | | |
| 14 | MAP 1 ID enable | 0 | MAP 1 serial output enable | r/w |
| 13 - 8 | MAP 1 ID | 0 | When a MAP has the MAP 1 ID, it will be output through the MAP serial link | r/w |
| 6 | MAP 0 ID enable | 0 | MAP 0 serial output enable | r/w |
| 5 - 0 | MAP 0 ID | 0 | When a MAP has the MAP 0 ID, it will be output through the MAP serial link | r/w |

## 4.2 REGISTERS ACCESSIBLE THROUGH THE APB HKPF INTERFACE

**TC READY Register: address 00H**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-5 | Unused | 0 | | |
| 4 | CPDU ready | 0 | CPDU status is ready | r |
| 3 | AU3 ready | 0 | AU3 status is ready | r |
| 2 | AU2 ready | 0 | AU2 status is ready | r |
| 1 | AU1 ready | 0 | AU1 status is ready | r |
| 0 | FAR ready | 0 | FAR status is ready | r |

**TC FAR Register: address 04H**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-0 | FAR status | | The FAR status | r |

**TC AU1 Register: address 08H**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-0 | AU1 status | | The AU1 status | r |

**TC AU2 Register: address 0CH**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-0 | AU2 status | | The AU2 status | r |

**TC AU3 Register: address 10H**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-16 | Unused | 0 | | |
| 15-0 | AU3 status | | The AU3 status | r |

**TC CPDU Register: address 14H**

| Bits | Name | Reset Value | Function | r/w |
|---|---|---|---|---|
| 31-16 | Unused | 0 | | |
| 15-0 | CPDU status | | The CPDU status | r |

# 5 FUNCTIONAL ARCHITECTURE

## 5.1 DESCRIPTION OF THE INTERNAL MEMORY DATA BUS PATH

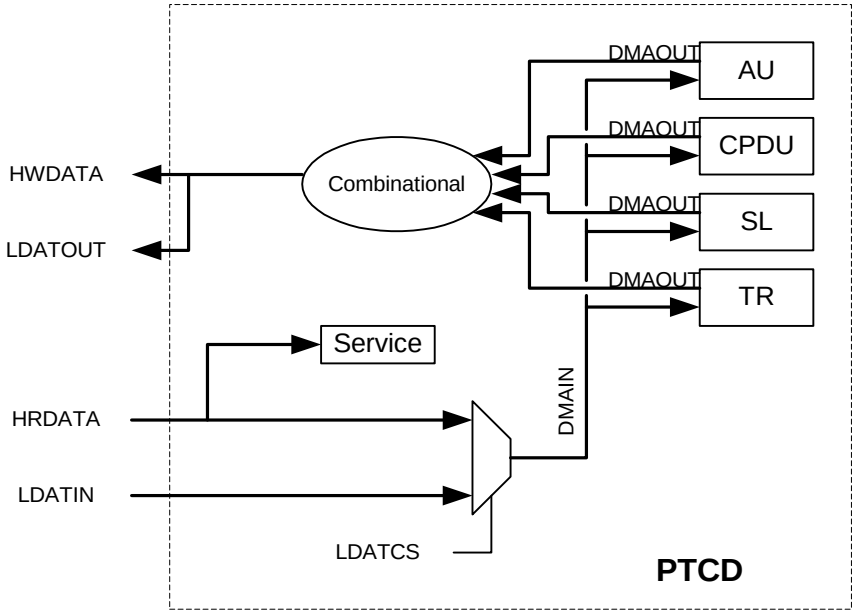


**Figure 3: Internal memory data bus**

The DMA FSM of the DMA sub-block has been modified to handle the AHB protocol.

The LDATIN and LDATOUT data buses remain.

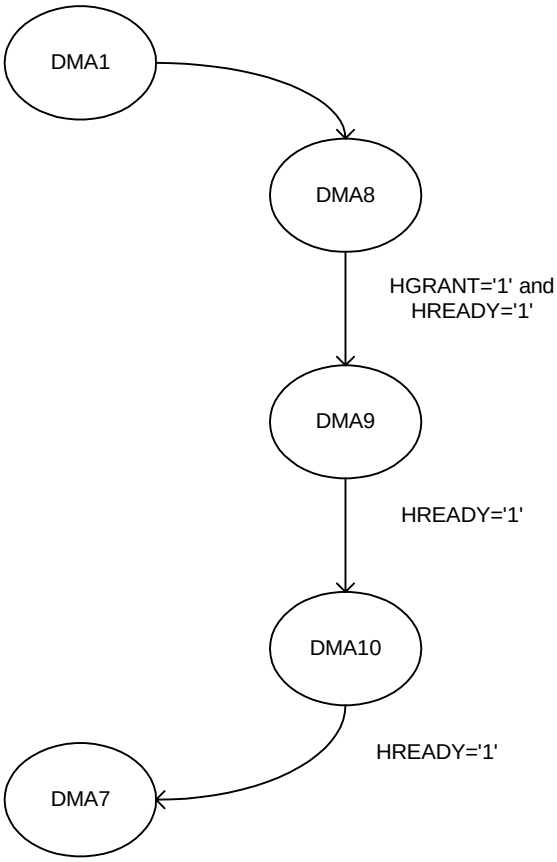


**Figure 4: Added states of the DMA FSM**

Description of the added states:

- The DMA8 state generates a bus request and waits for the bus grant signal to go to the DMA9 state.
- The DMA9 state inserts the address and the transfer type. The next state will be DMA10 when the information is taken into account (HREADY signal asserted).
- The DMA10 waits for the end of the transfer and goes to the DMA7 state. The ERROR, SPLIT, RETRY Responses are not taken into account.

### 5.2 DESCRIPTION OF THE CLCW INTERFACE

The goal is to send the updated value of CLCW to the PTME block through an APB interface. The APB protocol is ensured by the following FSM:

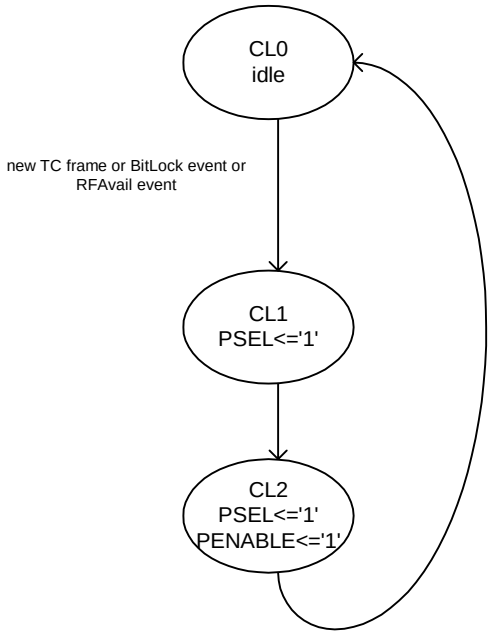


**Figure 5: APB FSM**

Description of the FSM:

- The CL0 state waits for an event of the RF_Available or BitLock signal or the end of a TC frame decoding to start an CLCW transfer.
- The CL1 state asserts the PSEL signal. The write address is 0x0000.
- The CL2 state keeps the PSEL signal high and asserts the PENABLE signal.

### 5.3 DESCRIPTION OF THE HKPF INTERFACE

The HKPF interface provides the FAR, AU and CPDU information following the protocol described in the RD1.

The protocol is ensured by the HKP FSM whose goal is to trigger the existing CPDU/FAR/AU request FSM in order to retrieve CPDU/FAR/AU information.

The HKP FSM generates CPDU/FAR/AU requests. This mechanism is in the TM sub-block.

The CPDU/FAR/AU request FSM has been modified to be sensitive to the HKP FSM.

Registers have been added to store the CPDU/FAR/AU information.

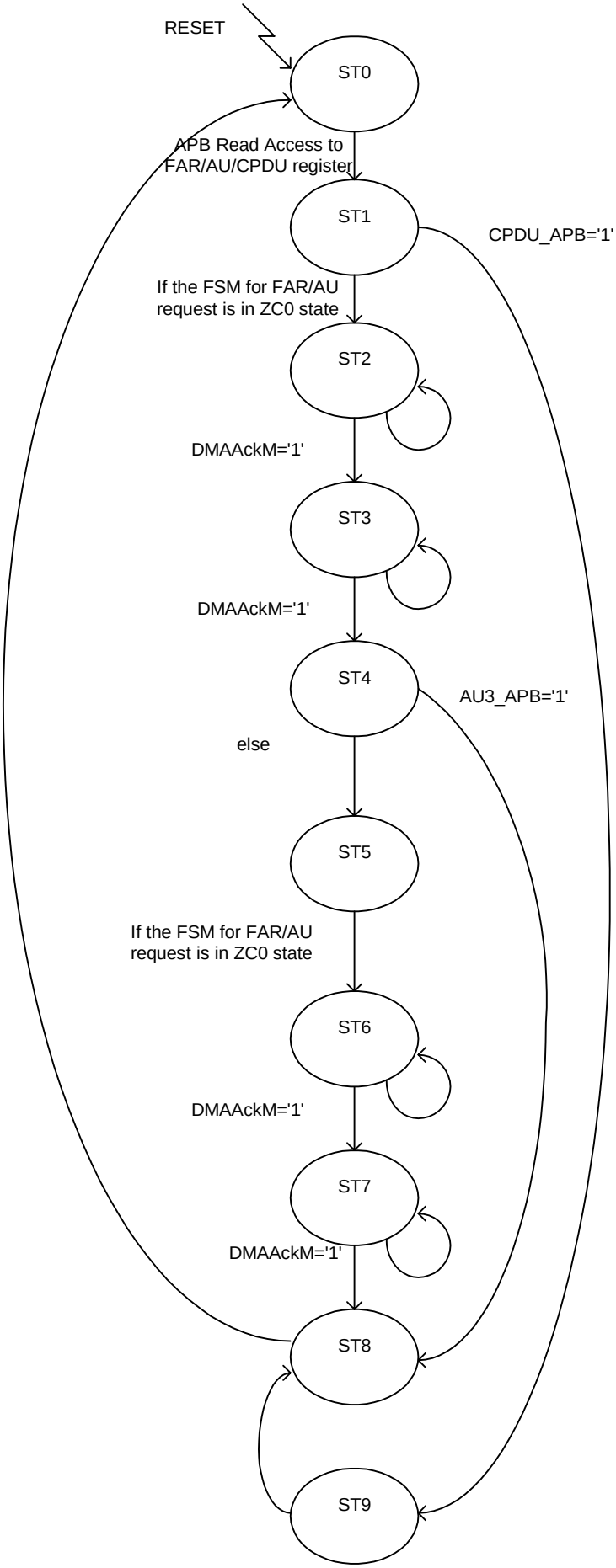
RESET
ST0
APB Read Access to
FAR/AU/CPDU register
ST1
CPDU_APB='1'
If the FSM for FAR/AU
request is in ZC0 state
ST2
DMAAckM='1'
ST3
DMAAckM='1'
ST4
AU3_APB='1'
else
ST5
If the FSM for FAR/AU
request is in ZC0 state
ST6
DMAAckM='1'
ST7
DMAAckM='1'
ST8
ST9

**Figure 6: HKP FSM**

Description of the HKP FSM:

- The ST0 state waits for an APB read access then identify the access (FAR, AU1, AU2, AU3 or CPDU). The corresponding flag is asserted (FAR_APB, AU1_APB, AU2_APB, AU3_APB or CPDU_APB). The next state will be ST1 if a read access into FAR/AU1/AU2/AU3/CPDU register is performed.
- In the ST1 state, if the CPDU_APB flag is asserted, an order is given to load the CPDU into the status buffer (TCStatus). The next state is ST9. Otherwise, an AU or FAR request is generated. The next state is ST2 if the AU/FAR request FSM is ready to receive the request from the HKP FSM.
- The ST2 state waits for a DMA acknowledge response (DMAAckM signal) to go to ST3 state. The DMAAckM is asserted when 8 bits of the status has been retrieved.
- The ST3 state waits for another DMA acknowledge response to load the 16 bits of the status into the status buffer. The next state will be ST4 when the DMAAckM is asserted.
- In the ST4 state, all the requests are clear. If the AU3_APB flag is high, the status value is completed, so the next state is ST8. Otherwise, 16 other bits of the status are needed and the next state is ST5.
- In the ST5 state an AU or FAR request is generated. The next state is ST6 if the AU/FAR request FSM is ready to receive the request from the HKP FSM.
- The ST6 state waits for a DMA acknowledge response (DMAAckM signal) to go to ST7 state. The DMAAckM is asserted when 8 bits of the status has been retrieved.
- The ST7 state waits for another DMA acknowledge response to load the 16 bits of the status into the status buffer. The next state will be ST8 when the DMAAckM is asserted.
- In the ST8 state, all the requests and flags are clear. The TC READY register is updated to signal the TC status availability. In all cases, the next state is ST0.
- The ST9 state is use to delay the CPDU status ready flag insertion. In all cases, the next state is ST8.

## 5.4 DESCRIPTION OF THE MAP CPU INTERRUPT MECHANISM

Most of the MAP are handled by the CPU.

In the SL sub-block, the segment FSM has been modified to generate the MAP CPU interrupt. The following SD16 and SD17 states have been added:

- The SD16 state sets the MAP CPU interrupt and load the current value of AUBUF
- The SD17 waits for the Abort Segment Status read access

The MAP is output through the serial link if its MAP ID matches the MAP 0 ID or the MAP 1 ID and the MAP 0/1 ID enable is active. Otherwise the SD16 state is activated for an internal MAP decoding.

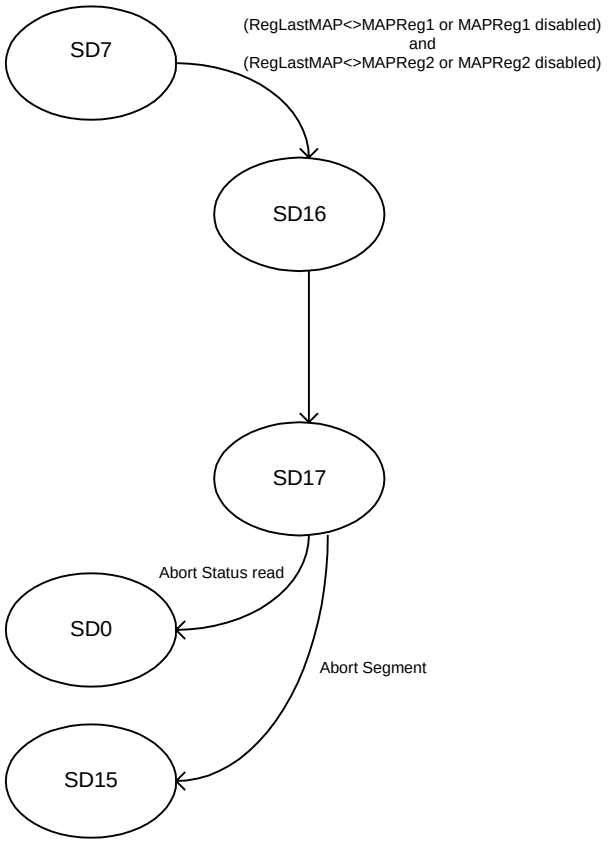


**Figure 7: Additional states**

## 5.5 BLOCK SUPPRESSION

The following blocks containing pads insertion have been suppressed in the modification for an IP core.

- B3STA3
- BINTTL
- BIOT3
- BOUT3
- INSTPAD

-----%-----%-----%-----%-----