Title

1553 BC/BM/RT VHDL CORE
DATA SHEET

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1 GENERAL

1.1 INTRODUCTION

This document specifies the working schemes and the functions to be implemented on the 1553 BC/BM/RT VHDL Core.

This IP is compatible with MIL-STD-1553B (notice 2) protocol and manages three different working modes: Bus Controller, Remote Terminal and Bus Monitor.

This IP1553 can be used to develop equipment for Space Applications.

1.2 APPLICABLE DOCUMENTS

AD1: MIL-STD-1553B Notice 2. (Department of Defence, Washington)
Digital Time Division Command/Response multiplex Data bus

AD2: STANAG 3838. (OTAN)
Accord de standardisation sur bus de données numériques du type commande/réponse à multiplexage temporel

AD3: AMBA™ Specification (Rev 2.0) Issue A © Copyright ARM Limited

1.3 REFERENCE DOCUMENTS

REF1: DTD-CCTD-ST-0044-ASTR (ASTRIUM)
MAT53CTM ASIC SPECIFICATIONS

1.4 ABBREVIATIONS

AHB:	Advanced High-performance Bus
ASIC:	Application Specific Integrated Circuit
BC:	Bus Controller
BM:	Bus Monitor
IO:	In Out
IP:	Intellectual Property
APB:	Advanced Peripheral Bus
RT:	Remote Terminal

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2 OVERVIEW

This chapter is not part of IP1553 specification. It only provides general information and brief description about the IP1553 architecture and operation.

2.1 GENERAL DESCRIPTION

The MIL-STD-1553B bus is a serial bus whose application is foreseen in several European Space Applications.

It is a multiplex data bus that operates asynchronously in a command/response mode. The transmission on the bus occurs in a half-duplex way. Every data transfer occurring on the bus is initialized and managed by the Bus Controller.

The data exchanges between the terminals connected to the bus involve 16 bits words. The data can be driven through the bus at a speed of 10^6 bits/s.

As described in Figure 1, the IP1553 provides all facilities for efficient coupling between the Application and the 1553B buses.

The IP1553 has a dual bus capability and operates as an autonomous unit in all three modes: Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (BM).

- Bus Controller mode:

  As a Bus Controller, the IP1553 can initiate all types of 1553B transfers on either the nominal or redundant bus. It has also a lot of programming facilities, such as conditional and unconditional Jumps, Subprograms management, automatic retry. This “microprocessor like” programming facilities drastically improve the IP1553 autonomy and reduce the need for the Application to take care of bus management.

- Remote Terminal mode:

  As a Remote Terminal, the IP1553 accepts all options and mode commands specified by the MIL-STD-1553B protocol. In addition, the transfer commands (including mode commands), may optionally be illegalized through dedicated Characterization words.

  In the Remote Terminal mode, the IP1553 offers a high level of autonomy. 1553B transfers is controlled by the IP1553 on a Sub Address based splitting scheme. The Application can allow multiple buffers which sizes are defined by Sub Address. The IP1553 provides a Control Word that ensures the completion and the validity of the message and an Information Word giving dating and the address where data were stored.

- Bus Monitor Mode:

  As a Bus Monitor, the IP1553 monitors the entire bus activity and gives any associated information to the Application. The IP1553 monitors each 1553B word transferred on both buses, and stores it with an associated Identification word. The Identification word provides the Application with additional information (Command/Status or Data word type, error type, dating).

  The IP1535 also features microprocessors compatibility providing a standard AMBA AHB and APB Application interface.

The IP1553 is based on the CM5 and MAT53 ASIC. It is fully compatible with MIL-STD-1553B protocol.

The next lines present the main features provided by the IP1553:

- Full MIL-STD-1553B compliance
- Bus Controller, Remote Terminal, and Bus Monitor capability
- Dual redundant bus capability
- Fully compatible with an AMBA bus interface
- Programmable non response time-out (14 µs or 31 µs)
- Loop test for transmission checking
- Illegal commands management (in RT mode)

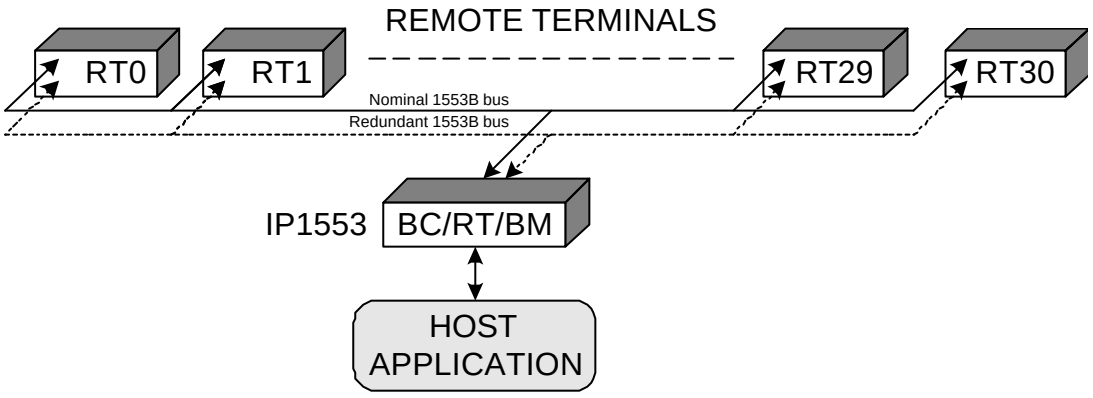

Figure 1: 1553B Bus architecture including IP1553 in BC mode

2.2 ARCHITECTURAL DESCRIPTION

2.2.1 1553B bus coupling module architecture

Figure 2 describes a typical IP1553 based on a 1553B bus coupling module. Very little additional hardware is required to ensure a full dual redundant 1553B bus coupling to an Application.

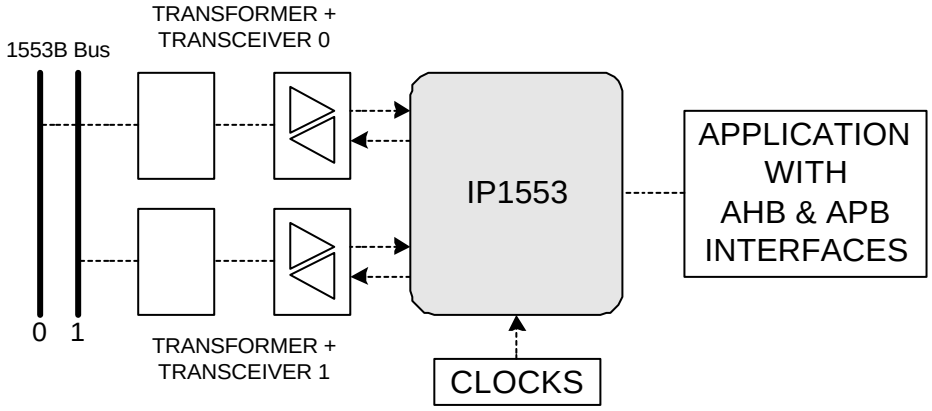

Figure 2: IP1553 environment

2.2.2 IP1553 internal architecture

The internal architecture of IP1553 is shown on Figure 3. It is composed of the five major following elements: Manchester Encoder/Decoder blocks, Internal registers, Commands management & Executing unit, Application Interface block including an AMBA AHB interface and an APB interface.

2.2.2.1 Manchester Encoder/Decoder blocks

The Encoder converts the parallel binary data to a serial Manchester encoded bit stream. The serial bit stream is then driven to the active 1553B bus transmitter. Two Encoders are included in the IP1535 chip.

The Decoder converts the 1553B serial Manchester data from one receiver to parallel binary data. Thanks to two independent Decoders the IP1553 is able to listen simultaneously on both buses.

2.2.2.2 Internal registers

These 16 bits registers (except the two General Purpose registers which are 32 bit wide) are dedicated to the BC mode. They contain necessary information for IP1553 chip's configuration or operation. The content of these registers is further detailed in this document in BC mode.

2.2.2.3 Commands management & executing unit

This block manages the 1553B protocol. Its function is defined by the Internal registers which control the way the IP1553 initiates transfers in the Bus Controller mode, responds to commands in the Remote Terminal mode, or saves messages in the Bus Monitor mode.

2.2.2.4 Application Interface block

The Application Interface provides an APB interface for configuration and status registers. It provides also an AMBA AHB interface for memory access.

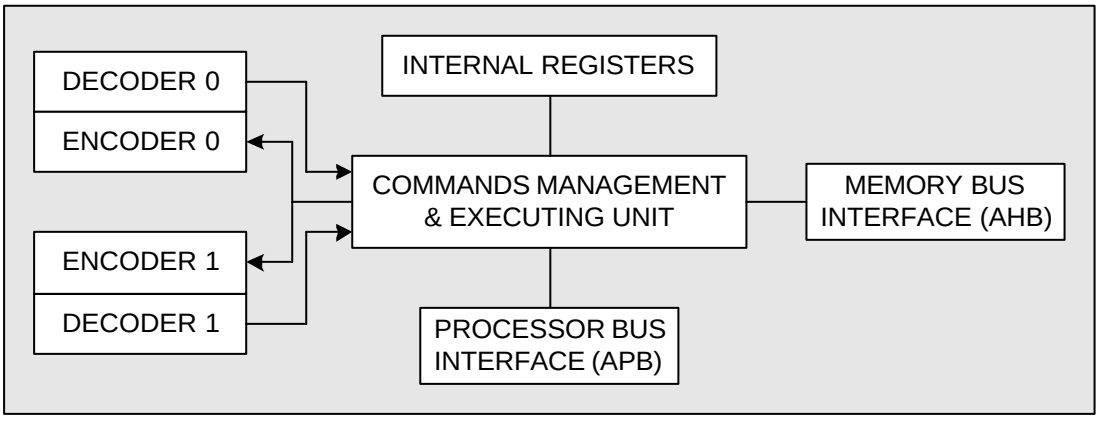

Figure 3: IP1553 internal block diagram

3 IP1553 SPECIFICATION

Following paragraphs are all parts of the IP1553 specification.

3.1 IP1553 INITIALIZATION

The IP1553 provides Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (BM) modes. All modes is exclusive and the only way to switch from one mode to another is to reset the device (by activation of RESET_N input pin or Rst1553 bit in Command and Status register, C53CDSTReg).

These modes is selected through two bits Mode in the Configuration register C53CFReg according to the following table:

MODE	RT	BC	BM	RT
Mode(1:0)	11	01	10	00

At initialization, the IP1553 enters the RT mode.

After a RESET_N activation, the IP1553 enters the initialization sequence. After a Rst1553 bit activation, the IP1553 enters the reset sequence.

During Initialization sequence, the IP1553 enter the RT mode, because all bits in registers are set to “0”

During Reset sequence, the IP1553 reads the Mode bits to enter the correct mode.

TX0	1	C53Rst	0
TX0B	1	C53Err	0
TX0Inh	1	Hwdata (31:0)	0 on the 32 bits
TX1	1	Haddr(27:0)	0 on the 28 bits
TX1B	1	Hbusreq	0
TX1Inh	1	Hwrite	0
MOD53(3:0)	0000	Hburst(2:0)	000
RSTCOM_N	1	Htrans(1:0)	00
SYNC_N	1	Hprot(3:0)	0000
Prdata(32:0)	0 on 32 LS bits, 1 on MS bit	Hlock	0
C53It	0	Hsize(2:0)	000

Note:

Pready and Prdata are not reset during Rst1553 bit activation to allow the Application to write in the C53CDSTReg to stop this bit activation in order to leave the reset sequence.

The Mode bits are read only on RESET_N or Rst1553 bit activation and memorized through the Configuration register otherwise. So to take into account any modification on these bits, activation of RESET_N signal or Rst1553 bit is required. The other inputs can be modifiable at any time.

In order to prevent any hazardous functioning of the chip, the following inputs or bits in registers must be stable out of the "Reset state": Mode, TimeOut, CdtCirBuf (in BM mode), DbcEn, BrCstEn, WdSize, LockEn, DW16En, ExtArea bits and LTEN_N, TXEN_N input pins. Any modification on these pins or bits must be followed by the activation of Rst1553 bit (C53CDSTReg).

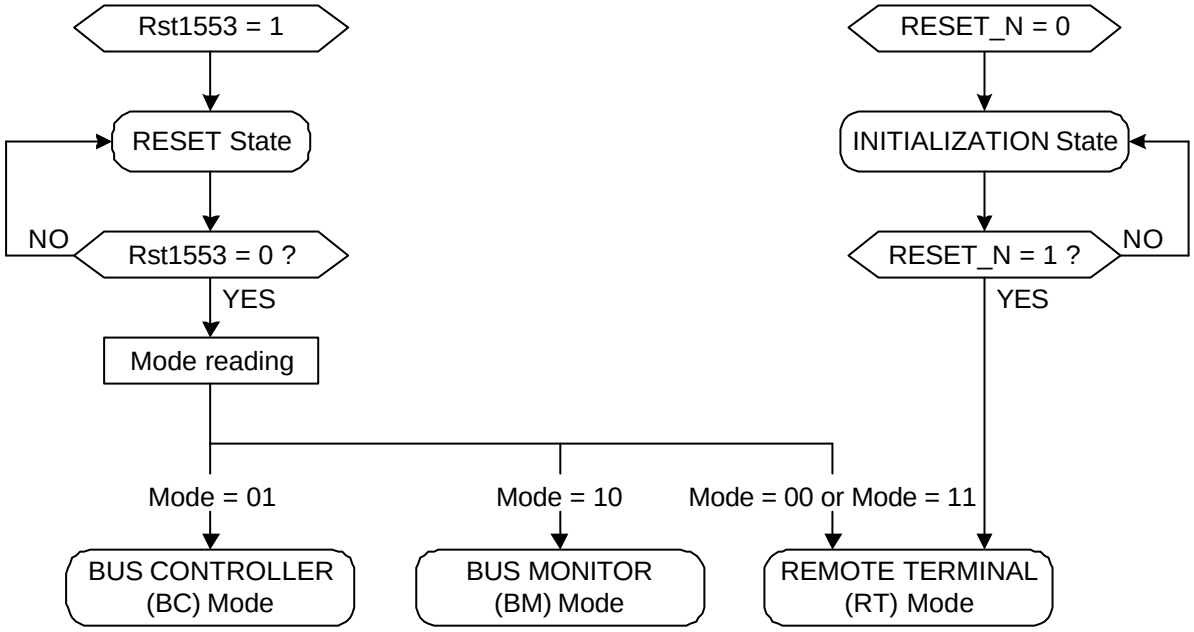

Figure 4: IP1553 initialization and reset sequence

The Reset state corresponds to a reset of the IP1553 except its Bus Processor Interface in order to allow the Application to write in its Configuration register and its Command register.

The Initialization state corresponds to a reset of the whole IP1553. Therefore, the IP1553 cannot be configured during Initialization state as its Bus Processor Interface is not active. The IP1553 leaves its Initialization state 5 µs after the rising edge of the RESET_N input pin (i.e: RESET_N value = '1')

3.2 APB INTERFACE

3.2.1 Registers description

IP1553 Command Status Register (C53CDSTReg), Address "0010":

Bits	Name	Reset Value	Function	r/w
0	Rst1553	0	1553 function reset: set to "1" to reset the 1553 part	r/w
1	GoStop	0	1553 Start Stop Command: set to "1" to activate the 1553 function	r/w
2	IntCmd	0	1553 Interrupt Command in BC mode: asserted to force the execution of a CALL instruction if INTMSK bit is set to "1"; reset by 1553 controller when the Int order has been taken into account	r/w
4-3	Unused			
5	RstSt	0	Reset State: • 0: Reset state or Initialization state • 1: Activity state given by BusyFlag	r
6	BusyFlag	0	Activity State: • 0: Stand-by state • 1: Active state	r
13-7	Unused			
14	ErrParAd	0	Set to "1" in case of RT address parity error	r
31-15	LastCmdAd	0x10FFE	Address in the 1553 memory area of the last command treated in RT mode. Before any command, the value is irrelevant so the reset value is set to a value out of the command area. (Word addressing)	r

IP1553 Extended Memory Base Address Register (C53EMBAReg), Address "0001":

Bits	Name	Reset Value	Function	r/w
25-0	ExtMemAd	0x0000000	Base Address of the extended memory area (written by 1553 link) (Word addressing)	r
31-26	Unused			

IP1553 Reception Table Index Register (C53RTIReg), Address "0111":

Bits	Name	Reset Value	Function	r/w
31-0	RTIndex	0x0000000	Reception Table Index Value	r

1553 Transmission Table Index Register (C53TTIReg), Address "1000":

Bits	Name	Reset Value	Function	r/w
31-0	TTIndex	0x0000000	Transmission Table Index value	r

IP1553 Configuration Register (C53CFReg), Address ”0000”:

Bits	Name	Reset Value	Function	r/w
1-0	Mode	0	1553 mode selection: • 00 or 11: RT mode • 01: BC mode • 10: BM mode	r/w
2	TimeOut	0	Programmable time-out selection: • 0: 14 µs time-out • 1: 31 µs time-out	r/w
3	DbcEn	0	Dynamic Bus Control Enable in RT mode: • 0: Disable • 1: Enable	r/w
4	BrCstEn	0	Broadcast mode enable in RT mode • 0: Disable • 1: Enable	r/w
5	CdtCirBuf	0	Conditional Instruction in BC mode, when EXTCND bit is set to “1 in first instruction word: • 0: JUMP/CALL is ignored • 1: JUMP/CALL is executed Circular buffer mode in BM mode: • 0: Single buffer mode • 1: Circular buffer mode	r/w
6	ExtArea	0	Extended Memory Area mode: • 0: Extended Memory Area mode inhibited • 1: Extended Memory Area mode activated	r/w
7	WdSize	0	Data Word Size: • 0: 32 bit Word Size • 1: 16 bit Word Size (if DW16En is set to 1)	r/w
12-8	ExtSubAd	0x00	Sub-address number for Extended Memory Area mode	r/w
13	ItTrokMask	0	ItTrok Mask: must be at “0” to allow C53It interrupt on end of a RT valid exchange.	r/w
14	ItSyncMask	0	ItSync Mask: must be at “0” to allow C53It interrupt on reception of synchronise order, or on end of a BC instruction bloc execution.	r/w
15	Err1553Mask	0	Err1553 Mask: must be at “0” to allow C53Err interrupt on 1553 error.	r/w
24-16	MemArea	0x00000	Memory area MSB: code the base address (19 LSB of Haddr at 0) of the 64Kwords of data memory, followed by the 64Kwords of BC instruction or RT command memory	r/w
25	LockEn	0	Memory Bus Lock Access mode Enable (Read-Modify-Write usage): • 0: Memory bus access without bus lock • 1: Control word access with bus lock in BC mode	r/w
26	CmdRstEn	0	Mode Command Reset Enable : • 0 : 1553 reset upon Reset RT command reception disabled • 1 : 1553 reset upon Reset RT command reception enabled	r/w

27	DW16En	0	16 bits Data Word Size Enable : • 0 : 16 bit Word Size disable • 1 : 16 bit Word Size enable	r/w
31-28	Unused			

IP1553 Nominal Interrupt Register (C53NITReg), Address "0011":

Bits	Name	Reset Value	Function	r/w
0	ItTrok	0	Maskable Interrupt: Set to "1" at the end of a RT valid exchange; reset upon register read access	r
1	ItSync	0	Maskable Interrupt: Set to "1" after reception of synchronise order, or at the end of a BC instruction bloc execution, if SYNC bit set in the first instruction word; reset upon register read access	r
2	ItDbc	0	Not Maskable Interrupt: Dynamic bus control Command reception: set to "1" after Dynamic bus control Mode command reception in RT mode; reset upon register read access	r
3	ItSwitch	0	Not Maskable Interrupt: Set to "1" after change of data address table for a Sub-address; reset upon register read access	r
8-4	SwitchSubAd	0x00	Last Sub-address number which activated ItSwitch	r
31-9	Unused			

IP1553 Error Interrupt Register (C53EITReg), Address "0100":

Bits	Name	Reset Value	Function	r/w
0	ErrMem	0	Not Maskable Interrupt: Set to "1" in case of DRAM access error; reset upon register read access	r
1	Err1553	0	Maskable Interrupt: Set to "1" in case of 1553 error; reset upon register read access	r
2	ErrInst	0	Not Maskable Interrupt: Set to "1" in case of BC Illegal Instruction error; reset upon register read access	r
3	CwError	0	Not Maskable Interrupt: Set to "1" when the CWERR bit is set in the control word in BC mode, reset upon register read access	r
4	ErrRTAd	0	Not Maskable Interrupt : Set to 1 in case of RT address parity error ; reset upon register read access	r
31-5	Unused			

IP1553 Reset Interrupt Register (C53RITReg), Address "0101":

Bits	Name	Reset Value	Function	r/w
0	RstCom	0	Not maskable Interrupt: Set to "1" after reception of a valid "Reset Remote Terminal"; reset upon register read access	r
31-1	Unused			

IP1553 Program Counter Register (C53PCReg), Address "0110":

Bits	Name	Reset Value	Function	r/w
15-0	ProgCnt	0x0000	Program Counter for instruction execution in BC. Current instruction/operand address	r
31-16	Unused			

The Application configures the IP1553 thanks to these registers. The Application does it after the Initialization state ends.

Then, if the Mode required is different from “00”, the Application modifies it and uses the Rst1553 bit to force the IP1553 to take into account the new mode. When the Application set the Rst1553 bit to “0”, the IP1553 leaves its reset state. The Application can then set the GoStop bit to “1”.

Upon Reset_N input activation the IP1553 enters Initialization state and reset its nine registers. Upon Rst1553 bit activation the IP1553 enters Reset state and reset the bits that are in read mode in the C53CDSTReg, C53RTIReg, C53TTIReg and the C53PCReg.

3.2.2 Signals description

Name	I/O	Function
Paddr(3:0)	I	Bits (5 down to 2) of APB address bus
Psel	I	APB select: this signal indicates that the IP1553 is selected and a data transfer is required.
Penable	I	APB strobe: this signal is used to indicate the second cycle of an APB transfer
Pwrite	I	APB transfer direction: when high this signal indicates an APB write access and when low a read access
Pwdata(32:0)	I	APB read data bus, the MSB is an odd parity bit
Prdata(32:0)	O	APB write data bus, the MSB is an odd parity bit

Note: All the outputs are set to “0” when the IP1553 is in initialization state

3.3 AHB INTERFACE

3.3.1 Function

The IP1553 is an AHB master. It is able to connect with an AHB bus thanks to its AHB interface. Some functions are not implemented such as SPLIT and RETRY management.

The IP1553 does not manage the transfer size information. It always indicates 32 bits on Hsize signal (i.e: Hsize = “010”).

The IP1553 does not manage the protection control. The value of Hprot signal is “do not care”.

The IP1553 is able to use the locked transfers if LockEn bit is set to “1” in the C53CFReg, to ensure its Read-Modify-Write function in BC mode.

The IP1553 makes 32 bit access. The IP1553 uses 32 bits or only 16 bits. When the IP1553 uses 16 bits, it is the MSB of the 32 bit word. When the IP1553 access the Application, the latter responds within 6 µs.

3.3.2 Signals description

Name	I/O	Function
Hrdata(31:0)	I	AHB read data bus
Hgrant	I	AHB bus grant: this signal indicates that the IP1553 is currently the highest priority master. The IP1553 gets access to the bus when both Hready and Hgrant are high
Hready	I	AHB transfer done: when high this signal indicates that the slave is available
Hresp(1:0)	I	AHB transfer response: this signal provides additional information on the status of a transfer: OKAY and ERROR. The RETRY and SPLIT response are not managed
Haddr(27:0)	O	AHB address bus (1)
Htrans(1:0)	O	AHB transfer type: this signal indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY. The BUSY is not used
Hwrite	O	AHB transfer direction: when high this signal indicates a write transfer to the slave and when low a read transfer from the slave
Hsize(2:0)	O	AHB transfer size: this signal indicates the size of the transfer (2)
Hburst(2:0)	O	AHB burst type: this signal indicates if the transfer forms part of a burst. Only SINGLE and INCR mode are managed. For INCR burst the length is 2 words. Early burst interruption are not checked (i.e. Hgrant will not be checked after the first transfer started)
Hprot(3:0)	O	AHB protection control (3)
Hwdata(31:0)	O	AHB write data bus
Hbusreq	O	AHB bus request: this signal indicates that the IP1553 requires the bus
Hlock	O	AHB locked transfers: when high this signal indicates that the IP1553 requires locked access to the bus and no other master should be granted the bus until this signal is low

Notes:

(1) Haddr(1:0) is always "00" as the IP1553 manages only word addressing

(2) Hsize(2:0) value is "010" except during reset.

(3) Hprot(3:0) value is "do not care" (i.e. "0000")

All the outputs are set to "0" when the IP1553 is in reset state.

3.4 BUS CONTROLLER (BC) MODE DEFINITION

3.4.1 BC mode working scheme

In Bus Controller mode, the IP1553 follows the basic sequence described hereafter (Figure 5):

- Wait for a high level on GoStop bit,
- Then load the Program Pointer register with the data contained at the base location in Program memory: “MemArea+10000H”,
- Then activate C53Err interrupt in case of memory access error (Time-out or Hresp input = Error), and return to “Stand-by state” waiting new activation of the GoStop bit,
- Read & Execute the first instruction block (memory address is defined by the content of the Program Pointer register and the MemArea bits),
- Then activate C53Err interrupt (in case of ErrMem, CwError or ErrInst activation), and return to “Stand-by state” waiting new activation of GoStop bit,
- Or activate C53Err interrupt if Err1553 activation with EXCHANGE instruction and no additional retry, then return to “Stand-by state” if EXCMSK = 1 otherwise continue in sequence,
- Or return to “Stand-by state” if GoStop bit is deactivated (low level) or if CHB bit is set to “0” in the Instruction block,
- Or activate C53It interrupt (in case of ItSync activation) if SYNC bit is set to “1” in the Instruction block, and continue sequence,
- Otherwise stay in “Active state” with Reading & Execution of the next Instruction block after loading of the Program Pointer register with the Interrupt address in case of Interrupt reception (see description § 3.4.3.6),

In addition, the BusyFlag bit (in the Status register) are forced to high level by the IP1553 to indicate that it is in the “Active state”, otherwise BusyFlag bit is low leveled.

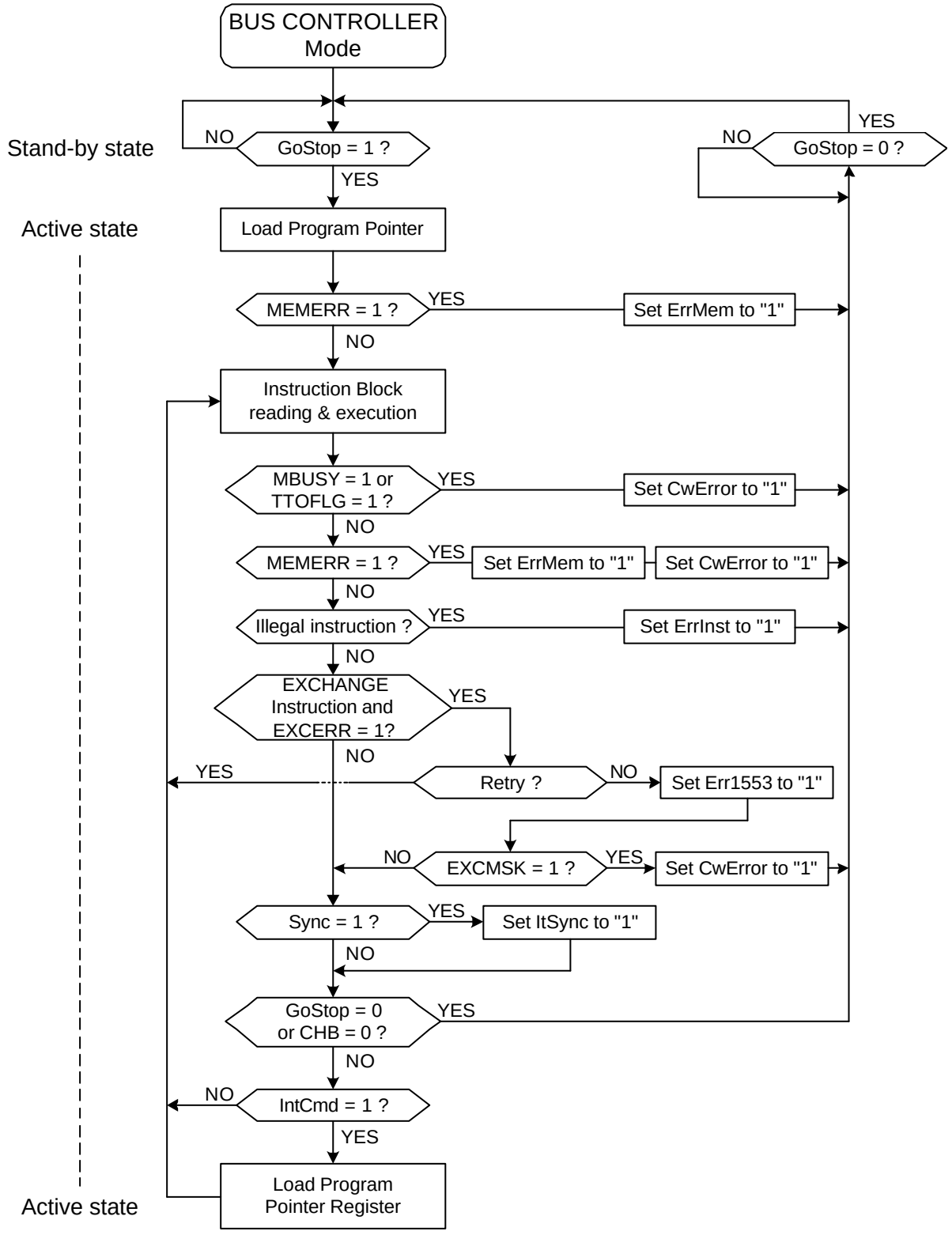

Figure 5: BC mode working scheme

3.4.2 BC mode internal registers definition

In BC mode, the IP1553 provides 16 internal registers accessible in read and/or write mode by the Application using WRITE or READ instructions as follows:

DESCRIPTION	ADDRESS (REG3:0)	BITS NB	ACCESS TYPE	INIT VALUE
PROGRAM POINTER REGISTER	0	16	R/W(1)	0000
DATA POINTER REGISTER	1	16	R/W(1)	0000
CONTROL WORD POINTER REGISTER	2	16	R/W(1)	0000
CONTROL WORD REGISTER	3	16	R(2)	0000
STATUS MASK REGISTER	4	16	R/W	0000
ERROR MASK REGISTER	5	16	R/W	0000
TIMER	6	16	R/W	0000
GENERAL PURPOSE REGISTER	7	16 (32)	R/W	0000
STACK POINTER REGISTER	8	16	R/W(1)	0005
INSTRUCTION WORD REGISTER	9	16	R/W(1)	0000
WORD COUNT REGISTER	10	16	R/W(1)	0000
COMMAND WORD 1 REGISTER	11	16	R/W(1)	0000
COMMAND WORD 2 REGISTER	12	16	R/W(1)	0000
DATA BUFFER ADDRESS REGISTER	13	16	R/W(1)	0000
INTERNAL STATE REGISTER	14	5	R/W	0000
GENERAL PURPOSE REGISTER	15	16 (32)	R/W	0000

(1) These registers are reserved for the IP1553 internal operations. So any access to these registers using WRITE instruction may provoke hazardous behaviour of the IP1553.

(2)) This register cannot be modified by a WRITE instruction.

These registers are reset only by RESET_N signal or Rst1553 bit activation. All these registers are 32 bits wide but only the 16 MSB are used, except for the two general purpose registers. A READ to these registers overwrites a 32 bits word in memory and only the 16 MSB of a word in memory is taken into account during a WRITE instruction (except for the two general purpose registers).

3.4.2.1 Program Pointer register

This register contains the address in Program memory of the next instruction to be executed. This register is automatically initialized with the data contained at location “MemArea+10000H” in memory upon activation of GoStop bit. This register is automatically written in the Context Block in memory when the IP1553 returns to “Stand-By state” or after the activation of ItSync bit, CwError bit or Err1553 bit

3.4.2.2 Data pointer register

This register contains the word address of the last access in the data area of the memory.

3.4.2.3 Control word Pointer register

This register contains the address of the last Control word stored in memory. This register is directly controlled by instruction block execution (see § 3.4.10) This register is automatically written in the Context Block in memory when the IP1553 returns to "Stand-by state" or after activation of ItSync bit, CwError bit or Err1553 bit.

3.4.2.4 Control word register

The function of the bits composing the Control word is as described hereafter:

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
CWERR	MEMERR	TTOFLG	MBUSY	EXCERR	LP	NR1	NR2	AD1	AD2	HIWRD	LOWRD	WWRD	STW1	STW2	DBLFLG

Figure 6: Control word structure

CWERR	Control word error = MEMERR + TTOFLG + MBUSY + EXCERR.EXCMSK (see note 4)
MEMERR	Memory access error = Time-out + (Hresp input = Error)
TTOFLG	Transmission time-out activation on selected bus
MBUSY	Data buffer not available (DBLFLG = 1)
EXCERR	Execution error (see note 1)
LP	Loop test failure indicator
NR1	No response from RT1 (see note 2)
NR2	No response from RT2 (see note 2)
AD1	Address error in RT1 Status word (see note 2)
AD2	Address error in RT2 Status word (see note 2)
HIWRD	Number of words received higher than expected
LOWRD	Number of words received lower than expected
WWRD	Wrong word received: parity, synchronization or Manchester error
STW1	Bit set and non masked in RT1 Status word (see notes 2&3)
STW2	Bit set and non masked in RT2 Status word (see notes 2&3)
DBLFLG	Data buffer locked by the IP1553 or the Application

Notes:

1) EXCERR = "Control word register" AND "Error mask register" (see definitions § 3.4.2.6)
2) For RT to RT transfers, "RT2" refers to the RT addressed by the "Transmit Command" and "RT1" refers to the RT addressed by the "Receive Command". For non RT to RT transfers, only "RT1" is used, and the bits related to RT2 is forced to "0"
3) STW = "RT Status word" AND "Status mask register" (see definitions § 3.4.2.5)
4) Except during EXCHANGE instructions execution, EXCMSK is forced to "0"

All these bits are active high, which means that they are set to "1" in case of error. For DBLFLG description, refers to § 3.4.8.3.

The Control word register contains information generated by the IP1553 related to the last instruction block execution. This register is updated after each instruction block execution (bits BIT0 to BIT10 are updated only after each EXCHANGE instruction execution).

The Control word register is loaded after each EXCHANGE instruction execution in memory at location specified by the "Control word address" of the instruction block. This register is automatically written in the Context Block in memory when the IP1553 returns to "Stand-by state" or after activation of ItSync bit, CwError bit or Err1553 bit.

3.4.2.5 Status mask register

This register is used to individually mask bits BIT0 to BIT10 of each incoming "Remote Terminal Status word" to build STW1 and STW2 flags (bits BIT1 and BIT2) of the Control word. Bits BIT11 to BIT15 of this register (corresponding to RT address) are not used, so are to "0".

3.4.2.6 Error mask register

This register is used to individually mask bits BIT1 to BIT10 of the Control word to build EXCERR flag (bit BIT11) of the Control word. Only bits BIT1 to BIT10 of this register are used, the others are set to "0". Any modification of this register produces recalculating of EXCERR flag in the Control word.

3.4.2.7 Timer

This register allows to generate time intervals internally to the IP1553. This timer is under Application control according to WRITE and READ instructions (see description § 3.4.10). A WRITE instruction addressing the timer initializes it and automatically starts the count down. When the timer reaches zero, it stops and stay to zero.

After activation, the timer counts down even if the IP1553 returns to "Stand-by state".

The resolution of this timer is 2 µs. During count down, the timer can be read and the value of the counter will not be modified but it can delay the end of count down if the exchange duration is longer than 1 µs. The timer is frozen to allow a proper reading of its value.

3.4.2.8 Stack Pointer register

This register is used to store current Stack pointer (see description § 3.4.4)

3.4.2.9 Instruction word register

This register is used to store the current Instruction word.

3.4.2.10 Word Count register

This register is used to store the word count during a 1553 transfer.

3.4.2.11 Command word 1&2 registers

These registers is used to store the first and second (for RT to RT transfer) command word(s) of each 1553 transfer. For RT to RT transfers, the Command word 1 register stores the Receive command, the Command word 2 stores the Transmit command.

3.4.2.12 Data buffer address register

This register is used to store the address of the data buffer attached to each 1553 transfer in the data area of the memory. This register is directly controlled by instruction block execution (see § 3.4.10) This register is automatically written in the Context Block in memory when the IP1553 returns to "Stand-by state" or after activation of ItSync bit, CwError bit or Err1553 bit.

3.4.2.13 Internal state register

This register is used to store the state information of the IP1553. The upper bits (BIT15 to BIT5) will not be used. The bits (BIT4 to BIT1) are reserved for the IP1553. These bits will not be affected by a WRITE instruction. The lower bit (BIT0) contains the Interrupt mask (INTMSK flag). It is used to mask/unmask IntCmd bit of the Command and Status register (see description § 3.4.3.6)

3.4.2.14 General Purpose registers

These two registers are not used by the IP1553 and be reserved for the Application.

3.4.3 BC mode special functions

3.4.3.1 GoStop bit (C53CDSTReg):

It is possible to control the IP1553 activity with this bit.: A low to high transition or a high level allows the IP1553 to start/continue its instruction block processing, otherwise it stays/returns to "Stand-by state" (after completion of current instruction block processing).

When the input HALT is set to "1" the IP1553 behaves as if GoStop bit is set to "0". Otherwise the IP1553 follows the value of the bit GoStop.

3.4.3.2 Chain bit (CHB bit)

A dedicated bit in each instruction block (first word) allows stopping the Program Instruction chain. The IP1553 stops after completion of the processing of the instruction containing an inactive CHB bit (CHB = "0"), then program continuation is put under Application control. Otherwise it continues in sequence with the next Instruction block …

3.4.3.3 Conditional or Unconditional Instruction

The JUMP/CALL instruction execution (described hereafter) is conditional or unconditional according to EXTCND and ERRCND bits contained in the first word of the instruction block, CdtCirBuf bit (C53CFReg) and EXCERR flag contained in the Control word.

EXTCND	ERRCND	CDTCIRBUF	EXCERR	IP1553 OPERATION
0	0	X	X	JUMP or CALL is executed
1	0	0	X	continue with next Instruction
1	0	1	X	JUMP or CALL is executed
0	1	X	0	continue with next Instruction
0	1	X	1	JUMP or CALL is executed
1	1	0	0	continue with next Instruction
1	1	1	X	JUMP or CALL is executed
1	1	X	1	JUMP or CALL is executed

Note: X means “do not care”

3.4.3.4 Automatic retry for 1553 exchange

Programming REP bit in the instruction block (first word) allows automatic retry of last exchange in case of execution error (EXCERR flag set in the Control word).

If after one retry, the exchange did not succeed, the IP1553 stores in the Context Block in memory the Program Pointer register, the Data Buffer address register, the Control word Pointer register and the Control word register. Then it generates C53Err interrupt.

In addition if EXCERR flag is not masked by the EXCMSK bit of the instruction block, the IP1553 stops execution and return to “Stand-by state”.

3.4.3.5 Memory access error

When the IP1553 encounters a Memory access error (Time-out access, Hresp input = Error), it sets MEMERR and CWERR flags in the Control word.

In that case, the IP1553 stores in the Context Block in memory the Program Pointer register, the Data Buffer address register, the Control word Pointer register and the Control word register. During these accesses, the IP1553 does not take into account any other memory access error. Then it generates C53Err interrupt, stop execution and return to “Stand-by state”.

3.4.3.6 IntCmd bit (C53CDSTReg) & INTMSK bit

It is possible to interrupt a program execution with IntCmd bit: a low to high transition on this bit with INTMSK set to "1" in the Internal state register (see description § 3.4.2.13) forces the IP1553 to execute a CALL instruction.

The CALL instruction is executed only at the end of the current instruction treatment except for a WAIT instruction. In that case, the treatment is immediately aborted and the WAIT instruction will be lost. The CALL address is given by the data contained at location "MemArea+00004H" in memory. Execution of the CALL instruction is indicated by the IP1553 by resetting the IntCmd bit and setting to "0" the INTMSK bit of the Internal state register.

A RETURN instruction is programmed at the end of the "interrupt subroutine" to force the IP1553 to return to the main program. In addition, setting INTE bit in any RETURN instructions forces the IP1553 to set to "1" the INTMSK bit, then enable the IP1553 to take into account any other interrupt.

The INTMSK bit of the Internal state register is also be set or reset by a WRITE instruction. The IntCmd bit has no effect in "Stand-by state".

3.4.4 Stack management

The IP1553 uses a Stack to store the "return address" at the beginning of each subroutine execution, and retrieve the "return address" at the end of each subroutine execution. The Stack is located in the data area of the memory. It is addressed using the Stack Pointer register located inside the IP1553 (see Figure 7).

This register is also initialized by a WRITE instruction.

The Stack is fully managed by the IP1553: write and read access to the Stack and update of the Stack Pointer register.The Stack has no size limit (except the size of the data area) and can be placed anywhere in the data area of the memory. The same Stack is used for the CALL instructions and for the Interrupts.

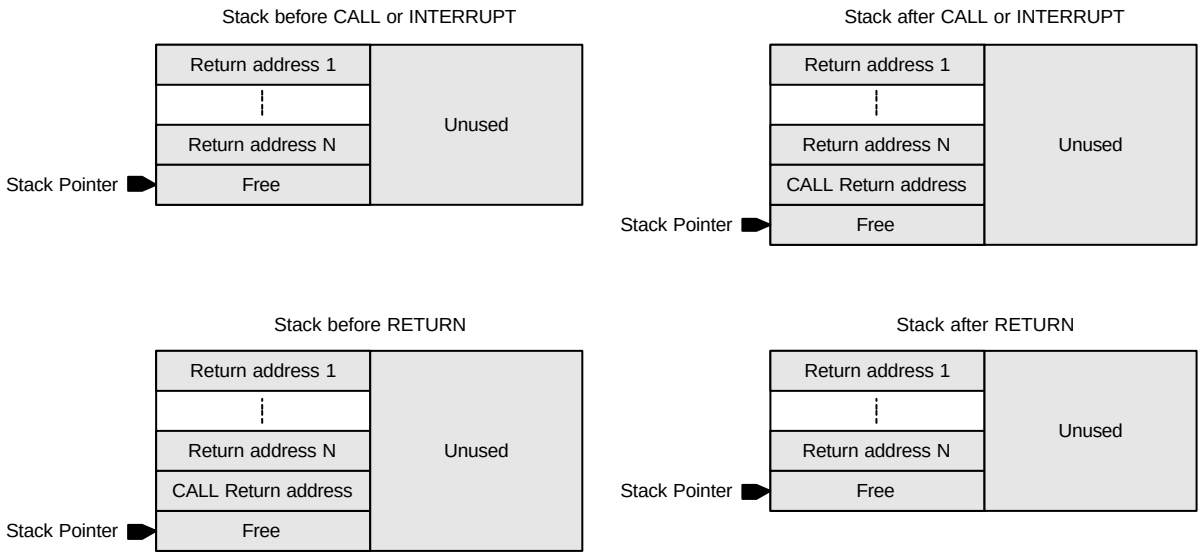

Figure 7: Stack management

3.4.5 No response time-out management

The IP1553 is able to handle programmable no-response time-out. The time-out value is taken into account to detect a no-response from a Remote Terminal.

The TimeOut bit (C53CFReg) determines the chosen value for no-response time-out. The smallest value is 14 µs (TimeOut = "0"), and the highest value is 31 µs (TimeOut = "1").

3.4.6 Redundancy management

Each EXCHANGE instruction specifies the bus (nominal or redundant) on which the corresponding transfer has to be initiated.

This is done with a dedicated bit ("BUSID") inside the first instruction word of instruction block as follows: bus 0 used if BUSID = "0", bus 1 used otherwise.

3.4.7 Test support & Error report

3.4.7.1 Control word

This 16 bit word is the error register of the IP1553. Its content indicates the errors that have occurred during the last 1553B bus transfer (see definition § 3.4.2.4).

The Control word is stored in the Control word register within the IP1553 and in memory at the location given by the instruction word.

3.4.7.2 Loop test

Each word transmitted within a given message is looped back through the active receiver channel for wrap-around test. The loop test is made at the level of the transceiver/transformer connection.

This function is enabled when LTEN_N input pin is low level.

If a mismatch occurs between the stored and the looped word, the IP1553 sets to "1" the LP bit of the Control word. In addition, the IP1553 stores in the Context Block in memory the Program Pointer register, the Data Buffer address register, the Control word Pointer register and the Control word register. Then it generates C53Err interrupt, stop execution and return to "Stand-by state". Furthermore, the transmission is aborted on the 1553B bus.

3.4.8 Memory management

The IP1553 manages the two following memory areas (see Figure 8):

- The data area (used to store or to fetch transfer data): “MemArea+00000H” to “MemArea+0FFFFH”,
- The program area (containing the 1553B transfer instructions): “MemArea+10000H” to “MemArea+1FFFFH”.

The IP1553 is able to address up to 64 Kwords (32 bits) of program area.

The IP1553 is able to address up to 64 Kwords (32 bits) of data area.

MemArea defines an area for the IP1553 of 128Kwords. This area can be placed in memory at each multiple of 128K word address in the whole memory, i.e. when MemArea is increased by 1 the IP1553 area will be moved of 128 K word address.

3.4.8.1 Program area

The IP1553 uses the Program Pointer register to address the program area.

The IP1553 fetches its instructions at the location defined by the Program Pointer register.

The Instructions are organized in instruction blocks. Each instruction block contains up to 3 instruction words (see description § 3.4.10.1).

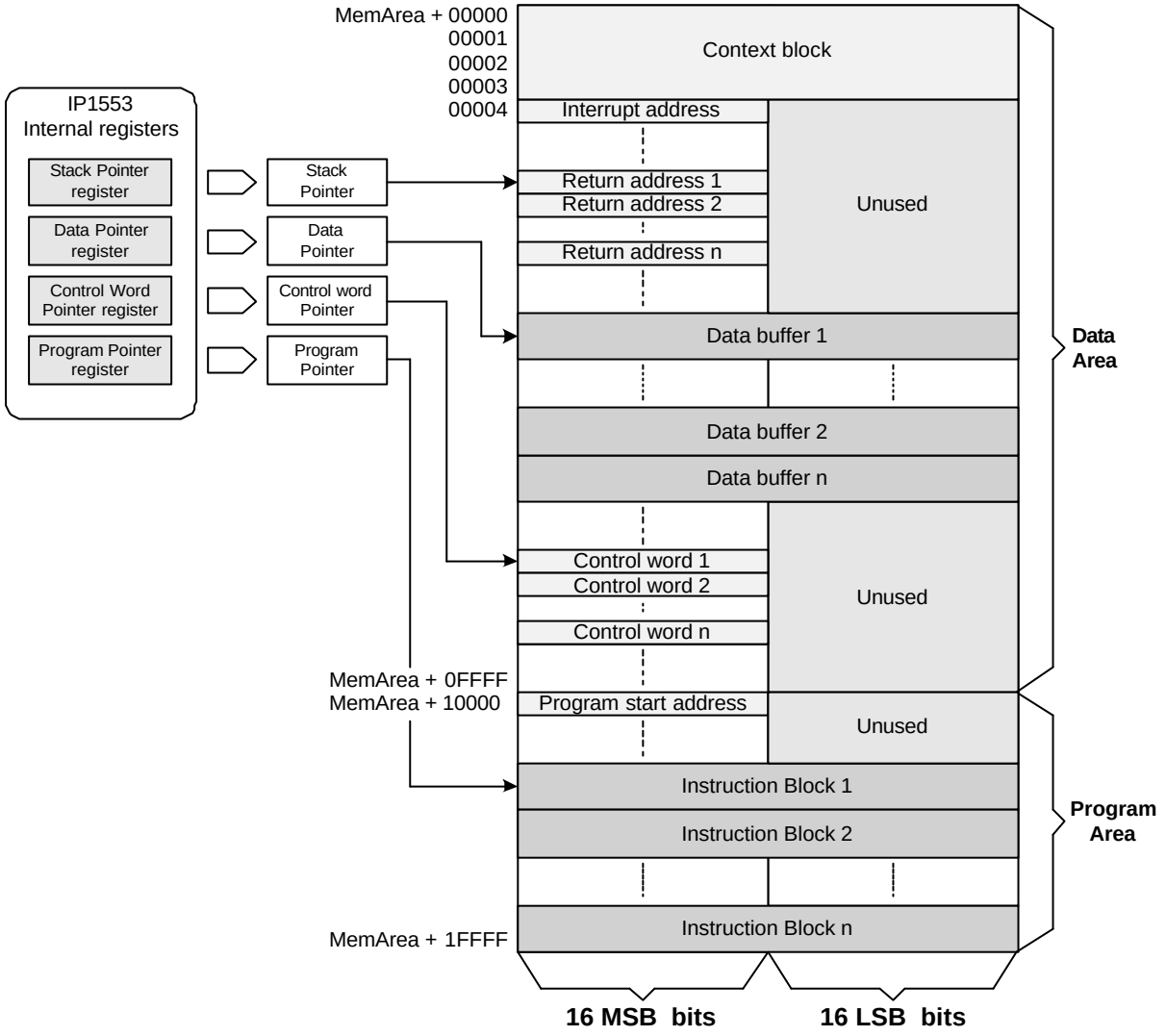

Figure 8: Memory mapping and addressing

Note:

MemArea + 00000	Program address	Unused
00001	Data buffer address	
00002	Control word address	
00003	Control word	

Figure 9: Context block structure when 16 bit Word mode

MemArea + 00000	Program address	Data buffer address
00001	Control word address	Control word
00002	Unused	
00003		

Figure 10: Context block structure when 32 bit Word mode

The address given on the Figure 8 are words address (i.e Haddr(1:0) = “00”)

3.4.8.2 Data area

The IP1553 uses the Stack Pointer register, the Data Pointer register and the Control word Pointer register to address the data area (see Figure 8)

Only one Data buffer is used for a given transfer. The Data buffer location is defined by the "Data buffer address" of the instruction block. The Data buffer is used to store the received data words (for a RT to BC transfer or a RT to RT transfer) and status word (for both RT to BC and BC to RT transfers) and to fetch the transmitted data words (for a BC to RT transfer) as shown in Figure 11 and Figure 12. The Figure 11 represents the mapping of the status and data words when the 32 bit Word mode is activated, otherwise the mapping follows the Figure 12.

The Control word is read-modify-write in the data area at the beginning and at the end of each Data buffer access. In case of retry, the Control word corresponds to the last exchange.

The Control word location is defined by the "Control word address" of the instruction block.

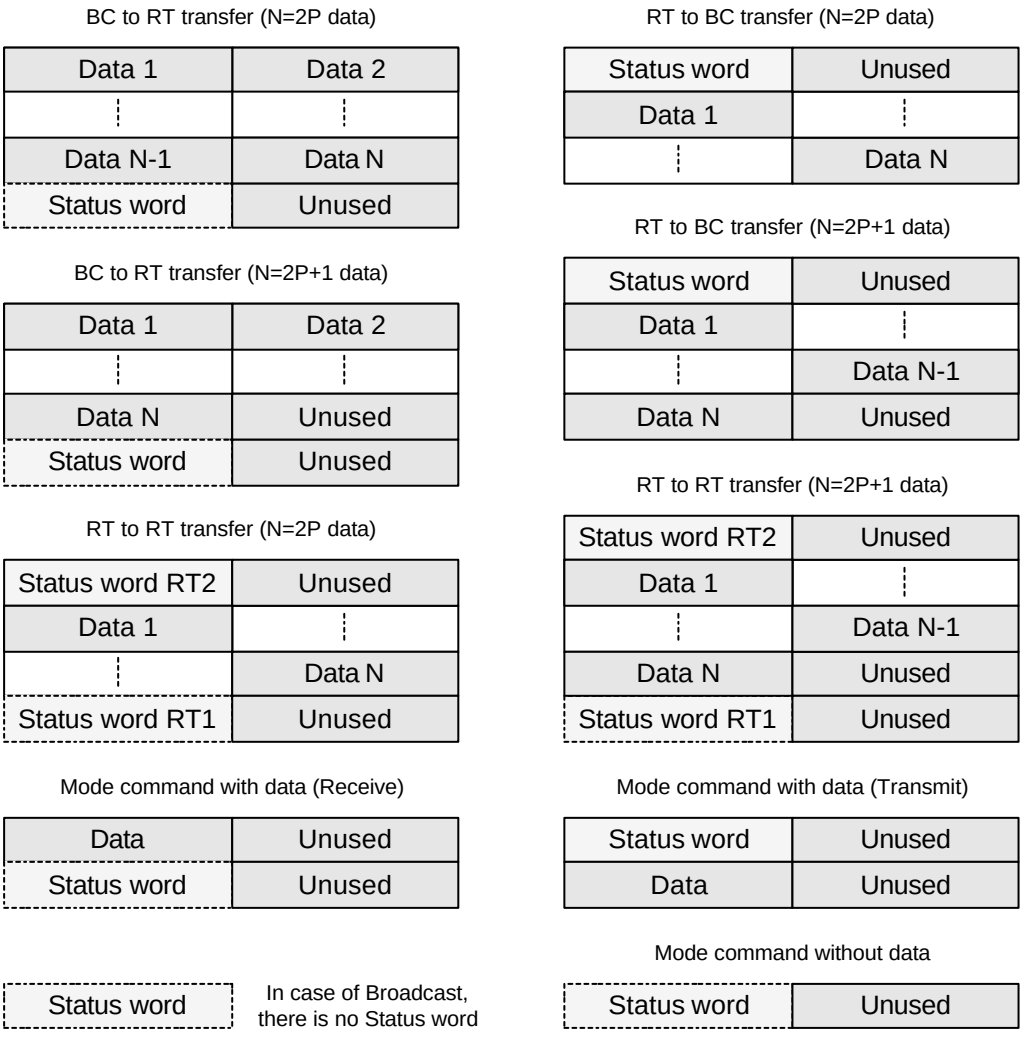

Figure 11: Data buffer format if 32 bit Word mode

Note: For RT to RT transfers, RT1 is the receiver, RT2 is the transmitter.

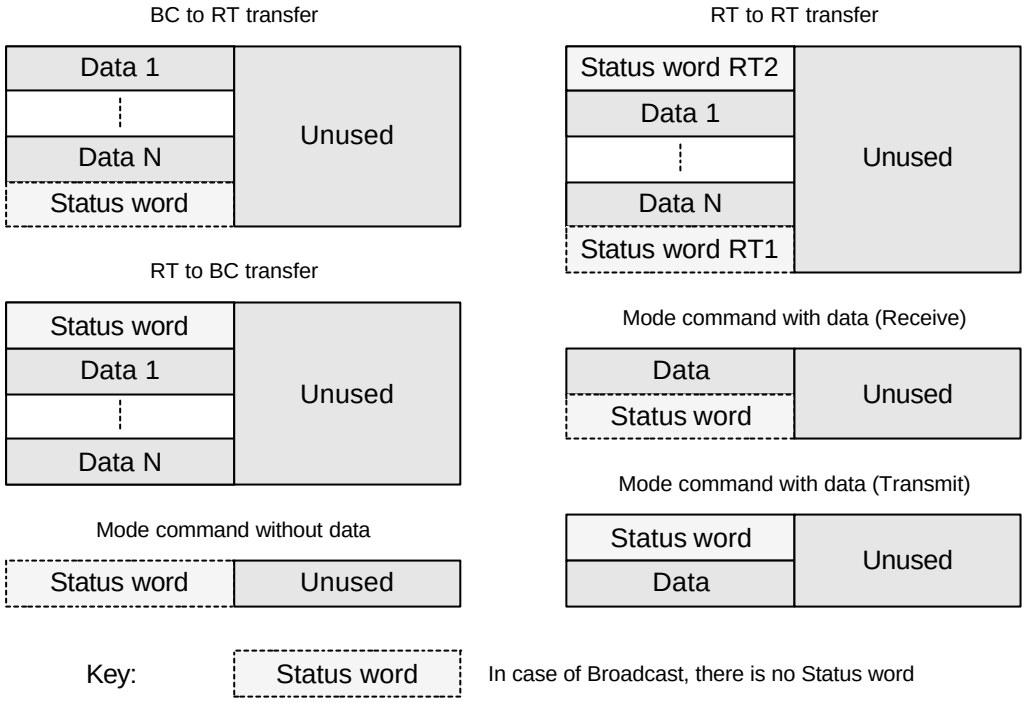

Figure 12: Data buffer format if 16 bit Word mode

3.4.8.3 Contention management

As the BC accesses the Data buffer associated with the current transfer, it follows the sequence defined hereafter (see Figure 13):

- Read the Control word in the data area, then analyze the DBLFLG bit,
- If this bit is set to “1”, it considers the situation as an error case, then it sets MBUSY and CWERR bits to “1” in the control word,
- If this bit is set to “0” it sets DBLFLG bit to “1” in the Control word (to lock the corresponding Data buffer), then store or fetch the relevant Data words, and finally set DBLFLG to “0” in the Control word (to unlock the Data buffer),
- Then it follows the instruction block execution.

The Control word reading-testing-writing operations are performed without releasing the Application bus (if LockEn bit (C53CFReg) is set to “1”), to forbid any modification of the Control word by the Application during these operations. Otherwise, if LockEn bit is set to “0”, the contention management is ineffective and the Application takes care to its use of the Data buffers.

This operation uses the Hlock output to prevent another master to use the AHB bus, when enabled with the LockEn bit in the C53CFReg.

Note: The reading-testing-writing constraint is also applicable to the Application.

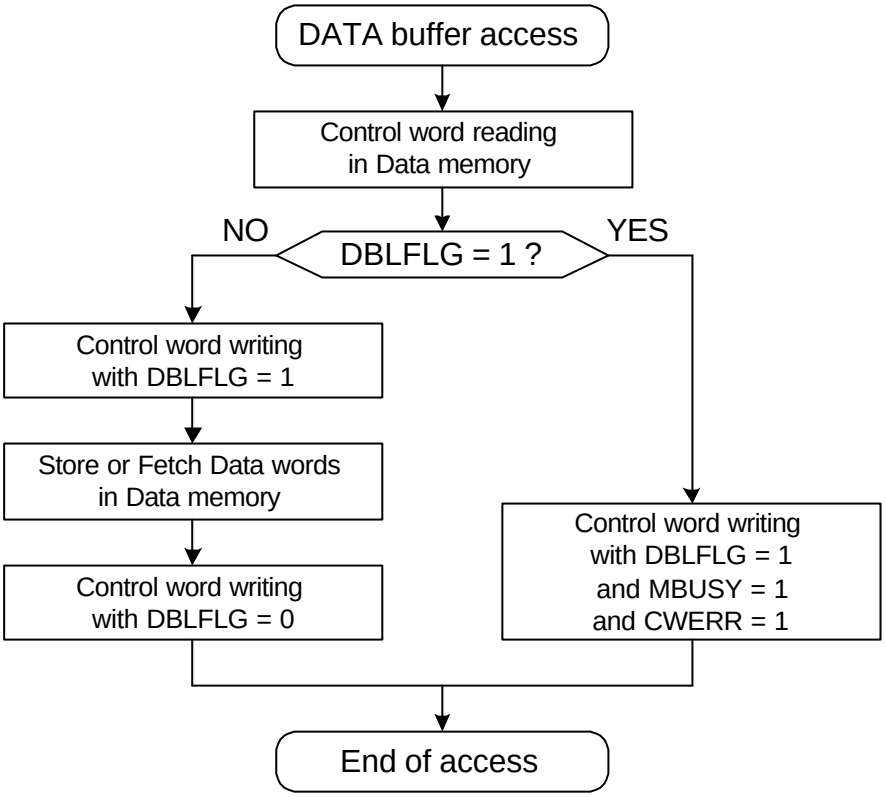

Figure 13: Memory contention management

3.4.9 Programming Facilities

The IP1553 provides the following programming facilities:

3.4.9.1 Subroutine facility

This facility is provided with CALL/RETURN instructions as defined in § 3.4.10.

The CALL instruction is Conditional (under CdtCirBuf bit (C53CFReg) control or EXCERR flag control) or Unconditional. The next instruction address is stored in the Stack in data area.

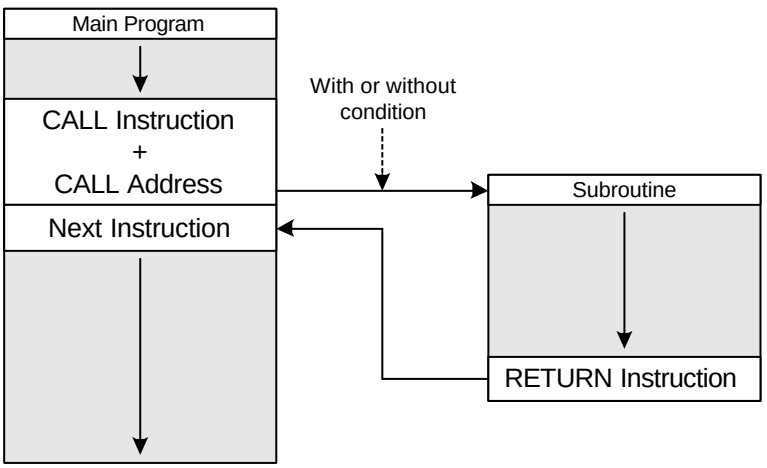

Figure 14: CALL instruction scheme

3.4.9.2 Frame shift facility

This facility is provided with JUMP instruction as defined in § 3.4.10.

The JUMP instruction is Conditional (under CdtCirBuf bit (C53CFReg) control or EXCERR flag control) or Unconditional.

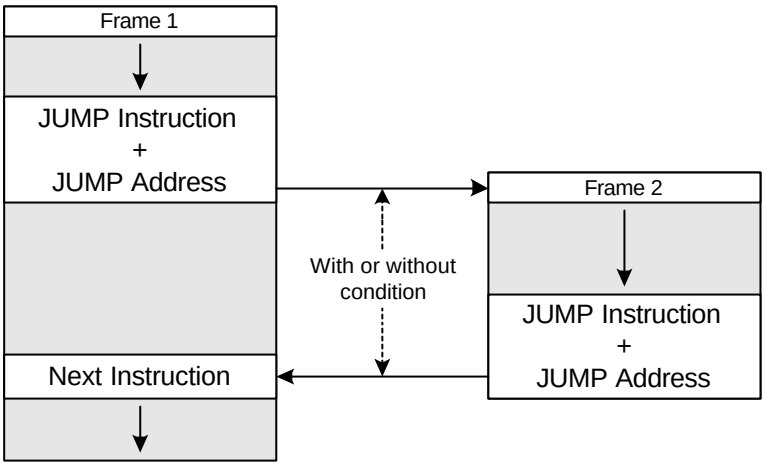

Figure 15: JUMP instruction scheme

3.4.10 Programming Instructions

3.4.10.1 Instruction block format

In BC mode, the IP1553 operates according to instructions blocks contained in the program area.

Each instruction block consists in one to five instruction words (16 bits). Furthermore, the length of each instruction block is variable (up to five words).

The first instruction word contains an Operation Code (OPCODE) in its first 4 most significant bits which defines the instruction block type as follows:

INSTRUCTION	OPCODE(3:0)	DESCRIPTION
WRITE	0000	Provide internal registers loading facilities
READ	0010	Provide internal registers reading facilities
CALL	0100	Provide subroutine facilities to the programmer
JUMP	0110	Provide shift facilities to the programmer
RETURN	1000	Provide subroutine facilities to the programmer
WAIT	1010	Allow to synchronize the transfers on 1553B bus
RT EXCHANGE	1100	Define all BC to RT, or RT to BC transfers
RT to RT EXCHANGE	1110	Define all RT to RT transfers
NOP	0001	No operation

When OpCode(0) is "1", the instruction is considered as a NOP instruction except if the ILLEGAL bit is set (see § 3.4.10.2).

The Instruction block format is as follows when 32 bit Word mode:

INSTRUCTION	**WORD1 (B31-16/B15-0)**		**WORD2 (B31-16/B15-0)**		**WORD3 (B31-16/B15-0)**	
WRITE/READ	Type	Memory @	-	-	-	
CALL/JUMP	Type	Memory @	-	-	-	
RT EXCHANGE	Type	Command word	Control word @	Data buffer @	-	
RETURN/WAIT	Type	1000H	-	-	-	
RT to RT EXCHANGE	Type	Receive Command	Transmit Command	Control word @	Data buffer @	1000H
NOP	Type	1000H				

If 16 bit Word mode, the instruction block format becomes as follows:

INSTRUCTION	**WORD1**	**WORD2**	**WORD3**	**WORD4**	**WORD5**
WRITE/READ	Type	Memory @	-	-	-
CALL/JUMP	Type	Memory @	-	-	-
RETURN/WAIT	Type	-	-	-	-
RT EXCHANGE	Type	Command word	Control word @	Data buffer @	-
RT to RT EXCHANGE	Type	Receive Command	Transmit Command	Control word @	Data buffer @
NOP	Type	-	-	-	-

Notes:

1) For WRITE/READ instructions, "Memory address" refers to program or data areas.
For CALL/JUMP instructions, "Memory address" refers to Program memory.
For EXCHANGE instructions, "Control word address" and "Data buffer address" refers to data area.
2) The "Memory address" is "do not care" for CALL/JUMP instructions referring to internal register. In that case, the address is defined by the content of the internal register selected by REG(3:0)
3) For RT EXCHANGE concerning Broadcast Mode command without data, the "Data buffer address" is "do not care".

3.4.10.2 Instruction type description

The Instruction bit name related to different Instruction types are as described hereafter:

DATA BUS	BIT NAME				
	NOP	**WRITE/READ**	**CALL/JUMP**	**RETURN/WAIT**	**RT (to RT) EXCHANGE**
BIT15 (MSB)	OPCODE3				
BIT14	OPCODE2				
BIT13	OPCODE1				
BIT12	OPCODE0				
BIT11	Unused				
BIT10	Unused				
BIT9	ILLEGAL				
BIT8	Unused	CHB			
BIT7	Unused	SYNC			
BIT6	Unused	Unused	EXTCND	RTC(1)	BUSID
BIT5	Unused	Unused	ERRCND	TIM/EXT(2)	EXCMSK
BIT4	Unused	PROG/DATA	REG/PGM	INTE(3)	REP
BIT3	Unused	REG3	REG3	Unused	Unused
BIT2	Unused	REG2	REG2	Unused	Unused
BIT1	Unused	REG1	REG1	Unused	Unused
BIT0 (LSB)	Unused	REG0	REG0	Unused	Unused

(1) Used only for a WAIT instruction

(2) Used only for a WAIT instruction and its meaning depends on the value of the bit RTC

(3) Used only for a RETURN instruction

The definition of the Instruction bits is as described hereafter:

OPCODE(3:0) Operation Code bits

ILLEGAL Illegal Instruction

"0" indicates that the word is a valid instruction

"1" indicates that the word is not a valid instruction

CHB Chain bit:

"0": no more instruction block to execute

"1": indicates that an instruction block follows this one

SYNC Interrupt at the end of instruction block execution:
- "0": interrupt disabled
- "1": interrupt enabled

PROG/DATA Program/Data memory:
- "0": Write/Read operation is performed in program area
- "1": Write/Read operation is performed in data area

REG(3:0) Address of the IP1553 internal register (see § 3.4.2)

EXTCND JUMP/CALL on CdtCirBuf bit (see § 3.4.3.3):
- "0": Unconditional
- "1" JUMP/CALL takes into account CdtCirBuf bit

ERRCND JUMP/CALL on error (see § 3.4.3.3):
- "0": Unconditional
- "1": JUMP/CALL takes into account EXCERR flag

REG/PGM Register or Program JUMP/CALL address:
- "0": JUMP/CALL address is defined by the content of the IP1553 internal register selected by REG(3:0)
- "1" JUMP/CALL address is defined by the "Memory address"

RTC&TIM/EXT:
- "00": internal delay (time is given by the internal timer)
- "01": external delay (time is given by DELIN_N input)
- "11": external delay (time is defined by Cycle input)
- "10": external delay (time is defined by Slot input)

INTE Interrupt enable:
- "0": no effect
- "1" set INTMASK to "1" and enables interrupt (IntCmd bit)

BUSID 1553B Bus identifier:
- "0" Bus 0
- "1" Bus 1

EXCMSK Execution error mask:
- "0" EXCERR flag masked (the BC does not stop on EXCERR)
- "1" EXCERR flag not masked (the BC stops on EXCERR)

REP Repetition on execution error (if EXCERR positioned)
- "0" no repetition
- "1" repetition enabled once

Note:

- The internal timer allows a programmable delay from 2 µs to 2^{17} µs with 2 µs step.
- When internal delay is chosen, the IP1553 waits that Timer reaches 0 to continue in sequence with the next instruction block
- When external delay is chosen, the IP1553 waits DELIN_N low level or Slot/Cycle high level to continue in sequence with the next instruction block.

3.5 REMOTE TERMINAL (RT) MODE DEFINITION

3.5.1 RT mode working scheme

The Remote Terminal sequence is as shown on Figure 16.

During “Initialization state” the IP1553 initializes its registers. During this period the IP1553 does not respond to any request from the 1553B bus. The RstSt bit (C53CDSTReg) is set to “1” by the IP1553 to indicate that it is in “Initialization state”, otherwise this bit is set to “0”.

The IP1553 enters its “Stand-by state” after the end of the initialization. If GoStop bit (C53CDSTReg) is set to “1”, the IP1553 enters its “Active state”. The BusyFlag bit (C53CDSTReg) indicates when it is set to “1” that the IP1553 is in “Active state”.

Upon receipt of a valid command, the IP1553 performs an RT address parity control. In case of mismatch between hard-wired parity and computed parity, the IP1553 does not process the command and set the ErrParAd bit in C53CDSTReg and generate C53Err interrupt through activation of the ErrRTAd bit in C53EITReg.

Upon receipt of “Reset remote terminal” Mode command, the IP1553 generates the C53Rst interrupt through activation of RstCom bit and generate a pulse on RstCom_N output.

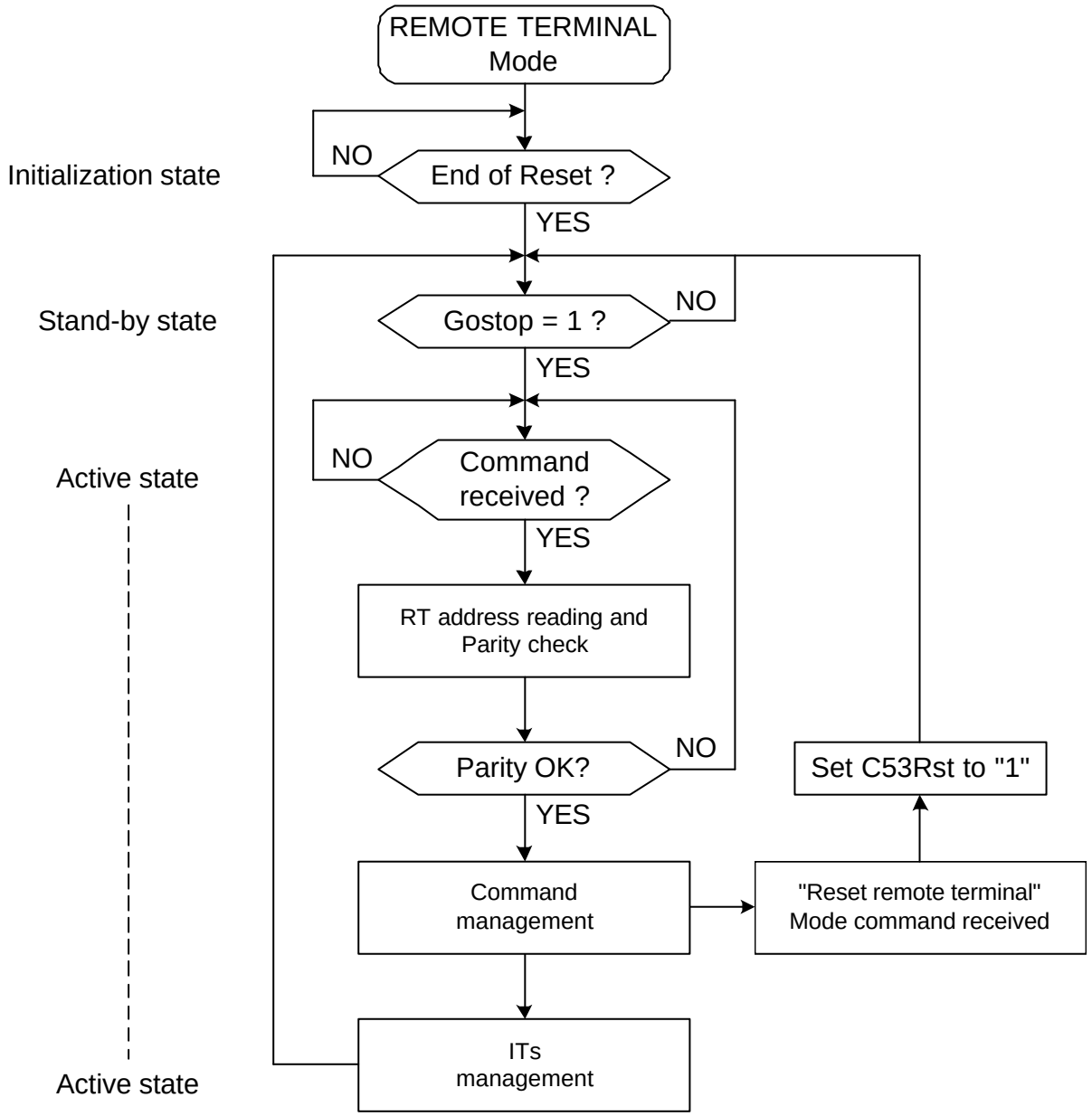

Figure 16: RT mode working scheme

3.5.2 RT mode internal registers definition

In the Remote Terminal mode, the following registers are used: the Status word register, the Last Command register and the BIT register.

3.5.2.1 Status word register

This register contains the last Status word sent in response to Bus Controller interrogation.

The Status word register is as described hereafter:

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
RTAD(4:0)					ME	NULL	SREQ	NULL	NULL	NULL	BRX	BUSY	SSF	DBC	TF

Figure 17: Status word structure

RTAD(4:0)	Remote Terminal address
ME	Message Error
SREQ	Service Request bit
BRX	Broadcast Command received
BUSY	Busy bit
SSF	Subsystem Flag bit
DBC	Dynamic Bus Control acceptance
TF	Terminal Flag Bit = TTOFLG + MEMERR + BUSYAP
NULL	Unused

During Transmit BIT word TF bit is forced to “0”. When TF bit is high, the bits B10 to B1 are irrelevant.

The bit BUSY is always set to “0” as none busy case can occur in the IP1553. It is possible for the Application to update SSF and SREQ bits of the Status word thanks to the Characterization word contained in memory. The Application is also updated the DBC bit of the Status word thanks to the DbcEn bit of the Configuration register (C53CFReg), see § 3.5.3.6 and § 3.5.4.2.

At initialization, the register is reset at 0000 (H) except Remote Terminal address.

3.5.2.2 Command word register

This register contains the last valid received command word addressing the RT. At initialization, the register is reset at 0000 (H)

The Command word register is as described hereafter:

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
RTAD(4:0)					T/R	SA(4:0)					WC(4:0)				

Figure 18: Command word structure

RTAD(4:0)	Remote Terminal address
T/R	Transmit/Receive
SA(4:0)	Sub-address/Mode
CWC(4:0)	Data word count/Mode code

3.5.2.3 Built-In-Test (BIT) word register

This register informs the Bus controller about possible 1553B transfer errors.

The BIT word register is as described hereafter:

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
NULL	MEMERR	TTO0	TTO1	TFINH	NULL	NULL	NULL	NULL	HIWRD	LOWRD	UNDCMD	T/R_ILL	LP	BUSYAP	TTOFLG

Figure 19: BIT word structure

MEMERR	Hresp input = Error
TTO0	Transmission time-out activation on bus 0
TTO1	Transmission time-out activation on bus 1
TFINH	Inhibition of Terminal Flag bit
HIWRD	Number of words received higher than expected
LOWRD	Number of words received lower than expected
UNDCMD	Undefined Command received
T/R_ILL	Bit T/R illegal in the Mode command received
LP	Loop test failure indicator
BUSYAP	Time-out access
TTOFLG	Transmission time-out activation on active bus
NULL	Unused

At initialization, the register is reset at 0000 (H).

Note:

- For transmission time-out description refer to § 3.5.7.3.
- Undefined Command bit is always set to “0” as Undefined commands are treated as illegal commands (see § 3.5.4.1)

3.5.2.4 Internal registers management

The internal registers is updated for each valid command addressing the RT (except for some Mode commands) in the following way:

TYPE OF THE COMMAND	COMMAND Register	STATUS Register	BIT Register
Mode command: “Transmit Last Command”	Not modified	Not modified	Not modified
Mode command: “Transmit Status word”	Updated	Not modified	Not modified
Mode command: “Transmit BIT word”	Updated	Updated	Not modified
Other valid commands addressing the RT	Updated	Updated	Updated
Invalid commands or commands addressing another RT	Not modified	Not modified	Not modified

3.5.3 RT mode special functions

3.5.3.1 GoStop bit (C53CDSTReg)

It is possible to control the IP1553 activity with this bit: a low to high transition or a high level allows the IP1553 to start/continue its Command processing, otherwise it stays/returns to "Stand-by state" (after the completion of the current Command processing).

When the input HALT is set to "1" the IP1553 behaves as if GoStop bit is set to "0". Otherwise the IP1553 follows the value of the bit GoStop.

3.5.3.2 RstSt bit (C53CDSTReg)

This signal is set to "0" by the IP1553 when it is in "Initialization state", otherwise it is set to "1" during "Active state". So it follows the activation of RESET_N input pin, 1553Rst bit or C53Rst interrupt.

3.5.3.3 Application interface management

The IP1553 is able to interface with an AMBA AHB bus.

3.5.3.4 BrCstEn bit (C53CFReg)

It is possible to control the authorization of Broadcast commands with BrCstEn bit.

If BrCstEn = "1" then Broadcast commands is allowed, otherwise Broadcast commands is rejected (is equivalent to commands with a different RT address).

3.5.3.5 Memory access error

When the IP1553 encounters a Memory access error, it sets MEMERR flag to "1" in the BIT word if Hresp input = Error during the access, or set BUSYAP bit to "1" in the BIT word if a Time-out has occurred during the access.

If the error occurs before transmission of the Status word, the IP1553 sends its Status word with ME bit set to "1" then stop the Command processing. Otherwise, it completes the emission of the current word then stop the Command processing. In all cases, the IP1553 generates the C53Err interrupt.

3.5.3.6 SSF and SREQ bits

During the Command processing, the IP1553 reads a Characterization word that contains information about SSF and SREQ bits. If these bits are set to "1" in the Characterization word, the IP1553 sets them to "1" in the Status word, otherwise the IP1553 sets them to "0".

3.5.3.7 RTAD(4:0) and RTParity input pins

The RTAD(4:0) define the Remote Terminal address according to the following table:

Address	RTAD(4)	RTAD(3)	RTAD(2)	RTAD(1)	RTAD(0)
0	0	0	0	0	0
1	0	0	0	0	1
…					
31	1	1	1	1	1

Note: Address 31 is reserved for broadcast messages (refer to AD1)

The RTParity input pin allows the detection of a possible address parity error. This input is wired in order to obtain an odd parity on the Remote Terminal address as stated hereafter:

RTParity = 1 Å **RTAD(4)** Å **RTAD(3)** Å **RTAD(2)** Å **RTAD(1)** Å **RTAD(0)**

The RTParity input value is checked for each valid command received. If the value reflects a parity error, the IP1553 does nottreat the command and sets ErrParAd bit to “1” in C53CDSTReg and generate C53Err interrupt through activation of ErrRTAd bit in C53EITREg.

3.5.4 Commands management

3.5.4.1 Commands legalization/illegalization

The IP1553 is able to legalize/illegalize any incoming command (including Mode commands, except “Transmit Last Command”, “Transmit Status” and “Transmit BIT”), using Characterization words included into the Characterization area of the memory. One Characterization word is linked to each command (the format is as defined § 3.5.8.4).

The IP1553 accesses to the Characterization memory at the beginning of each command processing to check the legality of the command (except for “Transmit Last Command”, “Transmit Status” and “Transmit BIT” Mode commands which are always legal).

To declare legal an incoming command the following condition is fulfilled:

- LEG bit of the Characterization word is set to “1”

For any illegal command the IP1553 sends back its Status word with ME bit set to “1”.

All unused commands is illegalized in the Characterization memory.

3.5.4.2 Mode commands management

The IP1553 behaviour is as described hereafter for the following Mode commands:

- Dynamic bus control:

The IP1553 is able to accept or not the control of the 1553B bus.

Application authorizes its acceptance by setting to “1” a dedicated bit DbcEn (C53CFReg).

Upon receipt of this command, if legalized and if DbcEn bit is high level, the IP1553 sends its Status word with DBC bit set to “1” and generate the C53It interrupt through the activation of the ItDbc bit (C53NITReg).

Otherwise it sends only its Status word with DBC bit set to “0” and also ME bit set to “1” if the command is illegalized.

The RT to BC mode switching will be effective only after modification of Mode bits (C53CFReg) and RESET_N or Rst1553 activation.

- Synchronize without data word:

Upon receipt of this command, if legalized, the IP1553 generates the interrupt C53It through the activation of the ItSync bit (C53NITReg) and a pulse on SYNC_N output pin (low level) and send its Status word. Otherwise it sends only its Status word with ME bit set to “1”.

- Synchronize with data word:

Upon receipt of this command, if legalized, the IP1553 stores the “Synchronization word” into the Buffer associated to Receive Mode commands, generate the interrupt C53It through the activation of the ItSync bit (C53NITReg) and a pulse on SYNC_N output pin (low level)) and send its Status word. Otherwise it sends only its Status word with ME bit set to “1”.

- Transmit status word:

Upon receipt of this command, if legalized, the IP1553 sends the content of the “Status word” register.

- Initiate self test:

Upon receipt of this command, if legalized, the IP1553 sends its Status word. Otherwise it sends only its Status word with ME bit set to “1”.

- Transmit BIT word:

Upon receipt of this command, if legalized, the IP1553 sends its Status word followed by the content of the “BIT word” register. Otherwise it sends only its Status word with ME bit set to “1”.

- Transmitter shutdown:

Upon receipt of this command, if legalized, the IP1553 inhibits the opposite bus transceiver by forcing to high level the corresponding pins (TX0, TX0B, TX0INHB or TX1, TX1B, TX1INHB). Otherwise it sends only its Status word with ME bit set to “1”.

- Override transmitter shutdown:

Upon receipt of this command, if legalized, the IP1553 cancels the inhibition of the opposite bus transceiver. Otherwise it sends only its Status word with ME bit set to “1”.

- Inhibit terminal flag:

Upon receipt of this command, if legalized, the IP1553 forces to “0” the TF bit of the Status word and send its Status word. Otherwise it sends only its Status word with ME bit set to “1”.

- Override inhibit terminal flag:

Upon receipt of this command, if legalized, the IP1553 cancels the inhibition of the TF bit of the Status word send its Status word. Otherwise it sends only its Status word with ME bit set to “1”.

- Reset remote terminal:

Upon receipt of this command, if legalized, the IP1553 sends its Status word and generate the C53Rst interrupt (C53RITReg) and a pulse on the RSTCOM_N output pin. Otherwise it sends only its Status word with ME bit set to “1”. It also enters Reset state if CmdRstEn bit is set in the C53CFReg.

- Transmit vector word:

Upon receipt of this command, if legalized, the IP1553 sends its Status word, read the Vector word from the Buffer associated to Transmit Mode commands send it. Otherwise it sends only its Status word with ME bit set to “1”.

- Transmit last command word:

Upon receipt of this command, the IP1553 sends its Status word followed by the content of “Command word” register.

- Selected transmitter shutdown:

Upon receipt of this command, if legalized, the IP1553 stores the “data word” into the Buffer associated to Receive Mode commands and send its Status word. Otherwise it sends only its Status word with ME bit set to “1”.

- Override selected transmitter shutdown:

Upon receipt of this command, if legalized, the IP1553 stores the “data word” into the Buffer associated to Receive Mode commands and send its Status word. Otherwise it sends only its Status word with ME bit set to “1”.

- Reserved Mode commands:

These Mode commands should be illegalized into the Characterization words. Then upon receipt of these commands, the IP1553 would only send its Status word with ME bit set to “1”.

The mode codes available is taken from the following table:

Transmit-receive bit	Mode code	Function	Associated data word	Broadcast command allowed	Command implemented
1	00000	Dynamic Bus Control	No	No	Yes
1	00001	Synchronize	No	Yes	Yes
1	00010	Transmit Status Word	No	No	Yes
1	00011	Initiate self-test	No	Yes	No(1)
1	00100	Transmitter shutdown	No	Yes	Yes
1	00101	Override transmitter shutdown	No	Yes	Yes
1	00110	Inhibit terminal flag bit	No	Yes	Yes
1	00111	Override inhibit terminal flag bit	No	Yes	Yes
1	01000	Reset remote terminal	No	Yes	Yes
1	01001	Reserved	No	TBD	No
1	01111	Reserved	No	TBD	No
1	10000	Transmit vector word	Yes	No	Yes
0	10001	Synchronize	Yes	Yes	Yes
1	10010	Transmit last command	Yes	No	Yes
1	10011	Transmit bit word	Yes	No	Yes
0	10100	Selected transmitter shutdown	Yes	Yes	Yes
0	10101	Override selected transmitter shutdown	Yes	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD	No
1 or 0	11111	Reserved	Yes	TBD	No

(1) The response for this command depends only on the legalization bit in the Characterization word. There is no special treatment associated with this command.

3.5.5 No response time-out management

The IP1553 is able to handle programmable no response time-out. The time-out value is taken into account to detect a no-response from a Remote Terminal in a RT to RT transfer. The TimeOut bit (C53CFReg) determines the chosen value for no response time-out. The smallest value is 14 µs (TimeOut = "0"), and the highest value is 31 µs (TimeOut = "1").

3.5.6 Redundancy management

The IP1553 is fully compliant to § 4.6 of document AD1.

The IP1553 is able to detect any incoming command on either the nominal or the redundant bus and respond on the bus it has been activated by.

The content of the internal registers (Status word register, Last Command register and BIT register) always corresponds to a transfer performed on the active bus.

If a transfer is interrupted on a 1553B bus by a valid command incoming on the other bus and addressing the RT, the IP1553 stops the processing of the previous command and start the processing of the new command.

3.5.7 Test support & Error report

3.5.7.1 Built-In-Test (BIT) word

This 16 bit word provides error information for each 1553B transfer.

The BIT word corresponds to the bit description given in § 3.5.2.3.

3.5.7.2 Loop test

Each word transmitted within a given message transfer is looped back through the active receiver channel for wrap-around test. The loop test is made at the level of the transceiver/transformer connection. This function is enabled only when LTEN_N input pin is low level.

The result of the loop test is stored in LP bit of the BIT word: LP bit set to "1" will indicate an error. In case of error, the transmission on the 1553B bus is aborted.

3.5.7.3 Transmission time-out

The IP1553 contains a time-out to preclude a signal transmission of greater than 800 µs. If this time-out triggers, then TTO0 or TTO1 and TTOFLG is set to "1" in the BIT word (see § 3.5.2.3).

This function does not preclude a correct transmission in response to a command.

Reset of this time-out function is performed by the reception of a valid command addressing the RT on the bus on which the time-out has occurred.

3.5.7.4 "Data wrap around Test" and "Self test"

The IP1553 does not implement a "Self Test".

During operating state, the loop test indicates that the encoder and decoder work properly.

The Application which uses the IP1553 manages the "Data wrap around Test" if this test is executed. The Application uses whichever subaddress needed to perform this test, by transferring the data received to the transmit buffer.

3.5.8 Memory management

The data management function ensures the following points:

- The transfer of received data from the 1553B bus to the memory,
- The availability of these data for the Application,
- The transfer of data to transmit on the 1553B bus from the memory.

The IP1553 realizes the memory management and communicate with the memory controller. It uses a shared area in memory. This area is defined by the Application thanks to MemArea bits (C53CFReg). MemArea defines an area for the IP1553 of 128Kwords. This area can be placed in memory at each multiple of 128K word address in the whole memory, i.e. when MemArea is increased by 1 the IP1553 area will be moved of 128 K word address. There are three different areas in this shared memory:

- A command area which size is 4 Kwords including the received command words, control words associated to these commands, associated data to Mode commands, characterization words and two double indirection tables of 32 addresses;
- A data received area which size is 32 Kwords including data words received on 1553B bus;
- A data to transmit area which size is 32 Kwords including data words to transmit on 1553B bus.

3.5.8.1 Command area

There are the following parts in the command area (Figure 23):

- A circular buffer, which contains the received command words on the 1553B bus. When a command is received and legalized, the IP1553 writes in this buffer at the end of the exchange the command word received, a control word giving information about the exchange and a 32 bit word containing a 21 bit dating field and the block number where the data of the command have been stored.

  This buffer is in write access mode by the IP1553 and in read access mode by the Application, the LastCmdAd bits in the C53CDSTReg gives the address in the command area of the last command treated.

  At the end of the buffer, the access pointer takes the beginning address of the area.

- Two 32 word tables including the data associated to each Mode Command.

  The first table contains the data associated to receive Mode command. It is in write access mode by the IP1553 and in read access mode by the Application. The Mode Code of the command gives the address in the table.

The second table contains the data associated to transmit Mode command. It is in read access mode by the IP1553 and in write access mode by the Application. The Mode Code of the command gives the address in the table.

- A 32 word table including characterisation words. Each word contains information about the legalization of the command (LEG bit), the enable of the ItTrok bit in the C53NITReg (TROK bit) and the Status response thanks to SSFB and SREQ bits. The Application initializes this table in order to allow the IP1553 to use it.

  When the IP1553 receives a command, it accesses to this table to read the characterization word associated to the command word received. The Sub Address or the Mode Code gives the address in the table.

- A double 32 word table giving the beginning block number for receive data, the maximum size of the buffer in blocks and the next block to be used by the IP1553 in the data area for each 32 Sub Address. The Application initializes this table in order to allow the IP1553 to use it.

  The table word is as described Figure 20 (detailed description § 3.5.8.4):

B31	B30.....B21	B20.....B11	B10.....B0
ADUPD	Current block	Maximum buffer size	Beginning buffer reception block

Figure 20: Indirection table word for reception

When a Receive Command is received, the IP1553 reads the Indirection table word at the address given by the Sub Address. Then the IP1553 writes the received data in the data area starting at the Beginning buffer reception block (BRBlk) + Current block value (CurBlk). The value of the CurBlk field is zero at the beginning. The size of a block is 16 (32 bit words) when 32 bit Word mode is activated, otherwise the size is 32 (32 bit words, but only MSB are used). Once this task is finished, the IP1553 compares the Maximum buffer size (MaxBS) with (CurBlk+1):

- If the buffer is not full (CurBlk + 1 < MaxBS), the IP1553 updates the CurBlk if the bit Address Update (ADUPD) is set to "1" by writing CurBlk+1. If the ADUPD bit is not set, the CurBlk does notbe updated and the next data received at this same Sub Address is written at the CurBlk + BRBlk. Meanwhile, the BRBlk may have been modified by the Application.
- If the buffer is full (CurBlk + 1 = MaxBS), the IP1553 changes its internal table indicator for this Sub Address in order to point on the complementary table at the time of the next Receive command at this Sub Address. The IP1553 updates the CurBlk field with zero and generate the C53It interrupt through the ItSwitch bit (C53NITReg) activation.

The IP1553 maintains a table, which contains the table indicator for each Sub Address. This indicator is reported in the Control Word associated to the received command.

At initialization, the IP1553 uses the table 0, which starts at "MemArea+10F80H" and ends at "MemArea+10F9FH". When the buffer available will be full and if the ADUPD bit is set to "1", the IP1553 uses the table 1 which starts at "MemArea+10FA0H" and ends at "MemArea+10FBFH" for the Sub Address considered. It warns the Application thanks to C53It. When the buffer defined by the table 1 will have be full and if the ADUPD bit is set to "1", the IP1553 uses the table 0 again, and so on…

- A double 32 word table giving the beginning block number for transmit data, the maximum size of the buffer in blocks and the next block to be used by the IP1553 in the data area for each 32 Sub Address. The Application initializes this table in order to allow the IP1553 to use it

  The table word is as described in Figure 21 (detailed description § 3.5.8.4)

B31	B30.....B21	B20.....B11	B10.....B0
ADUPD	Current block	Maximum buffer size	Beginning buffer transmission block

Figure 21: Indirection table word for transmission

When a Transmit Command is received, the IP1553 reads the Indirection table word at the address given by the Sub Address. Then the IP1553 reads the data to transmit in the data area starting at the Beginning buffer transmission block (BTBlk) + Current block value (CurBlk). The value of the CurBlk field is zero at the beginning. The size of a block is 16 (32 bit words) when 32 bit Word mode is activated, otherwise the size is 32 (32 bit words, but only MSB are used). Once this task is finished, the IP1553 compares the Maximum buffer size (MaxBS) with (CurBlk+1):

- If the buffer is not entirely read (CurBlk + 1 < MaxBS), the IP1553 updates the CurBlk if the bit Address Update (ADUPD) is set to "1" by writing CurBlk+1. If the ADUPD bit is not set, the CurBlk is not updated and the next data to transmit from this same Sub Address is read at the CurBlk + BTBlk. Meanwhile, the BTBlk may have been modified by the Application.
- If the buffer is entirely read (CurBlk +1 = MaxBS), the IP1553 changes its internal table indicator for this Sub Address in order to point on the complementary table at the time of the next Transmit command at this Sub Address. The IP1553 updates the CurBlk field with zero and generate the C53It interrupt through the ItSwitch bit (C53NITReg) activation.

The IP1553 maintains a table, which contains the table indicator for each Sub Address. This indicator is reported in the Control Word associated to the received command.

At initialization, the IP1553 uses the table 0, which starts at "MemArea+10FC0H" and ends at "MemArea+10FDFH". When the buffer available has been entirely read and if the ADUPD bit is set to "1", the IP1553 uses the table 1 which starts at "MemArea+10FE0H" and ends at "MemArea+10FFFH" for the Sub Address considered. It warns the Application thanks to C53It. When the buffer defined by the table 1 has been entirely read and if the ADUPD bit is set to "1", the IP1553 uses the table 0 again, and so on…

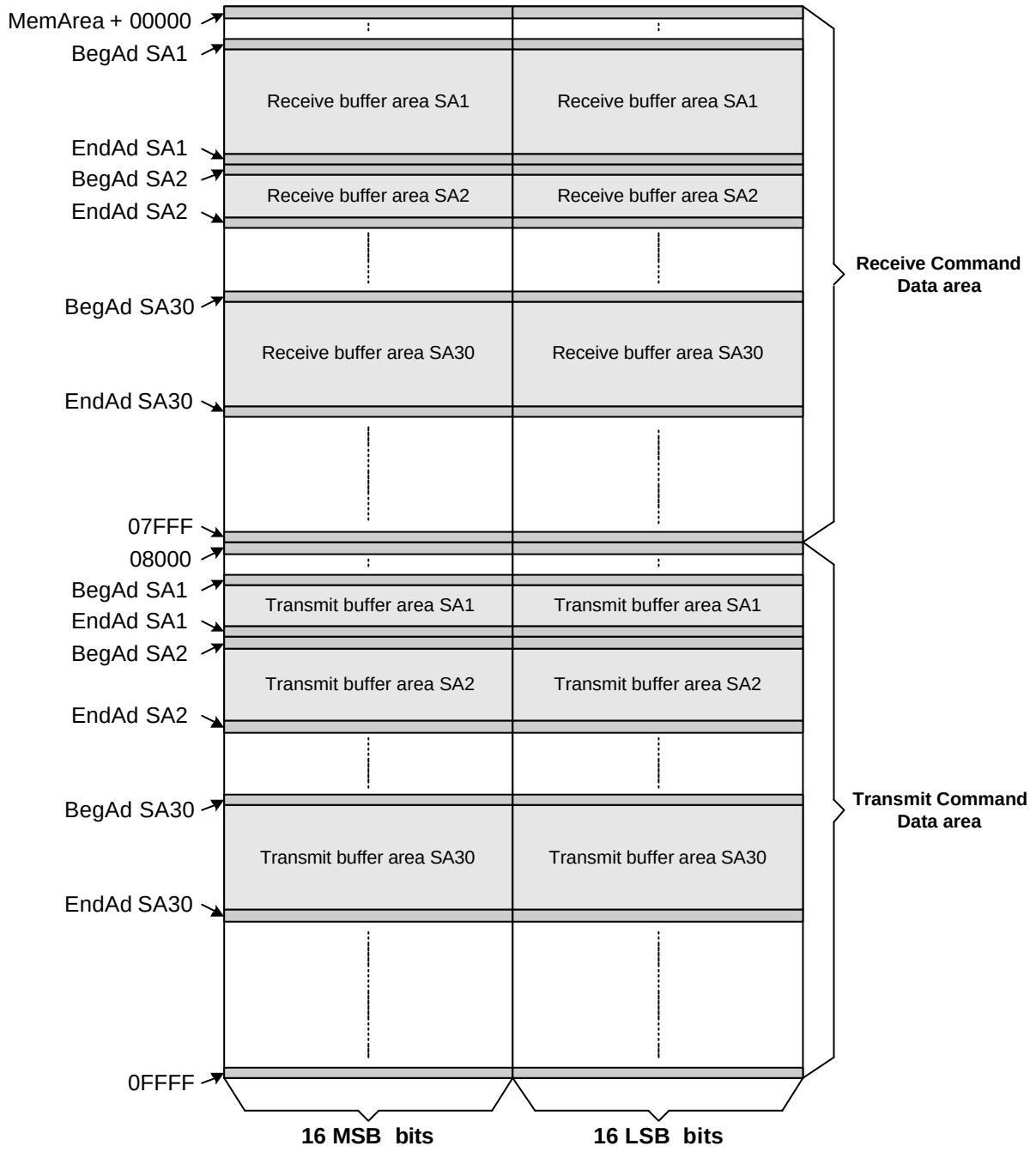

Figure 22: Data area mapping in RT mode

Note: The addresses in Figure 22 are address words.

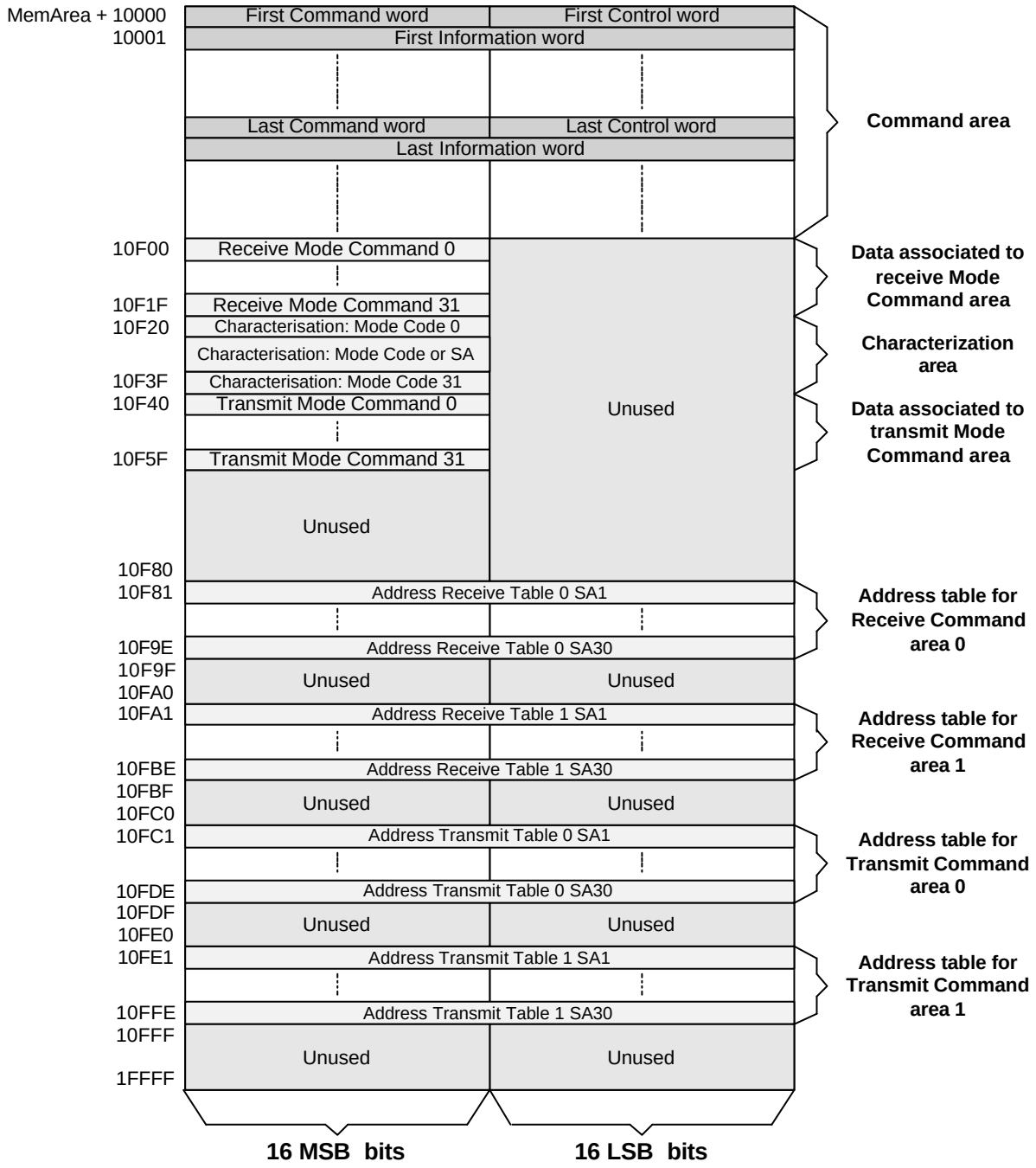

Figure 23: Command area mapping in RT mode

Note: The addresses in Figure 23 are address words.

3.5.8.2 Data reception area

The data reception area contains the data received on the 1553B bus. This area starts at "MemArea+00000H" and ends at "MemArea+08000H", that is to say 32 Kwords. It is virtually divided in 30 sub areas corresponding to the 30 Sub Address. Each sub area is identified by its BRBlk and MaxBS, written in the Indirection table word at the address related to the Sub Address of the received command. Each sub area contains whether one or several 16 word wide buffers if the 32 bit Word mode is activated, else one or several 32 word wide buffers to memorize the received data. The Figure 24 & Figure 25 show how the data are mapped:

	16 Most Significant Bits	16 Least Significant Bits
BRBlk+CurBlk & 0	1st 1553 Data received	2nd 1553 Data received
BRBlk+CurBlk & 1	3rd 1553 Data received	4th 1553 Data received
	⋮	⋮
BRBlk+CurBlk & E	29th 1553 Data received	30th 1553 Data received
BRBlk+CurBlk & F	31th 1553 Data received	32nd 1553 Data received

Figure 24: Data reception buffer mapping when 32 bit Word mode

	16 Most Significant Bits	16 Least Significant Bits
BRBlk+CurBlk & 00	1st 1553 Data received	Unused
BRBlk+CurBlk & 01	2nd 1553 Data received	
	⋮	
BRBlk+CurBlk & 1E	31th 1553 Data received	
BRBlk+CurBlk & 1F	32nd 1553 Data received	

Figure 25: Data reception buffer mapping when 16 bit Word mode

3.5.8.3 Data transmission area

The data transmission area contains the data to transmit on the 1553B bus. This area starts at "MemArea+08000H" and ends at "MemArea+0FFFFH", that is to say 32 Kwords. It is virtually divided in 30 sub areas corresponding to the 30 Sub Address. Each sub area is identified by its BTBlk and CurBlk, written in the Indirection table word at the address related to the Sub Address of the received command. Each sub area contains whether one or several 16 word wide buffers if the 32 bit Word mode is activated, else one or several 32 word wide buffers to memorize the data to transmit. The Figure 26 and Figure 27 show how the data are mapped:

	16 Most Significant Bits	16 Least Significant Bits
BTBlk+CurBlk & 0	1st 1553 Data to transmit	2nd 1553 Data to transmit
BTBlk+CurBlk & 1	3rd 1553 Data to transmit	4th 1553 Data to transmit
	⋮	⋮
BTBlk+CurBlk & E	29th 1553 Data to transmit	30th 1553 Data to transmit
BTBlk+CurBlk & F	31th 1553 Data to transmit	32nd 1553 Data to transmit

Figure 26: Data transmission buffer mapping when 32 bit Word mode

	16 Most Significant Bits	16 Least Significant Bits
BTBlk+CurBlk & 00	1st 1553 Data to transmit	Unused
BTBlk+CurBlk & 01	2nd 1553 Data to transmit	
	⋮	
BTBlk+CurBlk & 1E	31th 1553 Data to transmit	
BTBlk+CurBlk & 1F	32nd 1553 Data to transmit	

Figure 27: Data transmission buffer mapping when 16 bit Word mode

3.5.8.4 Memory words structure

There are 6 different words used by the IP1553 in the memory. The data words, the command words correspond to the document AD2. The Control Word, the Characterization Word, the Indirection Word and the Information Word are described hereafter:

- Control Word:

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
DV	T	RT-RT	BUSID	NULL	MEMERR	TTO0	TTO1	TFINH	HIWRD	LOWRD	UNDCMD	T/R_ILL	LP	BUSYAP	TTOFLG

Figure 28: Control Word structure

DV	Data Valid
T	Indirection table number used for the command treatment
RT-RT	RT-RT command received (when IP1553 is the receiving RT)
BUSID	Command received on the nominal (“0”) or redundant (“1”) bus
MEMERR	HResp input = Error for memory access
TTO0	Transmission time-out activation on bus 0
TTO1	Transmission time-out activation on bus 1
TFINH	Inhibition of Terminal Flag bit
HIWRD	Number of words received higher than expected
LOWRD	Number of words received lower than expected
UNDCMD	Undefined Command received
T/R_ILL	Bit T/R illegal in the Mode command received
LP	Loop test failure indicator
BUSYAP	Application Interface is busy (Time-out error for memory access)
TTOFLG	Transmission time-out activation on active bus
NULL	Unused (“0”)

During a nominal exchange bits B11 to B0 is set to “0”. For “Transmit Last Command”, “Transmit Status” and “Transmit BIT”, the control word written represents the state of the previous command.

- Characterization word:

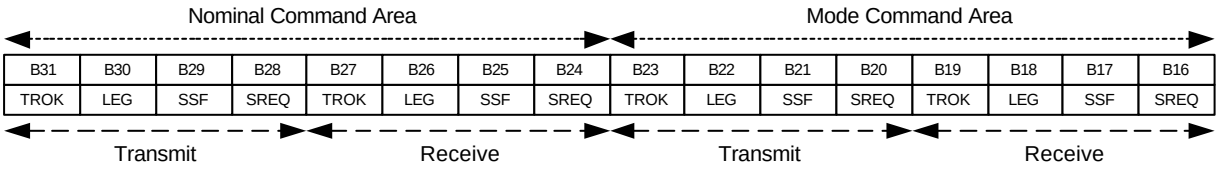

Figure 29: Characterization word structure

TROK	Enable of the ItTrok bit (C53NITReg)
LEG	Legalization bit: “0” Illegal / “1” Legal
SSF	Sub System Flag bit
SREQ	Service Request bit

For the Sub Address 31 and 32 (“00000b”), the bits B31 to B24 are irrelevant, as the command is a Mode command.

- Information words:

These words are written by the IP1553 after the command and control word in the command area for each valid and legal command treated.

When 32 bit Word mode, the fields in the indirection table are defined hereafter:

B31	B30.....B21	B20.....B11	B10.....B0
ADUPD	Current block	Maximum buffer size	Beginning buffer transmission block

B31	B30.....B21	B20.....B11	B10.....B0
ADUPD	Current block	Maximum buffer size	Beginning buffer reception block

Figure 30: Indirection table word for reception when 32 bit Word mode

Beginning buffer transmission or reception block field is 11 bits wide. We can access every block of 16 words of 32 bits (a full 1553 data buffer) in the data reception or transmit area, which size is 32 Kwords.

Maximum buffer size field is 10 bits wide. We cannot allocate more than 16 Kwords to a single Sub Address.

(Maximum buffer size value + Beginning buffer block value) must be lower than 7FFH, which is the address of the last block in the transmission or reception area.

B31.....B21	B20.....B0
Data block number	Dating

Figure 31: Information word structure when 32 bit Word mode

The Data block number field is 11 bits wide. Its value corresponds to the sum of Beginning buffer block and Current block. In case of Mode Command, Extended Memory mode or 1553 exchange error (Data Valid bit = “0”) this field has no significance and corresponds to the value of the last valid and legal command, which is not a Mode command. The Data block number for the first block of the memory is zero.

The Dating field is the copy of the DATEBUS input. This may be used as a mean to date the exchange. This copy is made at the end of the exchange.

When 16 bit Word mode, the fields in the indirection table are defined hereafter:

B31	B30.....B21	B20.....B11	B10.....B0
ADUPD	Current block	Maximum buffer size	Beginning buffer transmission block

B31	B30.....B21	B20.....B11	B10.....B0
ADUPD	Current block	Maximum buffer size	Beginning buffer reception block

Figure 32: Indirection table word for reception when 16 bit Word mode

Beginning buffer transmission or reception block field is 11 bits wide. But only the 10 LSB is used by the IP1553. We can access every block of 32 words of 16 most significant bits of the 32 bit words (a full 1553 data buffer) in the data reception or transmit area, which size is 32 Kwords.

Maximum buffer size field is 10 bits wide. We can allocate up to 32 Kwords to a single Sub Address.

(Maximum buffer size value + Beginning buffer block value) must be lower than 3FFH, which is the address of the last block in the transmission or reception area.

B31	B30.....B21	B20.....B0
0	Data block number	Dating

Figure 33: Information word structure when 16 bit Word mode

The Data block number field is 10 bits wide. Its value corresponds to the sum of Beginning buffer block and Current block. In case of Mode Command, Extended Memory mode or 1553 exchange error (Data Valid bit = "0") this field has no significance and corresponds to the value of the last valid and legal command, which is not a Mode command. The Data block number for the first block of the memory is zero.

The Dating field is the copy of the DATEBUS input. This may be used as a mean to date the exchange. This copy is made at the end of the exchange.

3.5.8.5 Extended Area access to the memory

The IP1553 provides 5 bits (ExtSubAd bits in C53CFReg) which are written by the Application to define a Sub Address to be used with the Extended Area mode. This mode is activated thanks to the ExtArea bit (C53CFReg). If this bit is set to "0", the ExtSubad is treated as the others.

The Extended Area mode allows the IP1553 to access the whole memory in write or read mode. The beginning address of these access is provided by the Extended Memory Base Address register (C53EMBAReg). The IP1553 is then able to access memory areas outside of the 128 Kwords normally provided thanks to MemArea bits (C53CFReg). In this peculiar case, there is not an end area address: the C53EMBAReg is incremented for each double 1553 word read or write in the memory, when the Sub Address defined is used and the Extended Area mode allowed. The words count associated to each 1553 command for this Sub Address is even.

The C53EMBAReg is programmable by the 1553B bus thanks to a Receive command with only two words sent to (ExtSubAd + 1). The 10 LSB of the first 1553 data is stored in the bits 25 to 16 of the C53EMBAReg(25 downto 0). The second data word is stored in the 16 LSB bits of this register.

3.6 BUS MONITOR (BM) MODE

3.6.1 BM mode working scheme

In the Bus Monitor mode, the IP1553 captures all 1553B words on either the nominal or redundant bus. Each message is transferred along with an Identification word and stored in the memory.

A Monitoring stack consists in two buffers (A and B), accessed in toggle mode.

When monitoring in continuous mode (CdtCirBuf bit set to “1”) the IP1553 uses alternatively buffers A and B (buffer A is used first, then buffer B…).

When monitoring in “one shot” mode (CdtCirBuf bit set to “0”), the IP1553 uses buffer A, then buffer B, and then stops.

So in Bus Monitor mode, the IP1553 follows the basic sequence described hereafter (see Figure 34):

- Wait for activation on GoStop bit,
- Read the “Buffer A start address word” and the “Buffer A stop address word” in memory,
- Then store the “Current buffer pointer” in memory in case of Memory access error (Time-out or Hresp input = Error), generate C53Err interrupt through ErrMem bit activation then return to “Stand-by state”,
- Wait for a 1553B word, then store it in the Buffer with the associated Identification word,
- Then store the “Current buffer pointer” in memory in case of Memory access error, generate C53Err interrupt through ErrMem bit activation then return to “Stand-by state”,
- Or store the “Current buffer pointer” in memory if GoStop bit is deactivated, or if Buffer B is full and “one shot” mode selected, then return to “Stand-by state”,
- Or store the “Current buffer pointer” in memory if current buffer is full, initialize the “Buffer start address word” and the “Buffer stop address word” with the information related to the complementary buffer, generate C53It interrupt through ItSync bit activation then wait for the next 1553B word,
- Otherwise stay in “Active state” and wait for the next 1553B word.

In addition, the Busyflag bit (C53CDSTReg) is forced to high level by the IP1553 to indicate that it is in the “Active state”, otherwise Busyflag bit is low level.

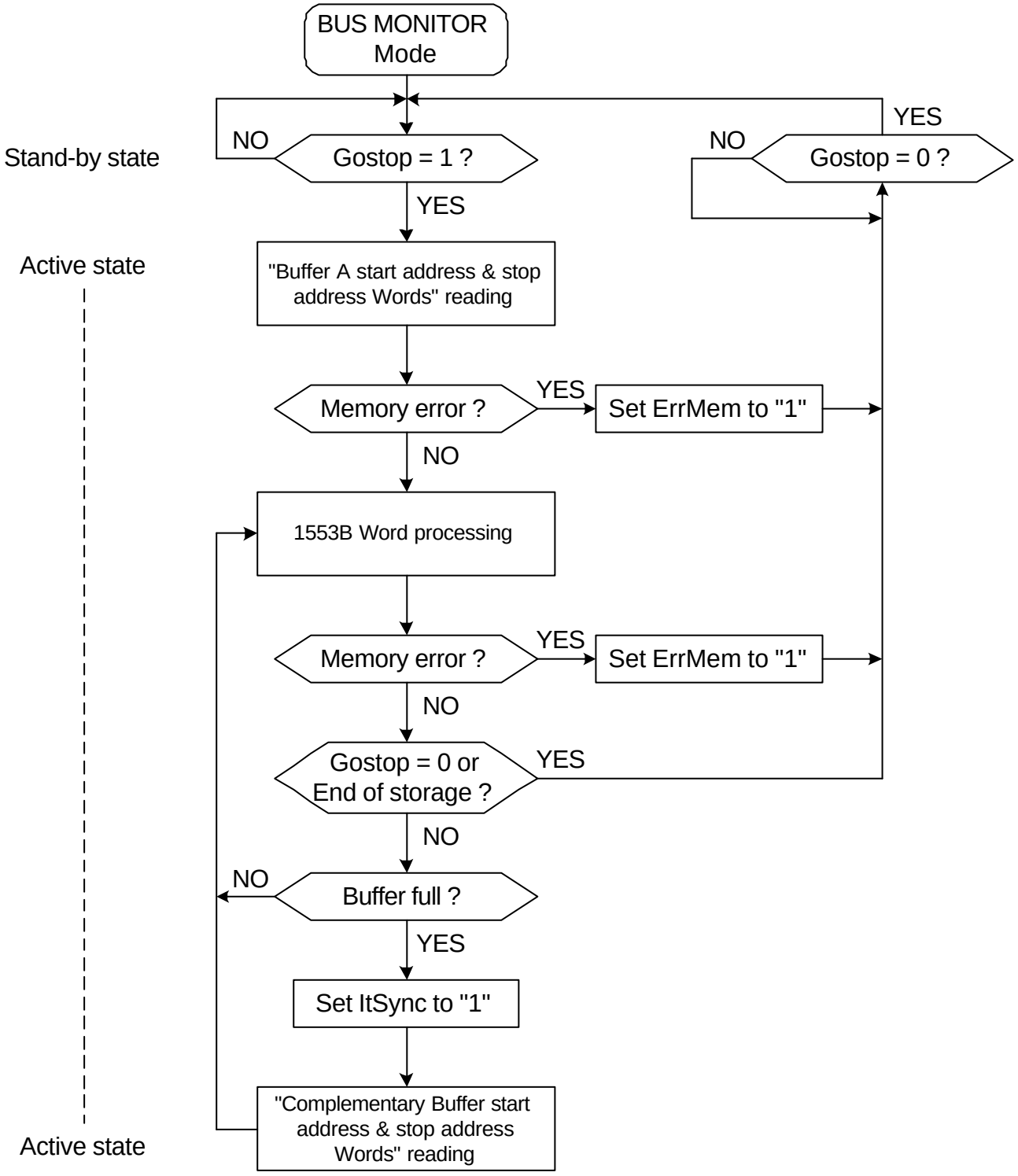

Figure 34: BM working sequence

Note: “End of storage” means Buffer B full and “one shot” mode selected

3.6.2 BM mode internal registers definition

In BM mode, the IP1553 provides at least the following internal registers of 16 bits : “Buffer start address register”, “Buffer stop address register”, “Buffer pointer register” and “Identification word register” which definitions are hereafter.

3.6.2.1 Buffer start address register and Buffer stop address register

It is possible to specify the location and the size of each monitoring buffer used to store the 1553B words and their associated Identification words.

The Buffer start address register contains the first address of the current buffer (A or B), and the Buffer stop address register contains the last address of the current buffer (A or B).

When entering the “Active state”, these two registers are initialized as follows:

- The “Buffer start address word” is read at location “MemArea+00000H” in the data area of the memory,
- The “Buffer stop address word” is read at location “MemArea+00001H” in the data area of the memory.

When toggling from buffer A (resp B) to buffer B (resp A), these two registers are initialized as follows:

- The “Buffer start address word” is read at location “MemArea+00002H” (resp “MemArea+00000H”) in the data area of the memory,
- The “Buffer stop address word” is read at location “MemArea+00003H” (resp “MemArea+00001H”) in the data area of the memory.

3.6.2.2 Buffer pointer register

When entering the “Active state”, the Buffer pointer register is initialized by the “Buffer start address word” read at location “MemArea+00000H” in the data area of the memory.

When toggling from buffer A (resp B) to buffer B (resp A), the Buffer pointer register is initialized by the “Buffer start address word” read at location “MemArea+00002H” (resp “MemArea+00000H”) in the data area of the memory.

In “Active state”, this register contains the address in the data area of the next word to be stored.

In case of Memory access error, the IP1553 stores the “Buffer pointer register” at location “MemArea+00004H in the data area, generate C53Err interrupt through the ErrMem bit activation (C53EITReg), then return to “Stand-by state”.

At high to low transition of GoStop bit or if Buffer B is full in “one shot” mode, the IP1553 stores the “Buffer pointer register” at location “MemArea+00004H” in the data area, then return to “Stand-by state”.

When toggling from buffer A to buffer B or from buffer B to buffer A, the IP1553 stores the “Buffer pointer register” at location “MemArea+00004H” in the data area of the memory, generate C53It interrupt through the activation of ItSync bit (C53NITReg), and continue recording.

3.6.2.3 Identification word register

This register contains information generated by the IP1553 related to the last word received: word validity, bus identifier, word type, and dating. This register is stored in memory after each valid data word.

The function of the 16 bits composing Identification word is as described hereafter:

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
WERR	BUSID	SYNCID	GAP	TOEXC	TIM10	TIM9	TIM8	TIM7	TIM6	TIM5	TIM4	TIM3	TIM2	TIM1	TIM0

Figure 35: Identification word structure (Bits number in case of 16 bit Word mode)

WERR	Word error:
	"0": Previous word valid
	"1": Previous word is invalid: Parity error coding error ...
BUSID	1553B Bus identifier:
	"0": Bus 0
	"1": Bus 1
SYNCID	Synchronization identifier:
	"0": Command/Status word
	"1": Data word
GAP	Gap between data words:
	"0": Data words are contiguous
	"1": Gap exists between previous word and current word
TOEXC	Time-out exceeded (see 3.6.4):
	"0": Gap between consecutive words does not exceed time-out
	"1": Gap between consecutive words exceeds time-out
TIM10	Time bit 10 (MSB)
TIM9	Time bit 9
TIM8	Time bit 8
TIM7	Time bit 7
TIM6	Time bit 6
TIM5	Time bit 5
TIM4	Time bit 4
TIM3	Time bit 3
TIM2	Time bit 2
TIM1	Time bit 1
TIM0	Time bit 0 (LSB)

If an invalid word is received (Parity error, Manchester error…), the wrong word is not stored in memory but the error is memorized in the Identification word (WERR bit set to "1") of the next valid data word.

The dating corresponds to a gap time: it indicates the time between receipt of the previous and current word.

The resolution of this dating is 2 µs. The width of the timer (11 bits: TIM0 to TIM10) allows to measure a delay up to 2^{12} µs. If the delay exceeds the width of the timer, BIT0 to BIT10 is all set to "1".

3.6.3 BM mode special functions

3.6.3.1 GoStop bit (C53CDSTReg)

It is possible to control the IP1553 activity with this bit: a low to high transition or a high level allows the IP1553 to start/continue its 1513B word processing, otherwise it stays/returns to “Stand-by state” (after completion of the current 1553B word processing).

When the input HALT is set to “1” the IP1553 behaves as if GoStop bit is set to “0”. Otherwise the IP1553 follows the value of the bit GoStop.

3.6.3.2 Memory access error

When the IP1553 encounters a Memory access error (Time-out access or Hresp input = Error), it stores the “Buffer pointer register” at location “MemArea+00004H” in data area, generate C53Err interrupt through ErrMem bit activation, then return to “Stand-by state”.

3.6.4 Time-out management

The IP1553 is able to handle programmable no response time-out.

The TimeOut bit (C53CFReg) determines the chosen value for no response time-out. The smallest value is 14 µs (TimeOut = “0”), and the highest value is 31 µs (TimeOut = “1”).

The time-out value is taken into account to update TOEXC bit of the Identification word as follows:

- If the time measured from mid-bit crossing of parity bit of previous word to mid-bit crossing of synchronization bit of current word exceeded time-out value, then TOEXC is set to “1”,
- Otherwise TOEXC is set to “0”.

3.6.5 Redundancy management

The IP1553 is able to monitor bus activity on either the nominal or redundant bus. A bit in the Identification word (BUSID) indicates the bus on which the word has been received.

3.6.6 Memory management

MemArea defines an area for the IP1553 of 128Kwords. This area can be placed in memory at each multiple of 128K word address in the whole memory, i.e. when MemArea is increased by 1 the IP1553 area will be moved of 128 K word address.

The IP1553 should be able to address up to 64 Kwords (16 bits) of data area.

The data area is addressed thanks to the content of the “Buffer pointer register”, which is incremented at each storage operation.

Each 1553B word is stored in the data area with an Identification word which provides the Application with additional information concerning the received 1553B message.

The data area is structured as a Monitoring stack, which automatically wraps around once it has been filled if CdtCirBuf bit (C53CFReg) is set to “1”, otherwise it stops at the end of the buffer B filling if CdtCirBuf bit is set to "0”.

When toggling from one buffer to the other, the interrupt C53It is generated through the ItSync bit activation if not masked by ItSyncMask bit (C53CFReg), see § 3.6.1.

The Monitoring stack mapping corresponds to Figure 38.

The 1553B and Identification words are stored in memory as shown in Figure 36 and Figure 37. The bits WdSize and DW16En (C53CFReg) determine if the IP1553 stores the words in 32 bit words or 16 bit words.

16 Most Significant Bits	16 Least Significant Bits
1st 1553B word	Unused
1st Identification word	
2nd 1553B word	
2nd Identification word	

Figure 36: 1553B and Identification words mapping with 16 bit Word mode

16 Most Significant Bits	16 Least Significant Bits
1st 1553B word	1st Identification word
2nd 1553B word	2nd Identification word

Figure 37: 1553B and Identification words mapping with 32 bit Word mode

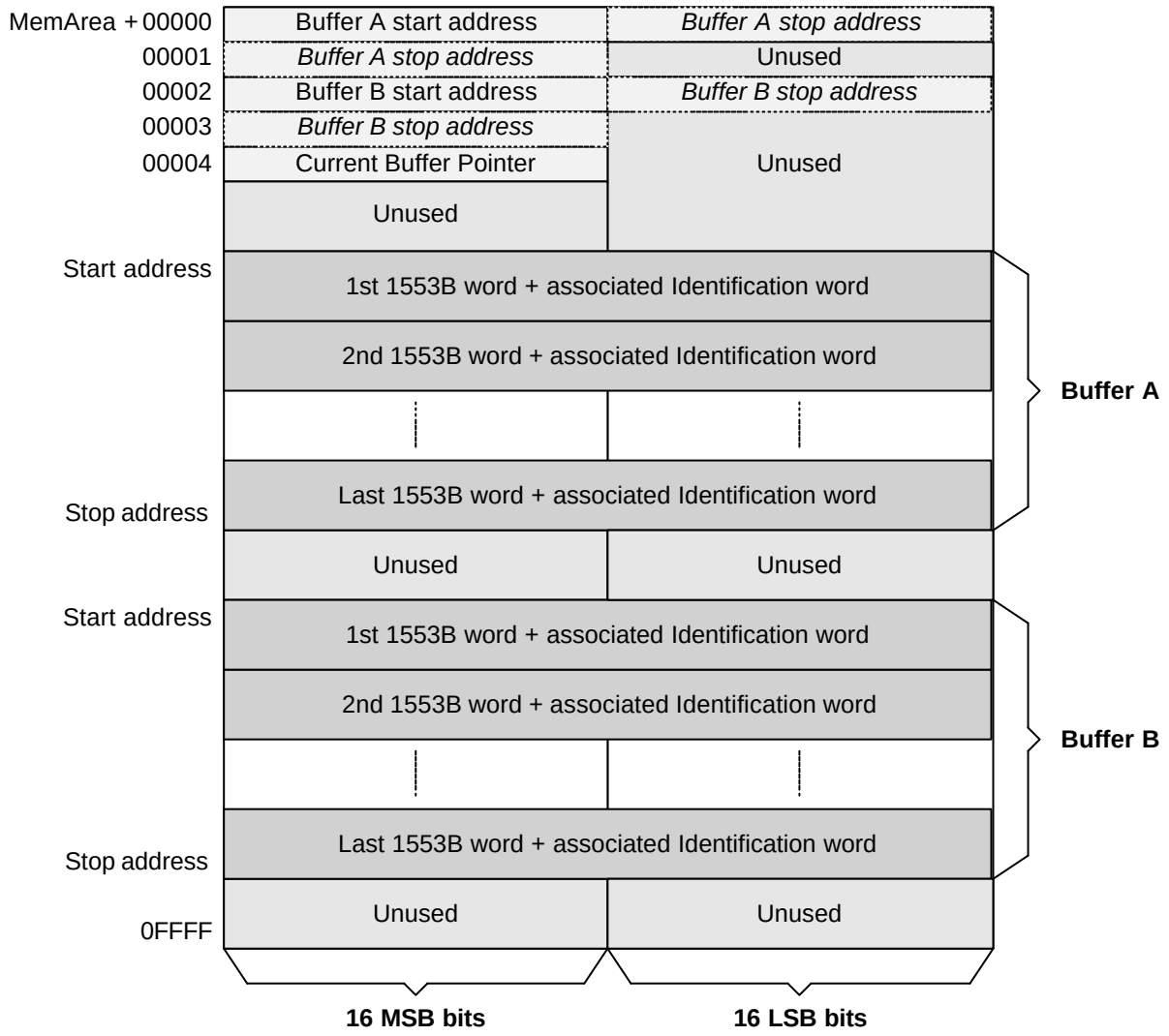

Figure 38: Data area mapping used in BM mode

Note:

If 32 bit Word mode, the Buffer A stop address and the Buffer B stop address are placed in LSB of the 32 bit words at MemArea + 00000H and MemArea + 00002H of memory.

If 16 bit Word mode, the Buffer A stop address and the Buffer B stop address are placed in MSB of the 32 bit words at MemArea + 00001H and MemArea + 00003H of memory.

3.7 IP1553 SYSTEM INTERFACE

3.7.1 Application interfacing scheme

3.7.2 Transceivers interface

The IP1553 is able to support a redundant 1553B bus.

Each connection to a 1553B bus is done through a Transceiver and a Transformer as shown in Figure 39.

Each Transceiver – IP1553 interface is composed of at least 5 signals: RX & RXB input signals for Receiver section, TX & TXB & TXINH output signals for Transmitter section. The waveform of these signals is in accordance with Figure 40 & Figure 41.

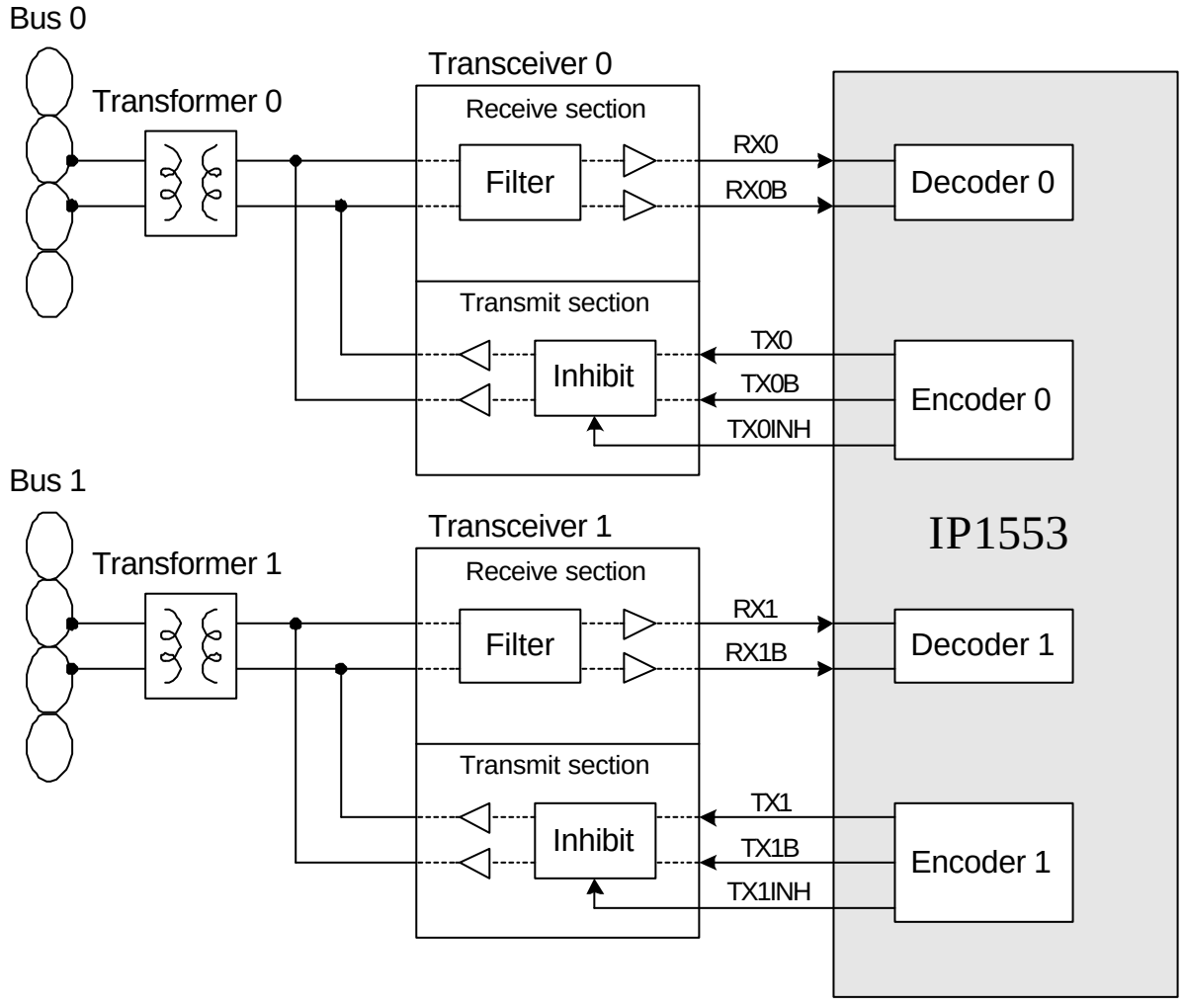

Figure 39: Transceiver interface

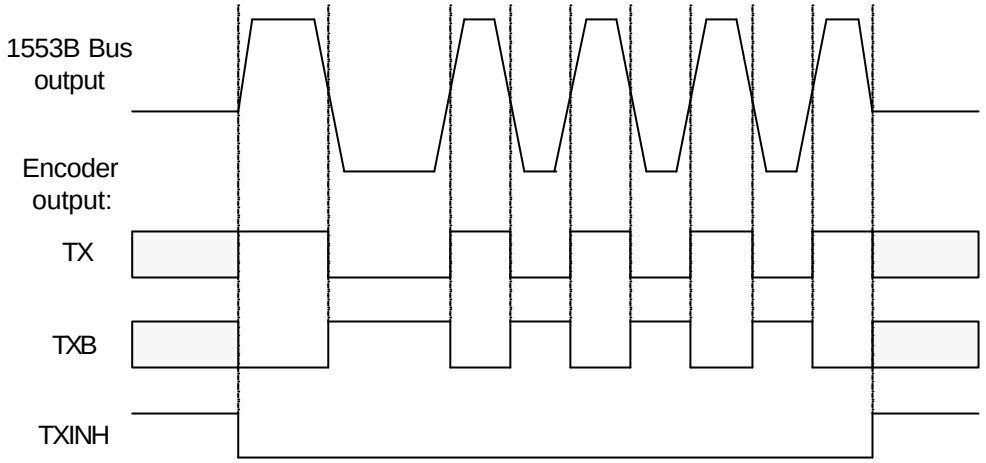

Figure 40: Transmitter signals waveform

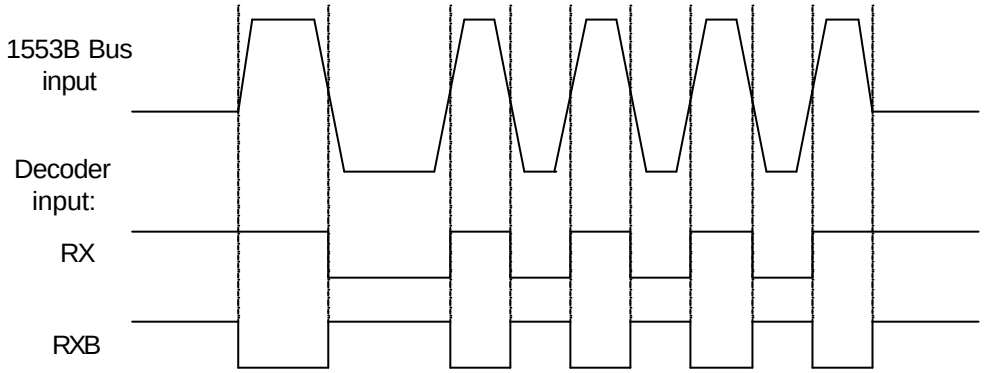

Figure 41: Receiver signals waveform

3.7.3 IP1553 Interrupts support

The IP1553 is able to inform the Application about special events, which are likely to happen. When these events occur, an output interrupt is generated. There are 3 different interrupts: a nominal, a reset and an error interrupt, which the causes are sometimes multiple. They are described hereafter:

- **C53It**: Nominal interrupt. It is generated thanks to the following bits activation: ItTrok, ItSync, ItDbc and ItSwitch. To generate the interrupt, the IP1553 combines these sources with a logical OR. These bits are in the Nominal Interrupt register (C53NITReg).
  - ItTrok: Maskable bit (ItTrokMask in C53CFReg). In RT mode, this bit is set to "1" at the end of each valid exchange. It is reset to "0" upon C53NITReg read access.
  - ItSync: Maskable bit (ItSyncMask in C53CFReg). In RT mode, this bit is set to "1" after "Synchronize" Mode command reception if this command is legalized. In BC mode, this bit is set to "1" after the execution of an Instruction block with SYNC bit set in the first Instruction word. In BM mode, this bit is set to "1" when the IP1553 toggles from one buffer to the other. It is reset to "0" upon C53NITReg read access.

- ItDbc: Non maskable bit. In RT mode, this bit is set to “1” after “Dynamic bus control” Mode command reception if this command is legalized. It is reset to “0” upon C53NITReg read access.
- ItSwitch: Non maskable bit. In RT mode, this bit is set to “1” after change of data address table for a sub-address. It is reset to “0” upon C53NITReg read access.

- **C53Rst**: Reset interrupt. In RT mode, it is generated after “Reset remote terminal” Mode command reception if this command is legalized. The bit RstCom is reset to “0” upon C53RITReg read access.
- **C53Err**: Error interrupt. It is generated thanks to the following bits activation: ErrMem, Err1553, ErrInst and CwError. To generate the interrupt, the IP1553 combines these sources with a logical OR. These bits are in the Error Interrupt register (C53EITReg).
  - ErrMem: Non maskable bit. In all modes, this bit is set to “1” in case of Memory access error: time-out access or Hresp input = Error. It is reset to “0” upon C53EITReg read access.
  - Err1553: Maskable bit (Err1553Mask in C53CFReg). In RT mode, this bit is set to “1” in case of 1553 error. In BC mode, this bit is set to “1” if EXCERR flag is set in the Control word without additional retry allowed. It is reset to “0” upon C53EITReg read access.
  - CwError: Non maskable bit. In BC mode, this bit is set to “1” when the bit CWERR is set in the control word written in memory.
  - ErrInst: Non maskable bit. In BC mode, this bit is set to “1” in case of Illegal Instruction detection by the BC. It is reset to “0” upon C53EITReg read access.
  - ErrRTAd: Non maskable bit. In all modes, this bit is set to “1” in case of RTAD parity error. It is reset to “0” upon C53EITReg read access.

3.8 IP1553 PIN DESCRIPTION

Signal name	I/O	Description	Clock
1553B Bus interface			
RX0	I	Positive Manchester data signal coming from bus 0 via transceiver 0 and assigned to decoder 0	
RX0B	I	Negative Manchester data signal coming from bus 0 via transceiver 0 and assigned to decoder 0	
TX0	O	Positive Manchester data signal issued from encoder 0	1553CLK
TX0B	O	Negative Manchester data signal issued from encoder 0	1553CLK
TX0Inh	O	Transmitter 0 inhibition	1553CLK
RX1	I	Positive Manchester data signal coming from bus 1 via transceiver 1 and assigned to decoder 1	
RX1B	I	Negative Manchester data signal coming from bus 1 via transceiver 1 and assigned to decoder 1	
TX1	O	Positive Manchester data signal issued from encoder 1	1553CLK
TX1B	O	Negative Manchester data signal issued from encoder 1	1553CLK
TX1Inh	O	Transmitter 1 inhibition	1553CLK
Interrupts			
C53It	O	Nominal interrupt. If ItDbc, ItSync, ItSwitch or ItTrok are set to “1”, C53It is set to “1”	SYSCLK
C53Rst	O	Reset interrupt. In RT mode, C53Rst is set to “1” after “Reset Remote Terminal” reception	SYSCLK
C53Err	O	Error interrupt. If ErrMem, ErrInst, CwError, Err1553 or ErrRTAd are set to “1”, C53Err is set to “1”	SYSCLK
Configuration interface			
RTAD(4:0)	I	Remote Terminal Address: hardwired inputs corresponding to the chip address in RT mode	
RTParity	I	Parity information associated to Remote Terminal Address	
LTEN_N	I	This signal is used to enable/disable the loop test function	
TXEN_N	I	This signal is used to activate/inhibit the 2 transmitters sections	
Clocks and reset			
SYSCLK	I	Host Application clock	
1553CLK	I	IP1553 master clock: 16 MHz frequency	

RESET_N	I	Master reset. It lasts at least 70 ns to be seen by the IP1553	

Signal name	I/O	Description	Clock
Application interface			
SLOT	I	RTC Slot pulse	
CYCLE	I	RTC Cycle pulse	
HALT	I	Application Halt. This signal forces the bit GoStop to "0" when it is active, and have no effect when it is inactive.	
DELIN_N	I	Delay trigger input: in BC mode, this signal will be generated by the Application to synchronize the 1553B bus transfers through WAIT instruction.	
DATEBUS(20:0)	I	This input is stored in the memory in the Information word in RT mode at the end of a valid and legal RT exchange. It may be used as a mean to date the exchanges.	
SYNC_N	O	In BC mode, this signal is pulsed to "0" at the end of the execution of an instruction block, in which SYNC bit is set in the first instruction word. In RT mode, this signal is pulsed to "0" after reception of a valid and legal "Synchronize" (with or without data word) Mode command. In BM mode, this signal is pulsed to "0" when buffer A toggles with buffer B.	1553CLK
RSTCOM_N	O	This signal is pulsed to "0" after the reception of a valid and legal "Reset Remote Terminal" Mode command	1553CLK
MOD53(3:0)	O	Current state of the 1553 controller for debug test purpose. In BC mode, this signal represents the Code Operation of the instruction in treatment. In RT mode, this signal represents the current state of the main state machine.	SYSCLK
APB interface			
Paddr(3:0)	I	APB address bus	SYSCLK
Psel	I	APB select: this signal indicates that the IP1553 is selected and a data transfer is required.	SYSCLK
Penable	I	APB strobe: this signal is used to indicate the second cycle of an APB transfer	SYSCLK
Pwrite	I	APB transfer direction: when high this signal indicates an APB write access and when low a read access	SYSCLK
Prdata(32:0)	I	APB read data bus, the MSB is an odd parity bit	SYSCLK
Pwdata(32:0)	O	APB write data bus, the MSB is an odd parity bit	SYSCLK

Signal name	I/O	Description	Clock
AHB interface			
Hrdata(31:0)	I	AHB read data bus	SYSCLK
Hgrant	I	AHB bus grant: this signal indicates that the IP1553 is currently the highest priority master. The IP1553 gets access to the bus when both Hready and Hgrant are high	SYSCLK
Hready	I	AHB transfer done: when high this signal indicates that the slave is available	SYSCLK
Hresp	I	AHB transfer response: this signal provides additional information on the status of a transfer: OKAY and ERROR. The RETRY and SPLIT response are not managed	SYSCLK
Haddr(27:0)	O	AHB address bus. IP1553 uses word address so Haddr(1:0) are set to "00"	SYSCLK
Htrans(1:0)	O	AHB transfer type: this signal indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY. The BUSY is not managed	SYSCLK
Hwrite	O	AHB transfer direction: when high this signal indicates a write transfer and when low a read transfer	SYSCLK
Hsize(2:0)	O	AHB transfer size: this signal indicates the size of the transfer	SYSCLK
Hburst(2:0)	O	AHB burst type: this signal indicates if the transfer forms part of a burst. Only SINGLE and INCR mode are managed. For INCR burst the length is 2 words..	SYSCLK
Hprot(3:0)	O	AHB protection control	SYSCLK
Hwdata(31:0)	O	AHB write data bus	SYSCLK
Hbusreq	O	AHB bus request: this signal indicates that the IP1553 requires the bus	SYSCLK
Hlock	O	AHB locked transfers: when high this signal indicates that the IP1553 requires locked access to the bus and no other master should be granted the bus until this signal is low	SYSCLK

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