Extending TASTE through integration with Space Studio

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space codesign™

m3 SYSTEMS
RESEARCH - CONSULTING

Outline

1) Overview of the Space Studio platform for hardware/software (Hw/Sw) codesign

2) Demo

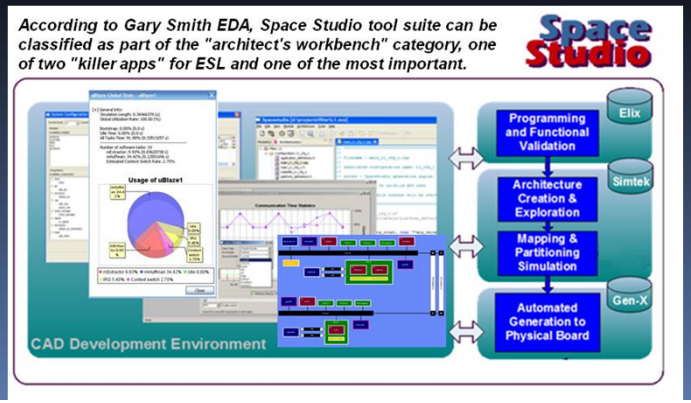
3) Propositions for adding Hw/Sw capabilities to TASTE

Problem and Market Need

- Electronics design is dealing with larger, more complex Hardware and Software that must work well together
- Rapid market changes impact product direction and strategy, changing requirements that drive design:
  - e.g.,Tablets versus Netbooks (iPad)
  - e.g., Smart versus Feature phone (iPhone)
- Decisions needed rapidly
- TI: Silicon Respin Cost – up to $3 Million (Synopsys)

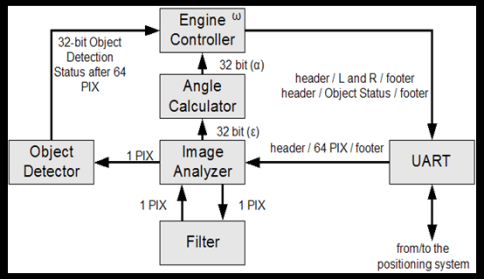
Solution Product & Technology

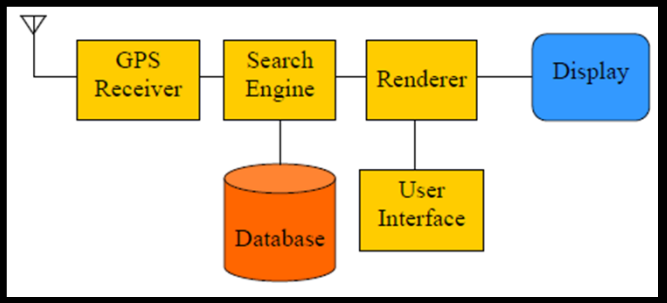
- Rapid decisions at front end of design process
  - Electronic System Level (ESL)
  - Create Large Complex Systems at Higher Level removes complexity of details …
  - Co-design of Software AND Hardware – together (Software content is increasing)



Mapping Problem (1)

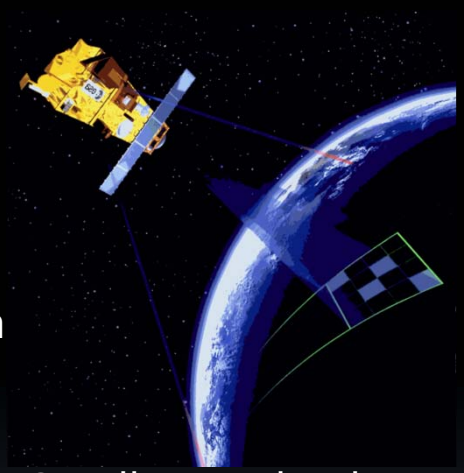
Vision based navigation





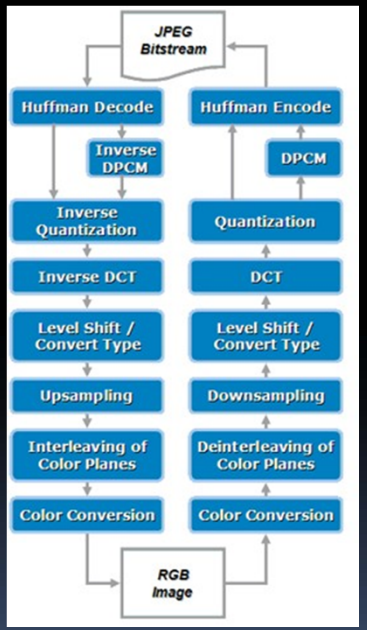
GPS

Mission exploration

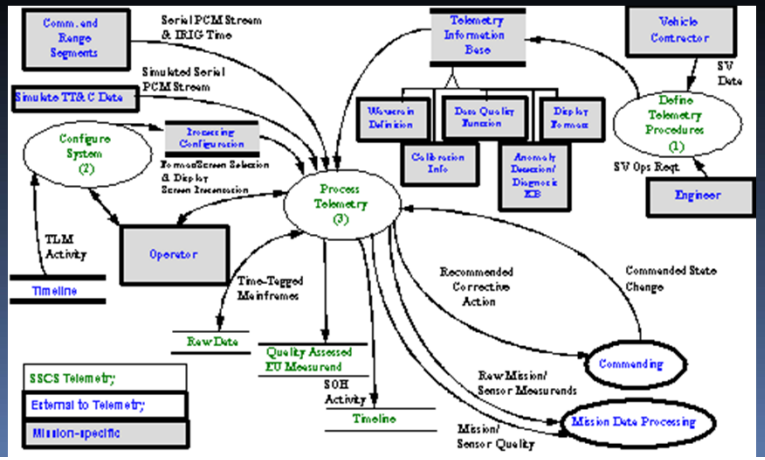


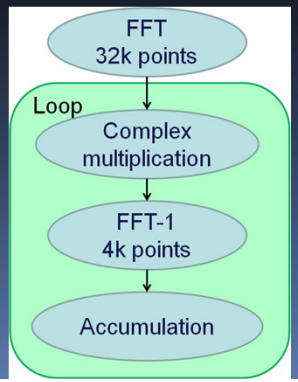
Satellite Payload

Motion JPEG



Telemetry

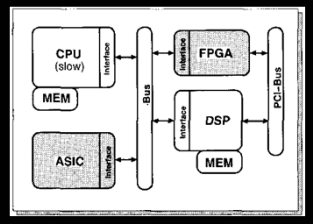


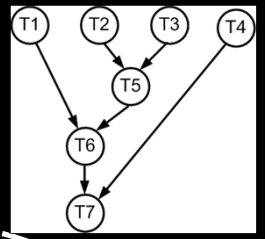


Acquisition algorithm for flexible GNSS

Mapping Problem (2)

Today's traditional workflow may take many iterations
And many hours per iteration

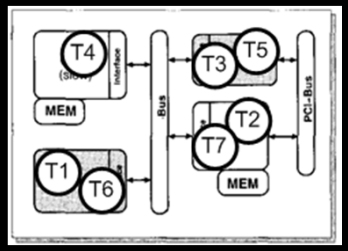




Architecture

Application

hours/days/weeks



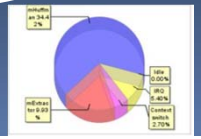
Mapping

hours/days

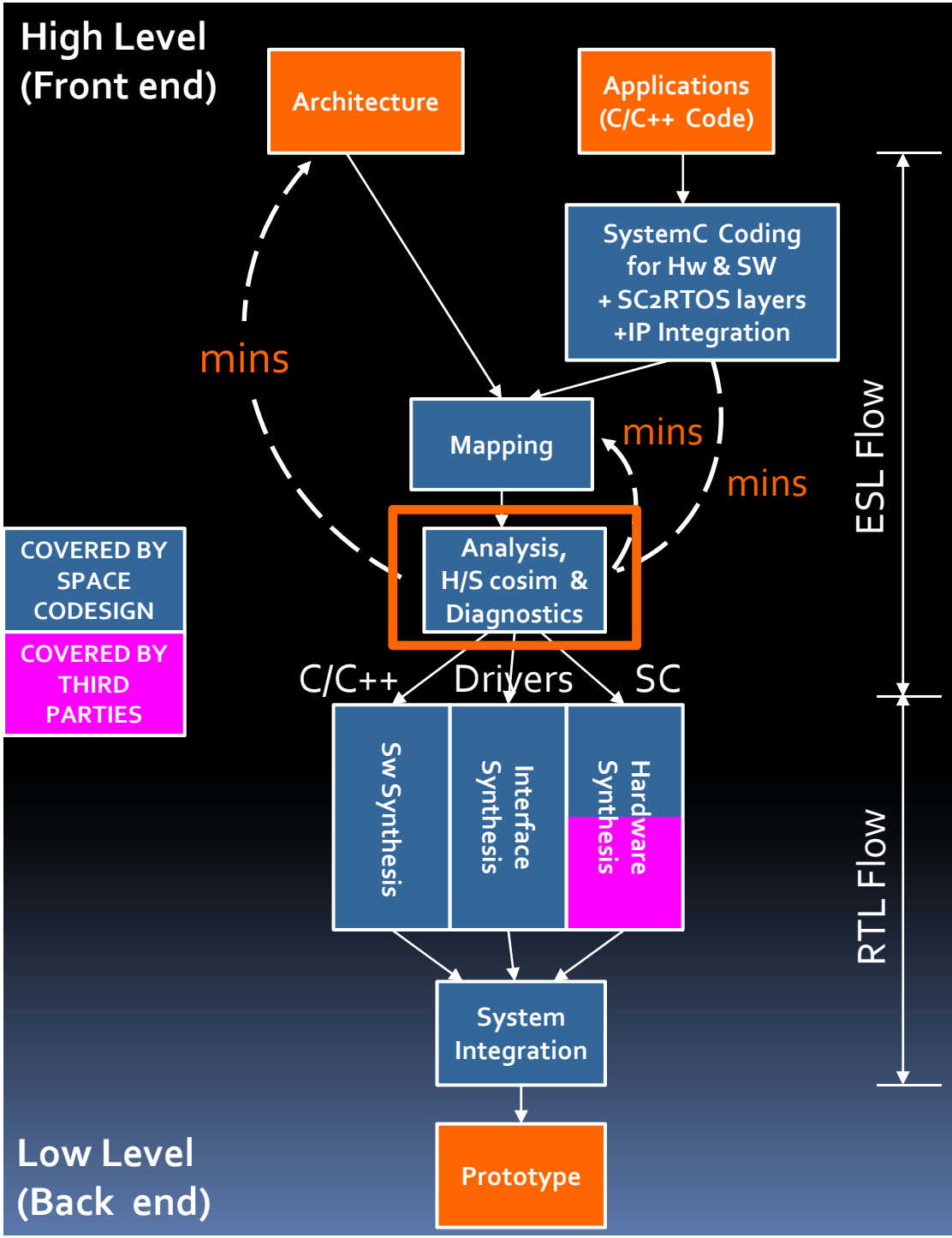
hours

Refinement

Analysis &
Diagnostic



Our Design Flow

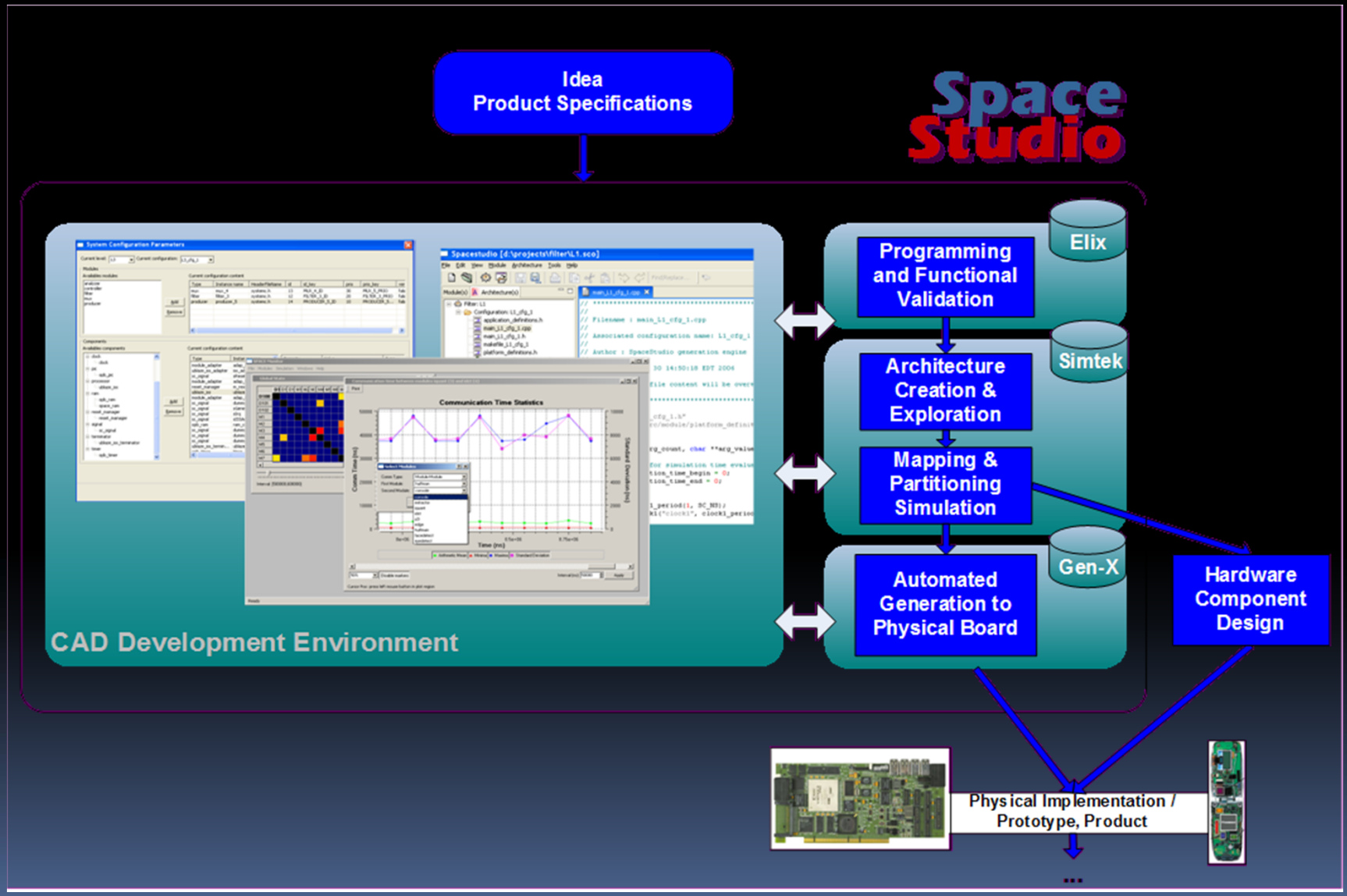


Extensive automation:

- Mapping iterations takes minutes no matter the kind of moves
- Fully transparent non-intrusive analysis

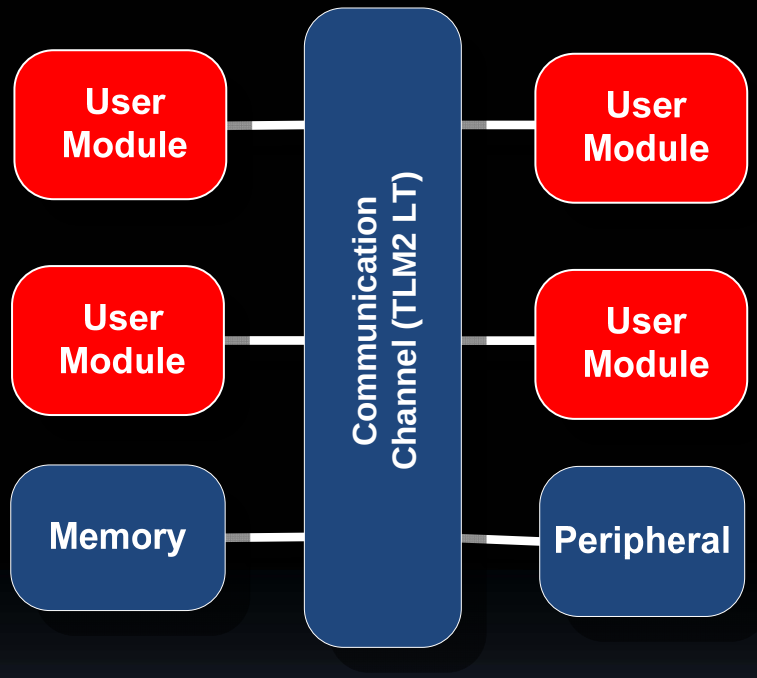
- No recoding from SystemC to VHDL is needed
- Firmware is automatically generated

Our Solution

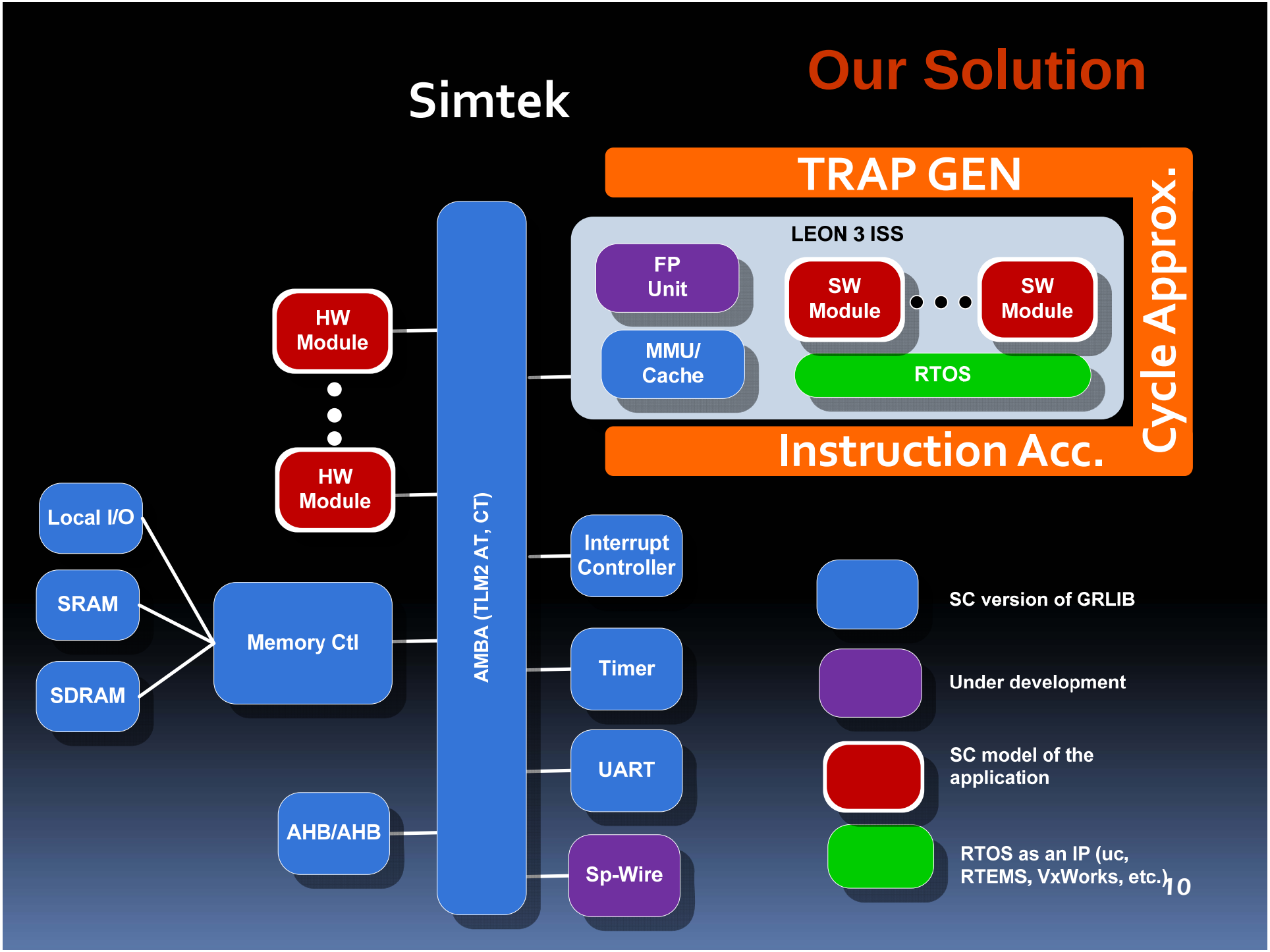


Elix : Functional Design and Validation

Our Solution

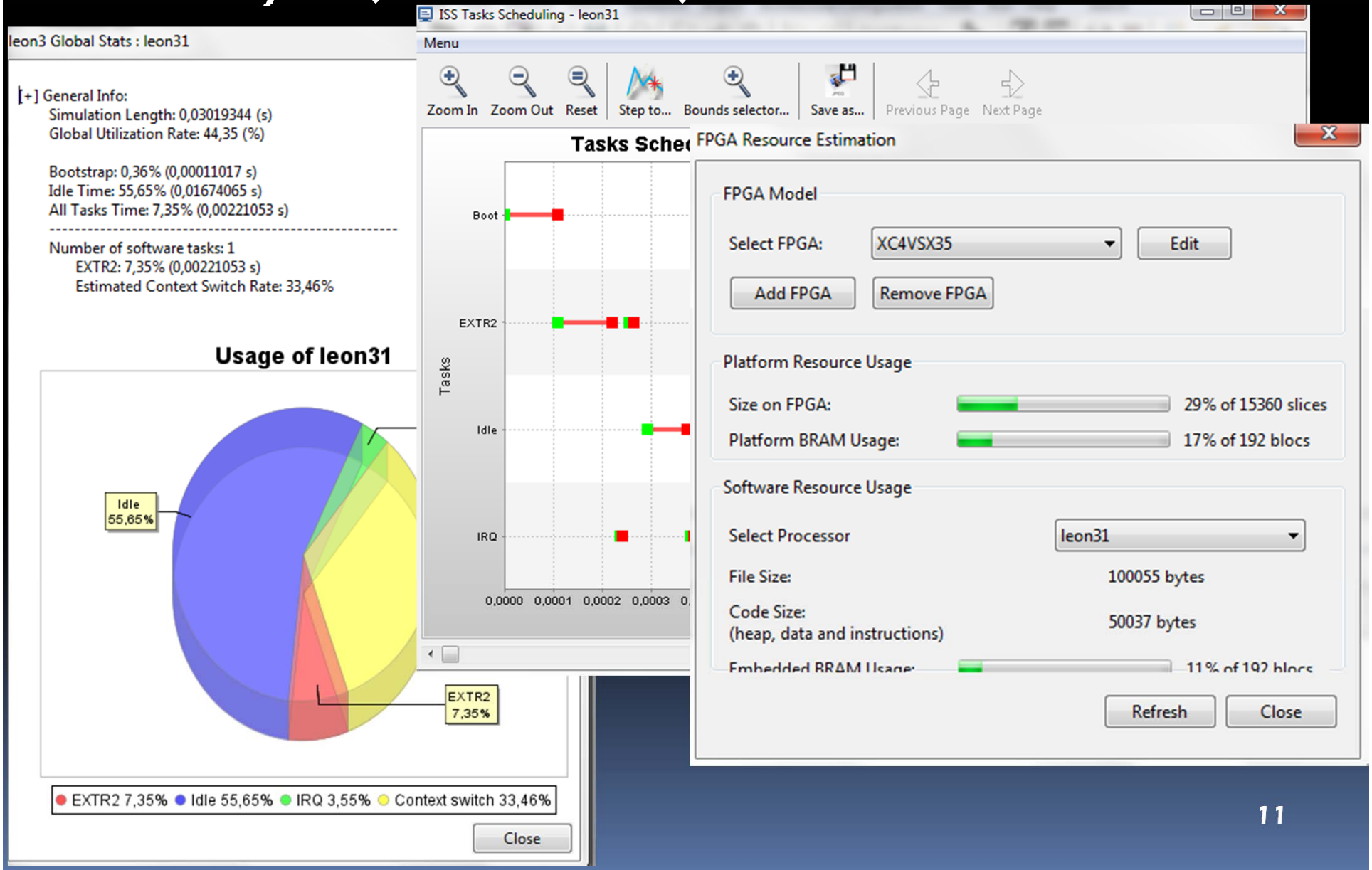


Our Solution

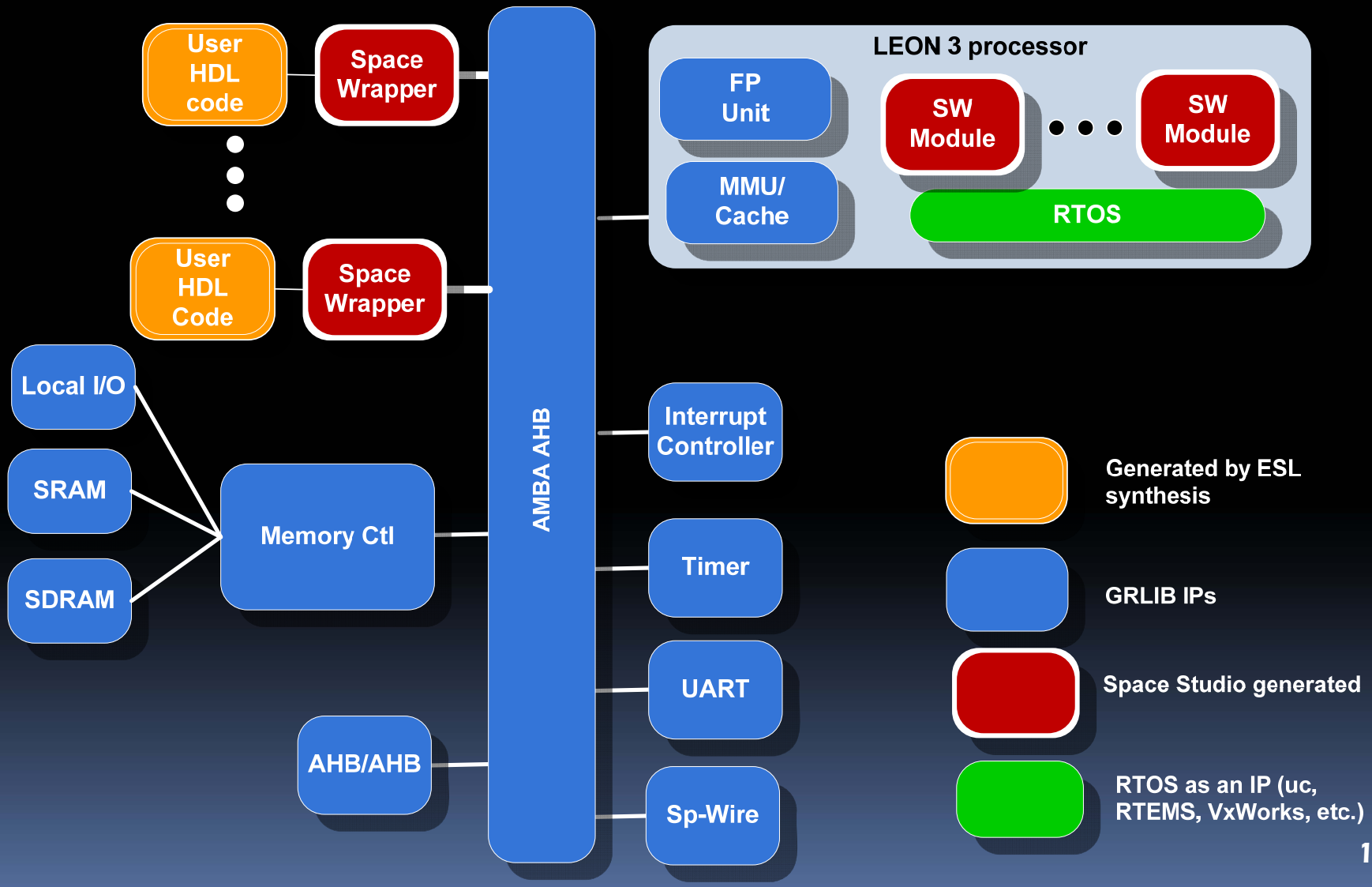


Also Performance Monitoring and Analysis (with Simtek)

Our Solution



Our Solution



Roadmap (products)

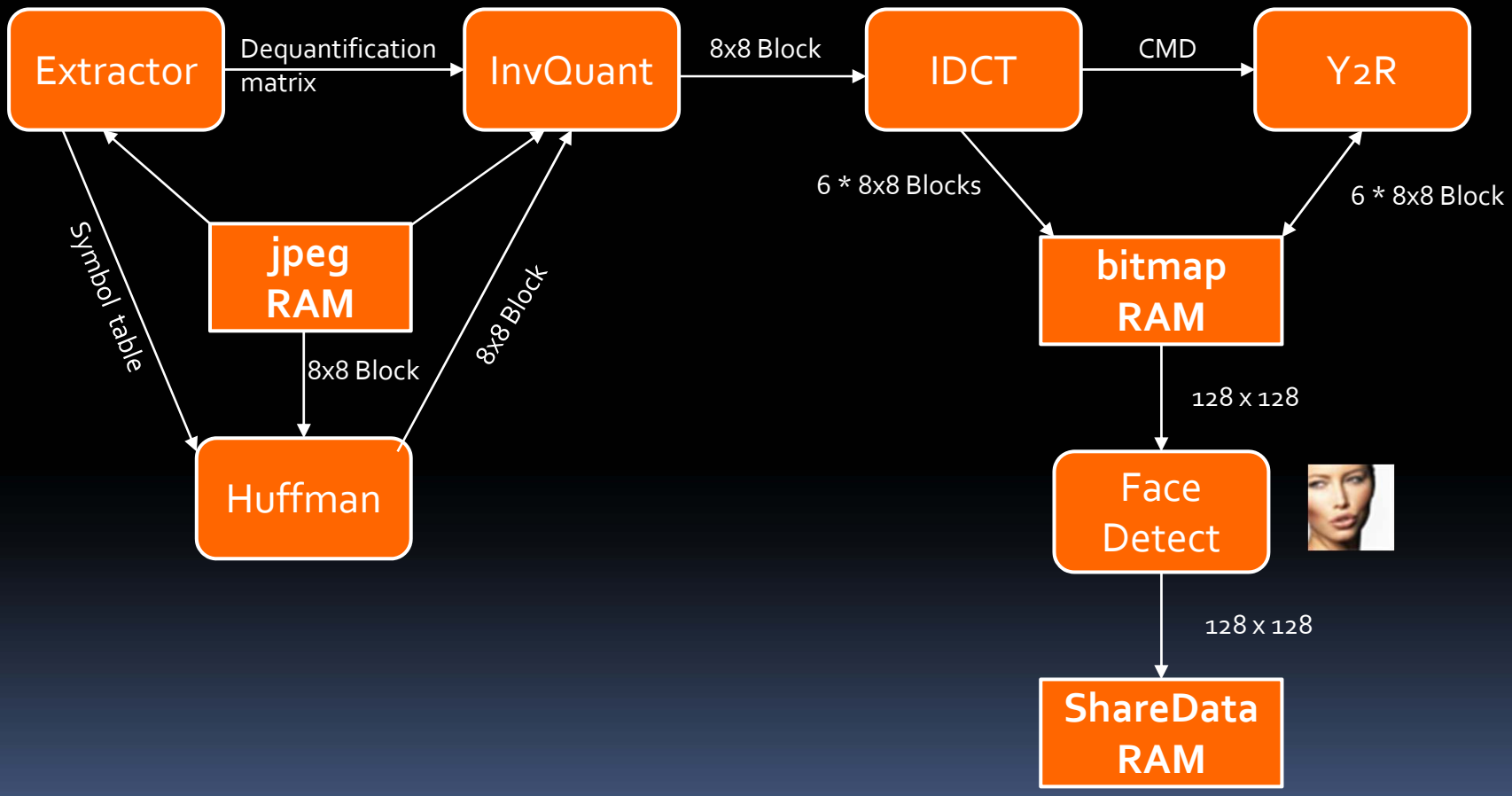
- During the next 3 years
- Priority according to market demands

Q2 2011	**SpaceStudio Aerospace** Aerospace version for FPGA – LEON processor + Larger IP Portfolio
Q4 2011	**SpaceStudio Multimedia** Xilinx Multimedia version for FPGA - ARM Cortex-A9 + Larger IP Portfolio

Aerospace – ESL for Actel Aerospace version for FPGA – Cortex M processor + Lower Power Strategies	**MultiM – ESL for Altera** Xilinx Multimedia version for FPGA - ARM Cortex-A9 + Low Power Strategies
Aerospace - ESL for ASIC Aerospace version for ASIC + Integrated Verification Flow + Leon 4	**MultiM - ESL** Multimedia version for ASIC + Integrated Verification Flow

JPEG Decoder

Demo



JPEG Decoder

Demo

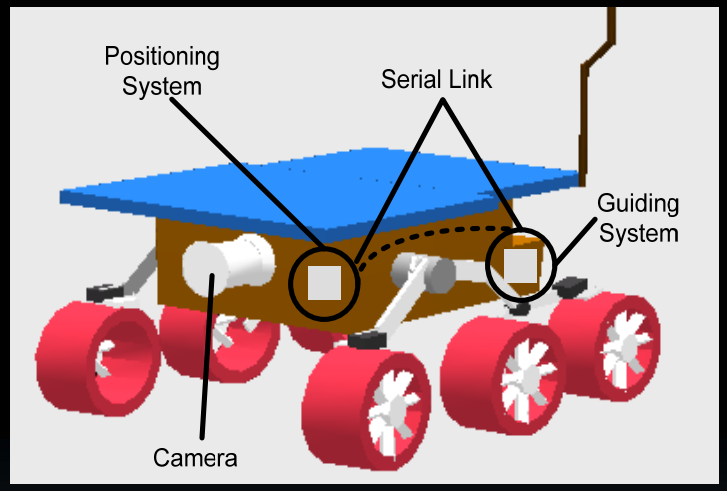
Architectural exploration examples

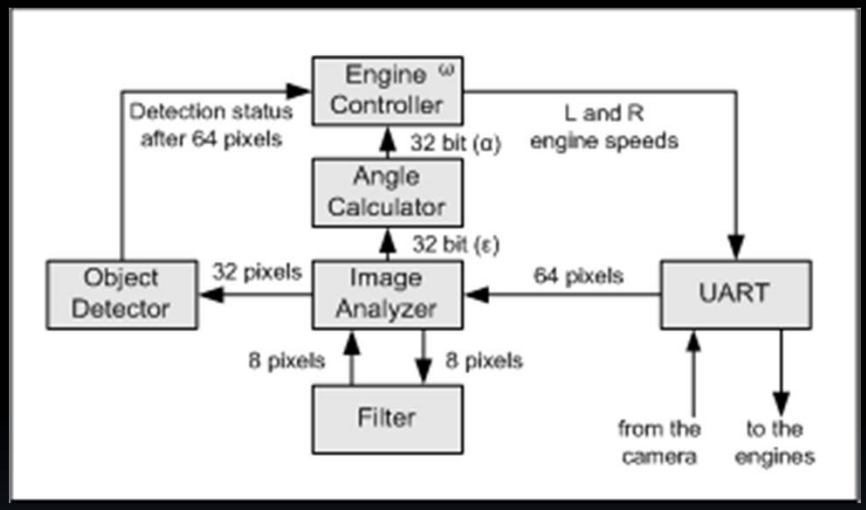
	# Processor		latency (s)	# images/sec		CPU %	AHB Bandwith %	
Config1	N/A		0,0022991	435		N/A		24
Leon 3								
Config2	1 Leon	with cache	0,0713448	15		100		8
		without cache	0,209142	5		100		20
Config3	2 Leon	with RTOS	0,0585551	18	P1:	99	AHB1:	7
					P2:	43	AHB2:	7
		without RTOS	0,0361186	28		100	AHB1:	7
						100	AHB2:	15
uBlaze								
Config2	1 uBlaze	BRAM	0,0938534	11		100		2

Rover

Demo

$$V = \tfrac{1}{2}(R+L) \bullet Vmax$$





TASTE Change Note: Objectives

- Demonstrate that TASTE's capabilities for complex systems development would greatly benefit from codesign technologies

- Show that such codesign technologies can be integrated into the TASTE toolset

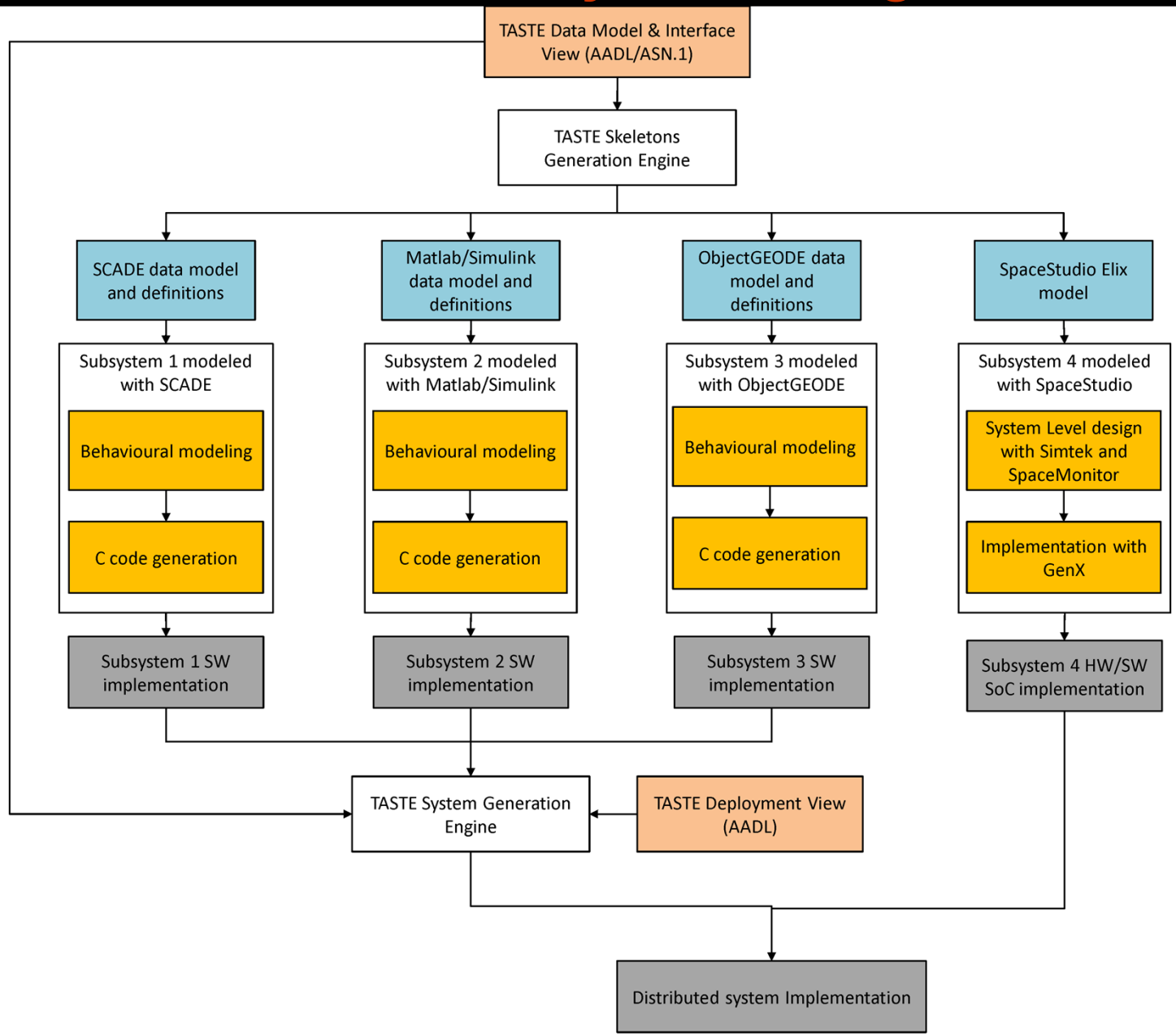
TASTE Change Note: Methodology

- Assessment of the TASTE and SpaceStudio tool suites
- Identification of complementarities between the TASTE and SpaceStudio
- Identification of integration possibilities
- Specification of a roadmap for integration
- Work performed jointly by Space Codesign and M3 Systems

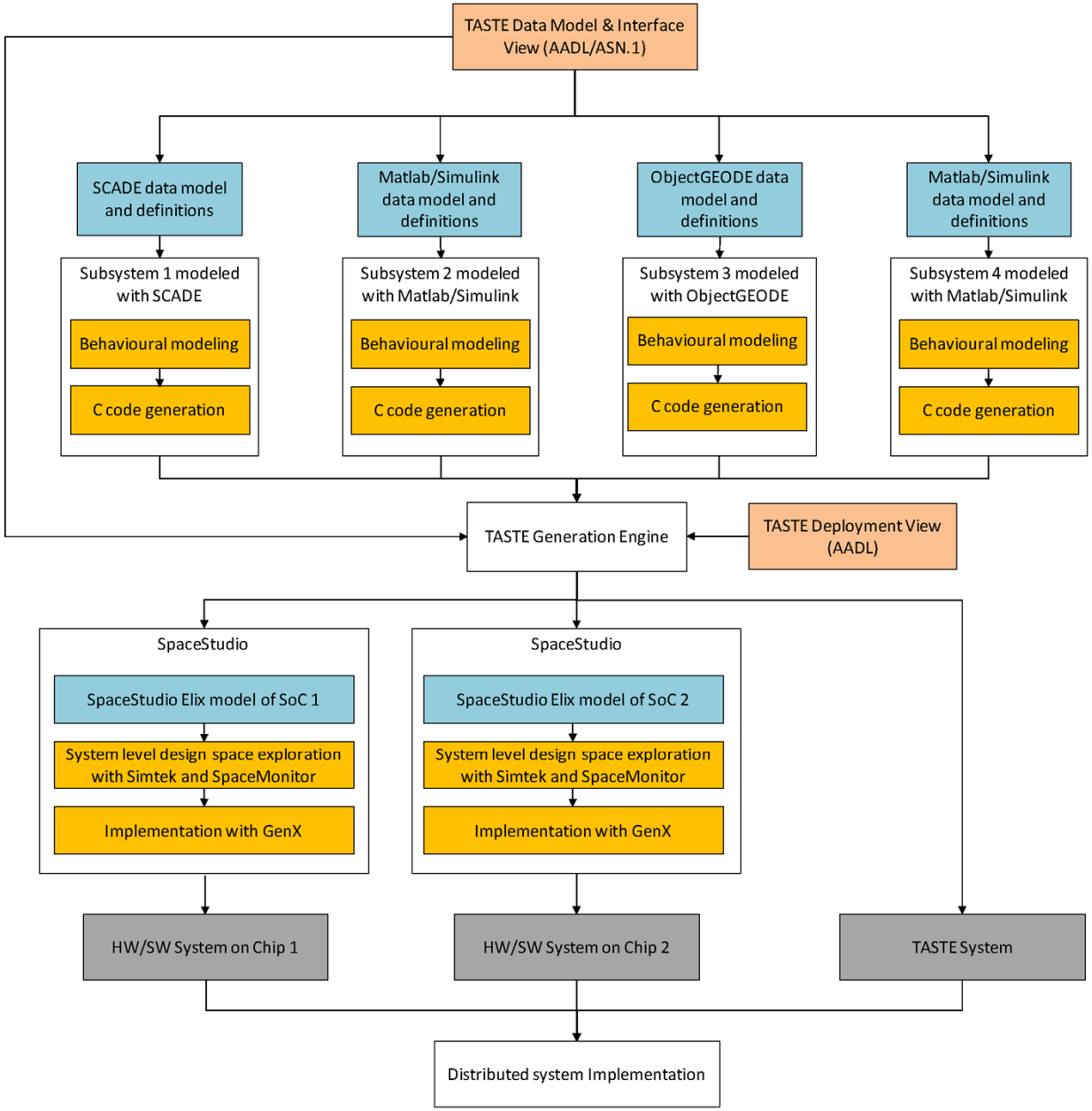
Complementarity of TASTE and SpaceStudio

Strong points of TASTE	Strong points of SpaceStudio
• Strong support for complex distributed multi-board systems • Graphical and explicit definition of component interfaces • Ease of implementation of individual system functions • Support for several languages for functional implementation • Strong support of aerospace technologies	• Strong support for complex systems-on-chip • Ease of defining and modifying the system-on-chip architecture • Ease of mapping functions on the architecture • Strong support for design space exploration & HW/SW co-design • Integrated performance monitoring and analytics

Side by side integration



Bottom-up Integration



Top-down Integration