



Extending TASTE through integration with Space Studio

Guy Bois, Laurent Moss - Space Codesign Systems

Marc Pollina, Yan Leclerc - M3 Systems

www.spacecodesign.com



Outline

- 1) **Overview of the Space Studio platform for hardware/software (Hw/Sw) codesign**
- 2) **Demo**
- 3) **Propositions for adding Hw/Sw capabilities to TASTE**



Problem and Market Need



- **Electronics design is dealing with larger, more complex Hardware and Software that must work well together**
- **Rapid market changes impact product direction and strategy, changing requirements that drive design:**
 - e.g., Tablets versus Netbooks (iPad)
 - e.g., Smart versus Feature phone (iPhone)
- **Decisions needed rapidly**
- **TI: Silicon Respin Cost – up to \$3 Million (Synopsys)**

Solution Product & Technology

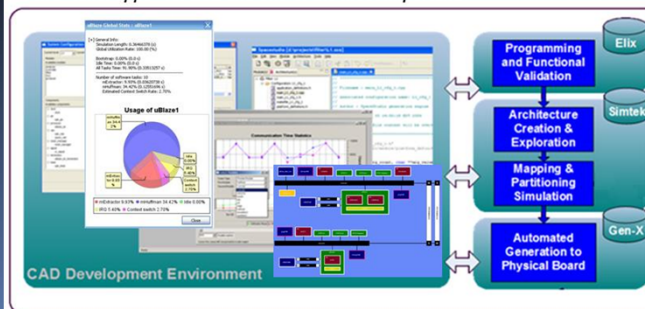
- Rapid decisions at front end of design process



- Electronic System Level (ESL)
- Create Large Complex Systems at Higher Level removes complexity of details ...
- Co-design of Software AND Hardware – together (Software content is increasing)

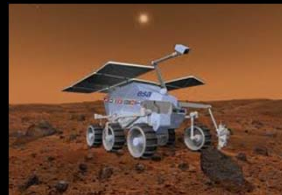
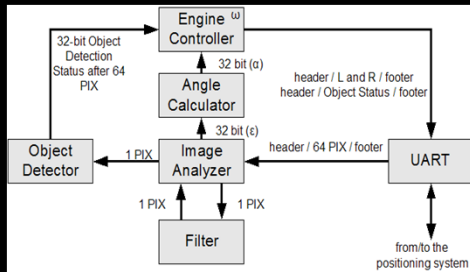
According to Gary Smith EDA, Space Studio tool suite can be classified as part of the "architect's workbench" category, one of two "killer apps" for ESL and one of the most important.

Space Studio

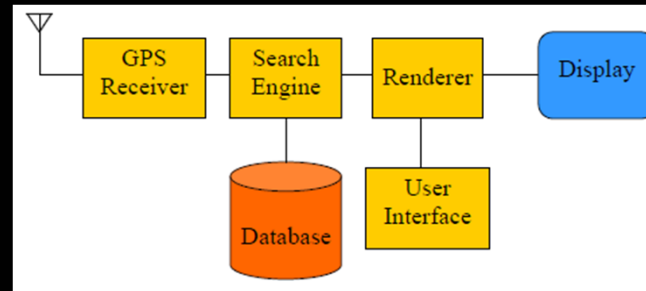


Mapping Problem (1)

Vision based navigation



Mission exploration

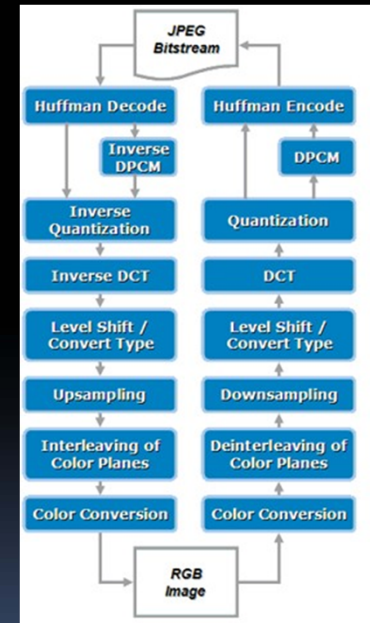


GPS



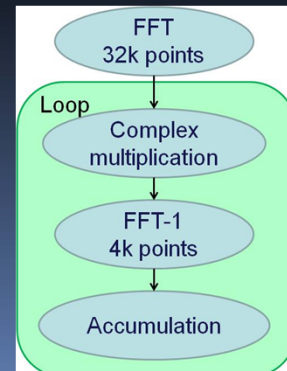
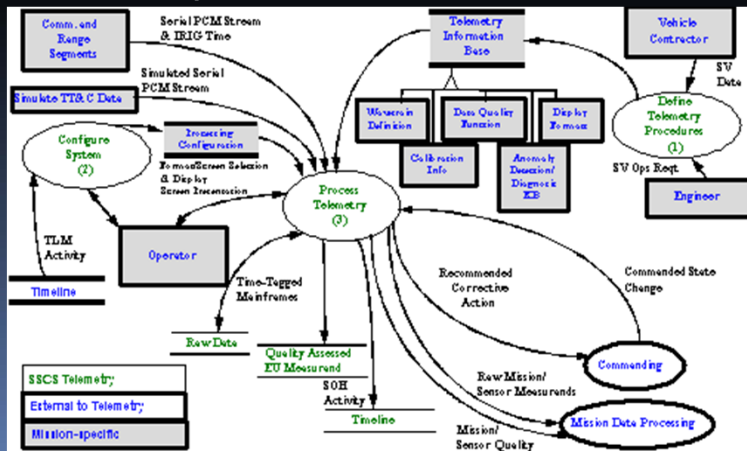
Satellite Payload

Motion JPEG



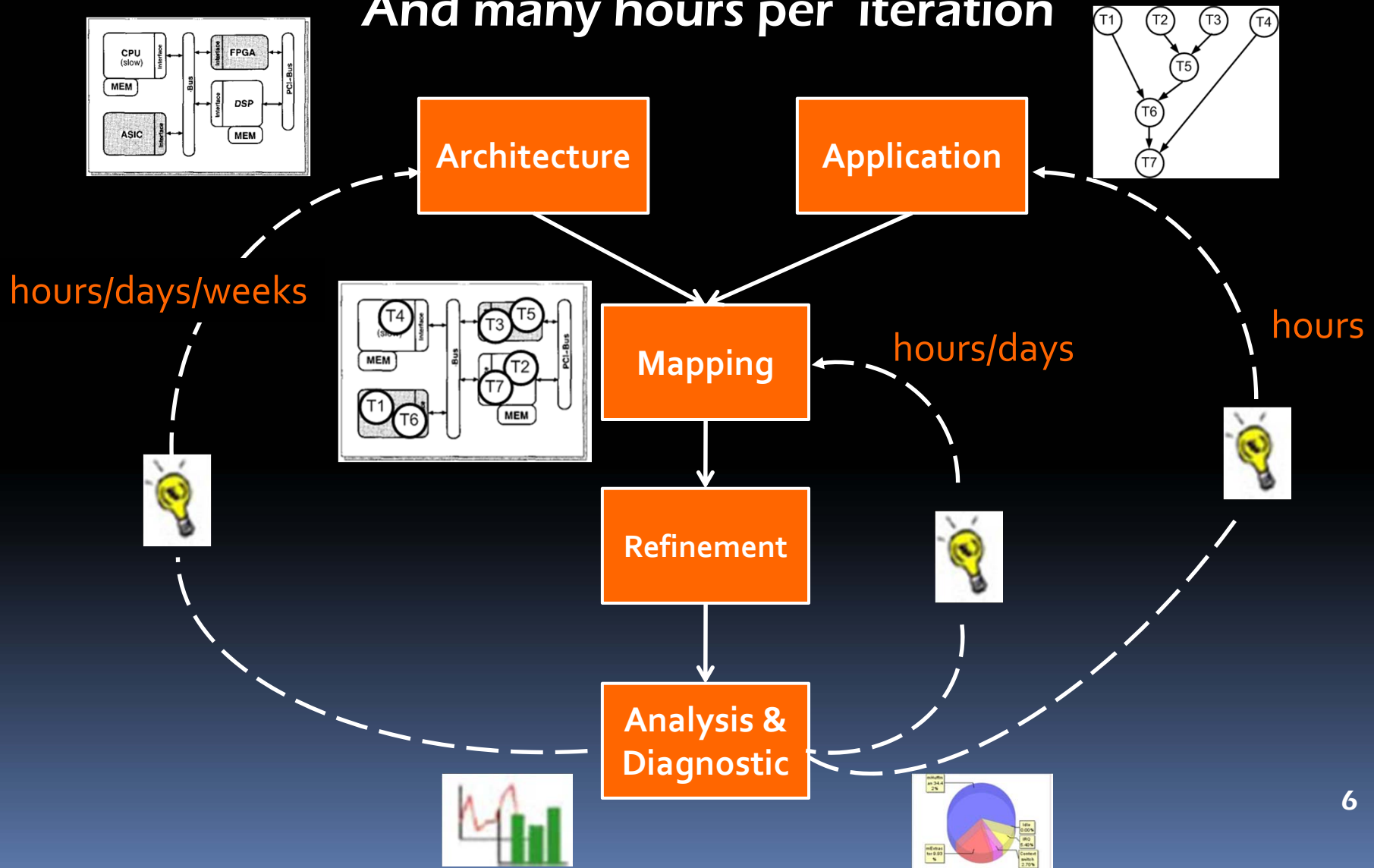
Acquisition algorithm for flexible GNSS

Telemetry

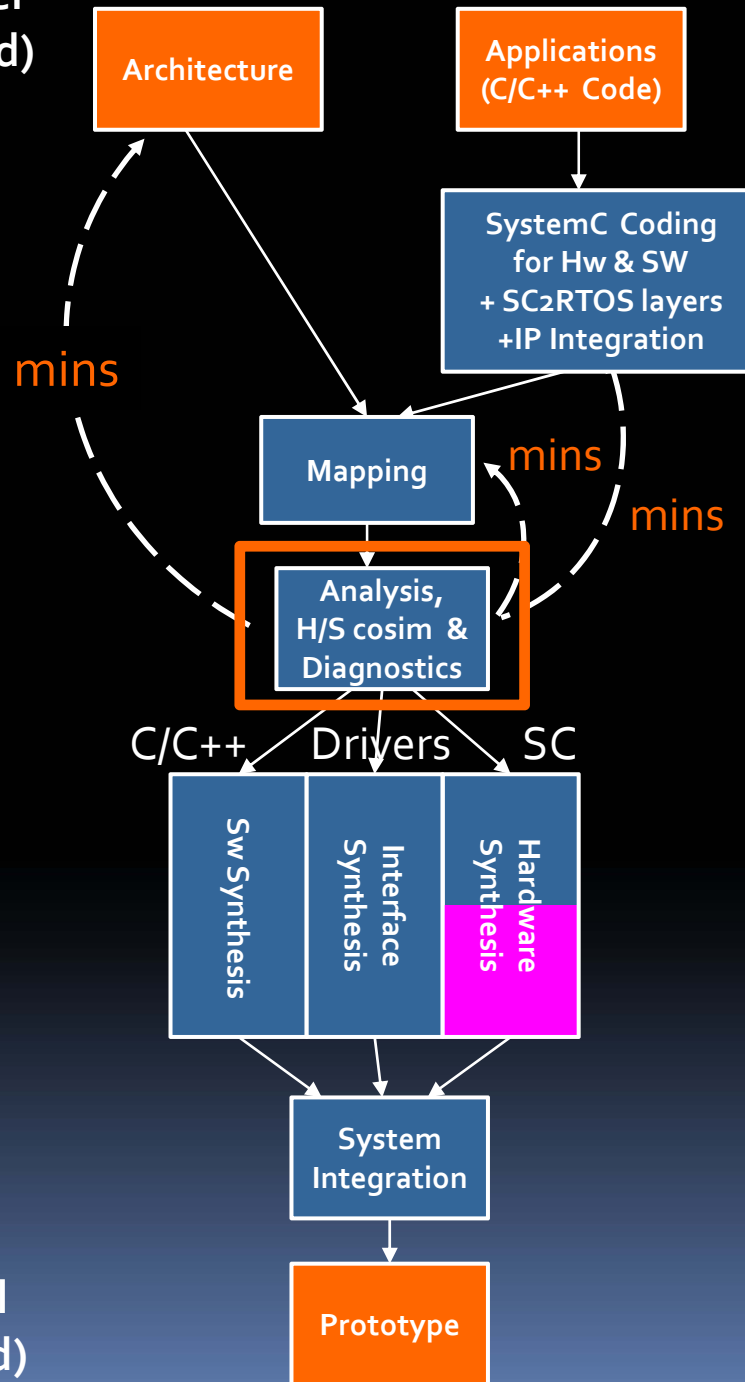


Mapping Problem (2)

Today's traditional workflow may take many iterations
And many hours per iteration



High Level
(Front end)



COVERED BY
SPACE
CODESIGN

COVERED BY
THIRD
PARTIES

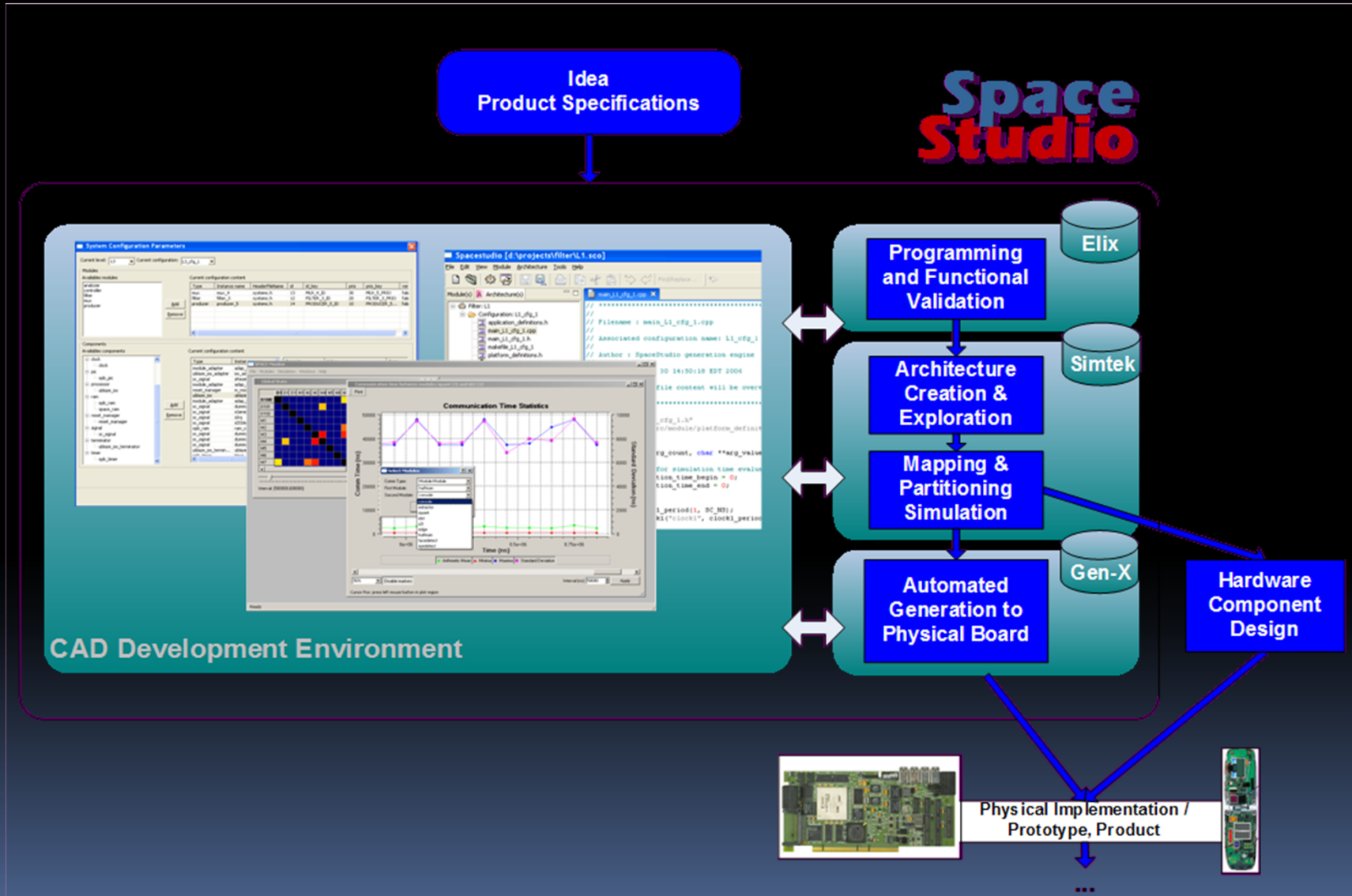
Low Level
(Back end)

Our Design Flow

Extensive automation:

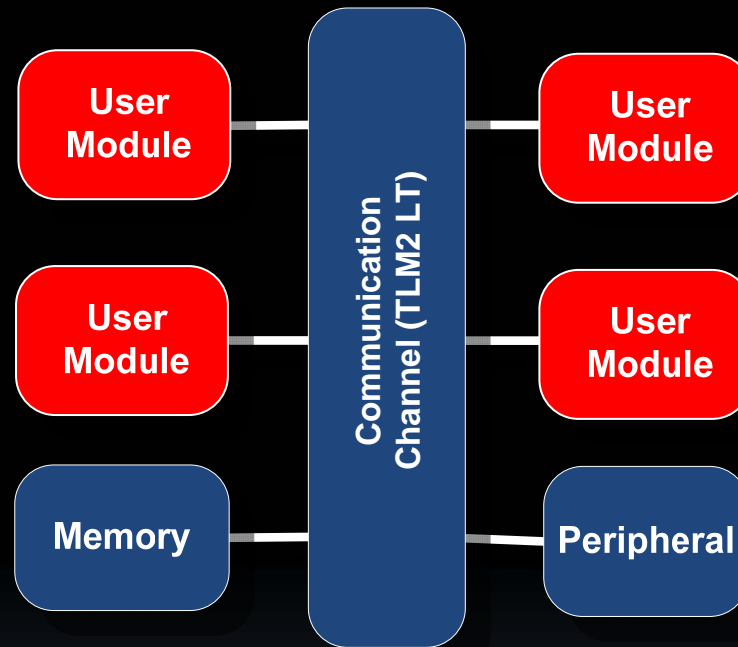
- Mapping iterations takes minutes no matter the kind of moves
- Fully transparent non-intrusive analysis
- No recoding from SystemC to VHDL is needed
- Firmware is automatically generated

Our Solution



Elix : Functional Design and Validation

Our Solution



Simtek

Our Solution

TRAP GEN

LEON 3 ISS

FP Unit

SW Module

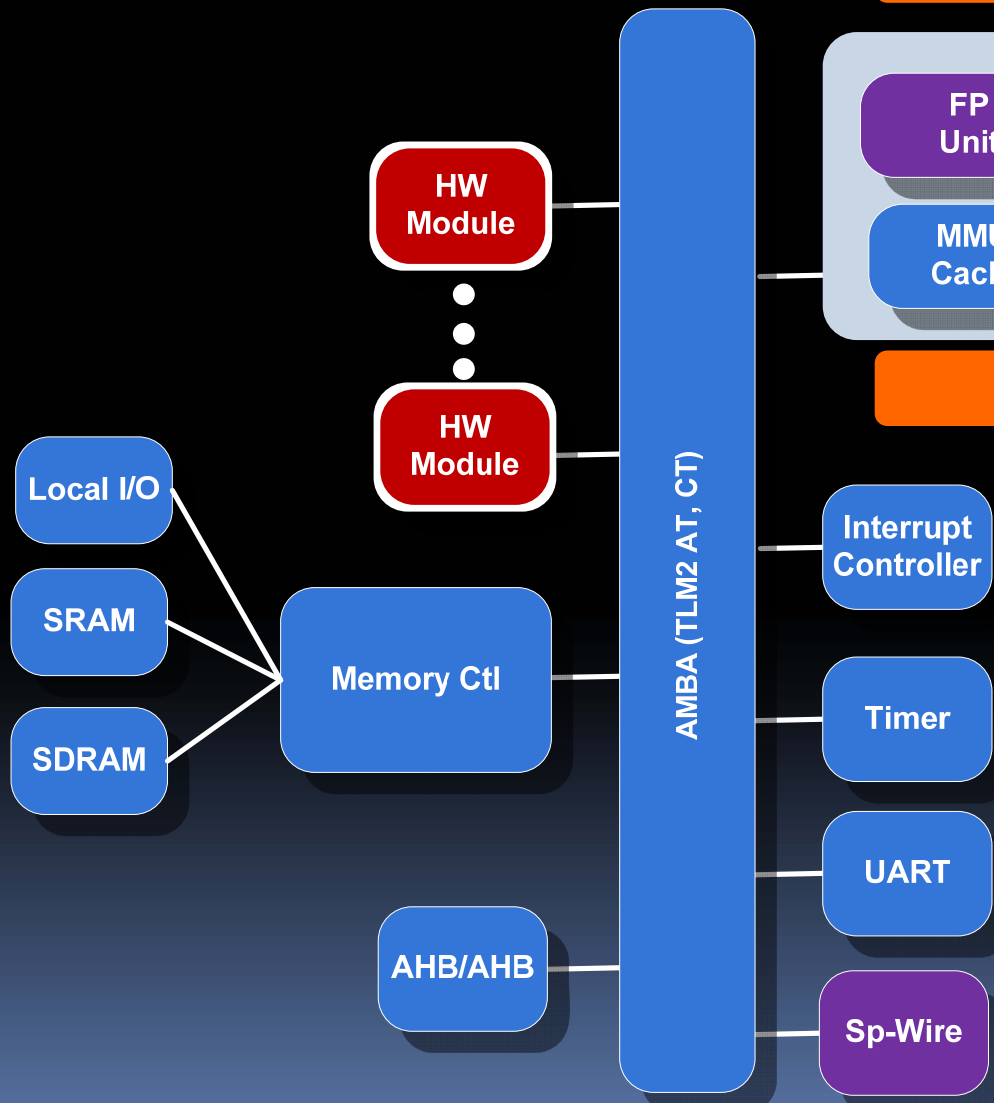
SW Module





MMU/ Cache

RTOS

Instruction Acc.

Cycle Approx.



-  SC version of GRLIB
-  Under development
-  SC model of the application
-  RTOS as an IP (uc, RTEMS, VxWorks, etc.)

Also Performance Monitoring and Analysis (with Simtek)

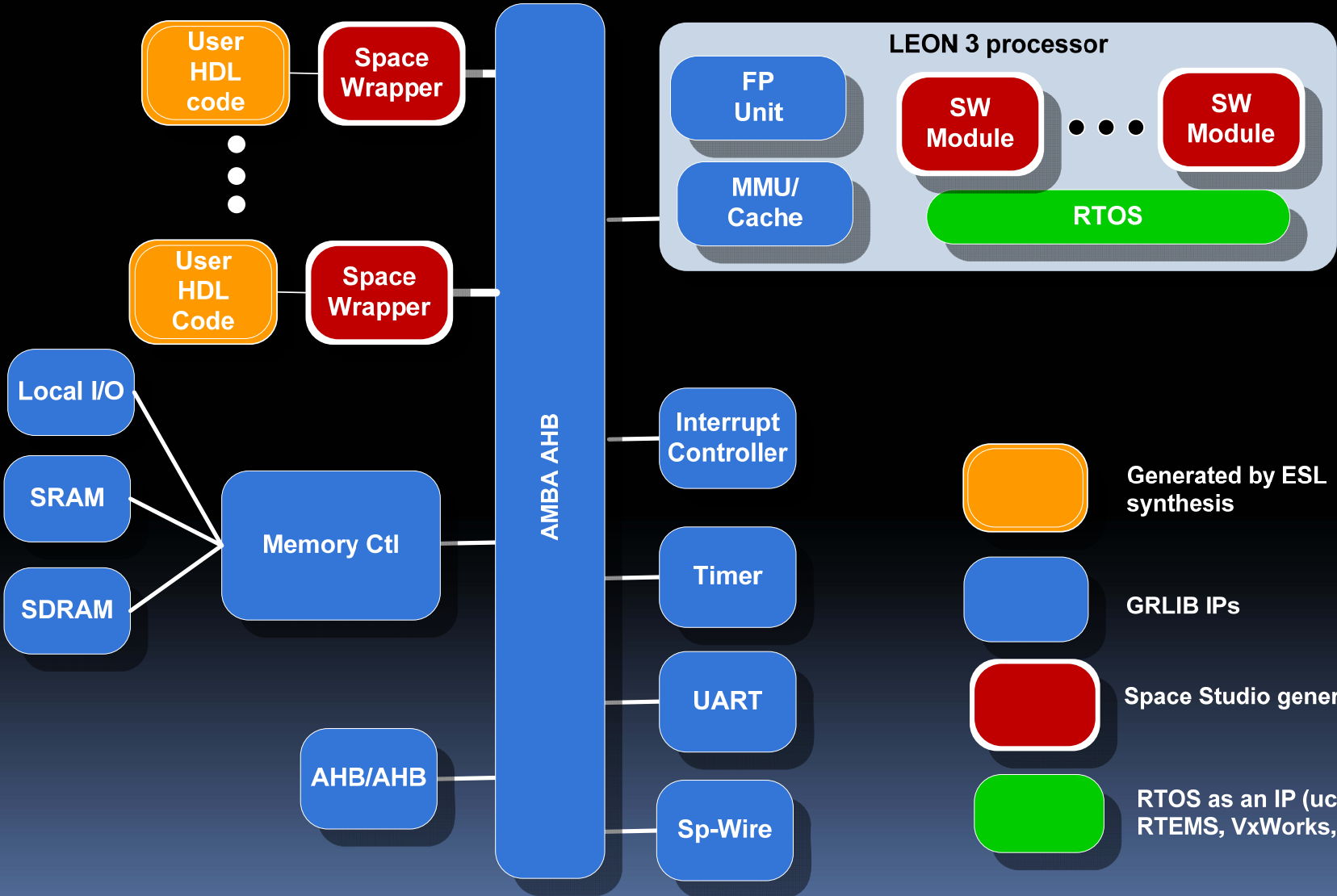
Our Solution

The screenshot displays the ISS Tasks Scheduling - leon31 interface, which is divided into several key sections:

- Global Stats (leon31):** Provides simulation parameters such as Simulation Length (0,03019344 s), Global Utilization Rate (44,35%), Bootstrap (0,36%), Idle Time (55,65%), and All Tasks Time (7,35%). It also lists the number of software tasks (1) and estimated context switch rate (33,46%).
- Usage of leon31:** A 3D pie chart showing the distribution of system states: Idle (55,65%), Context switch (33,46%), EXTR2 (7,35%), and IRQ (3,55%).
- Tasks Scheduler:** A Gantt-style chart showing task execution timelines for Boot, EXTR2, Idle, and IRQ over a time period from 0,0000 to 0,0003 s.
- FPGA Resource Estimation:** A detailed configuration panel for the Xilinx XC4VSX35 FPGA, including:
 - FPGA Model:** Select FPGA: XC4VSX35.
 - Platform Resource Usage:** Size on FPGA: 29% of 15360 slices; Platform BRAM Usage: 17% of 192 blocs.
 - Software Resource Usage:** Select Processor: leon31; File Size: 100055 bytes; Code Size: 50037 bytes; Embedded BRAM Usage: 11% of 192 blocs.

Our Solution

GenX



Roadmap (products)

- **During the next 3 years**
- **Priority according to market demands**

Q2 2011	SpaceStudio Aerospace Aerospace version for FPGA – LEON processor + Larger IP Portfolio
Q4 2011	SpaceStudio Multimedia Xilinx Multimedia version for FPGA - ARM Cortex-A9 + Larger IP Portfolio

Aerospace – ESL for Actel
Aerospace version for FPGA – Cortex M processor
+ Lower Power Strategies

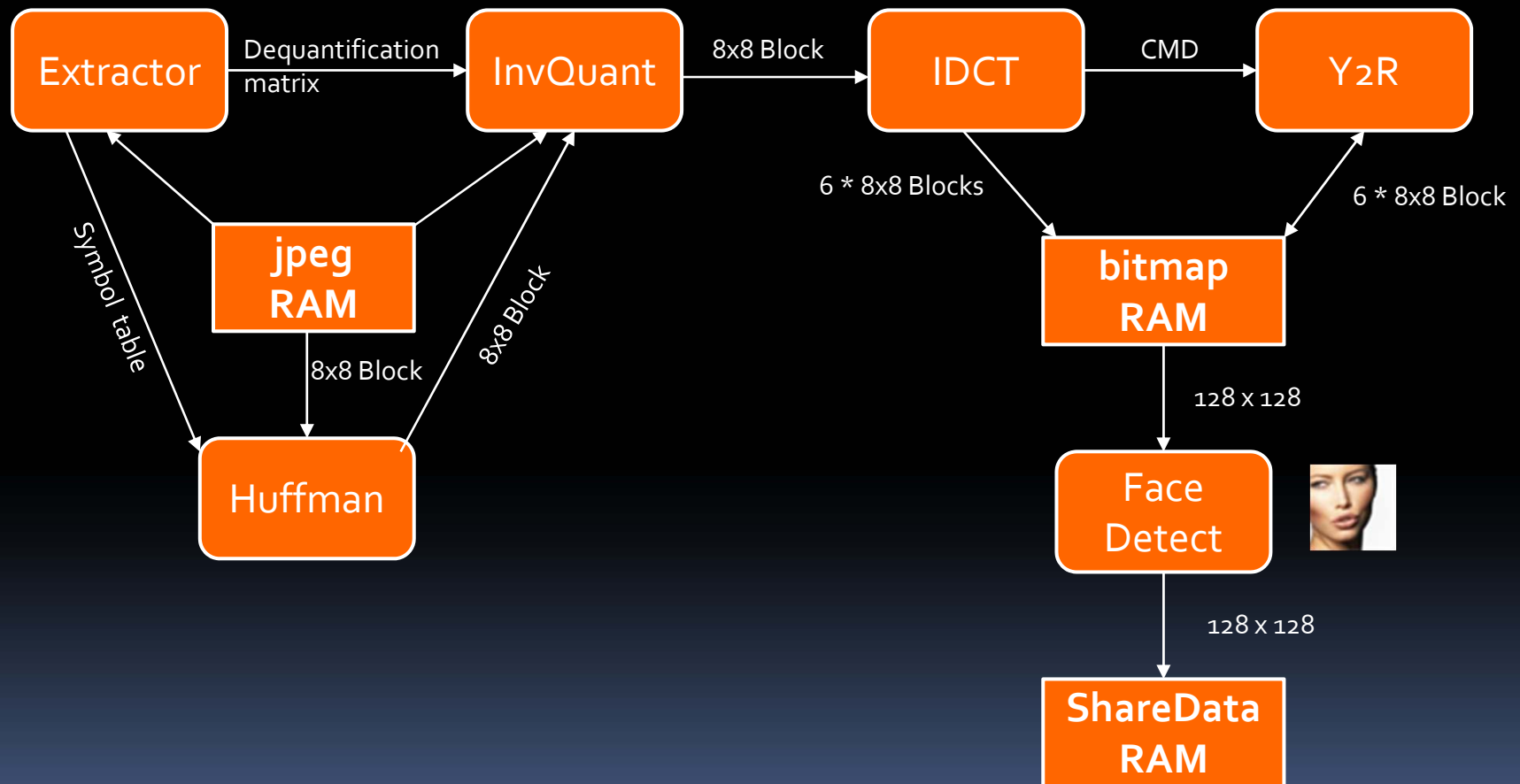
Aerospace - ESL for ASIC
Aerospace version for ASIC
+ Integrated Verification Flow
+ Leon 4

MultiM – ESL for Altera
Xilinx Multimedia version for FPGA - ARM Cortex-A9
+ Low Power Strategies

MultiM - ESL
Multimedia version for ASIC
+ Integrated Verification Flow

JPEG Decoder

Demo



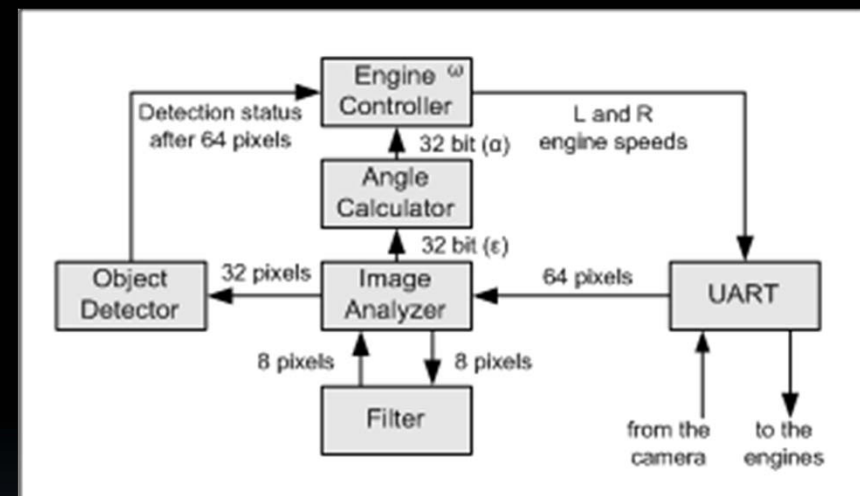
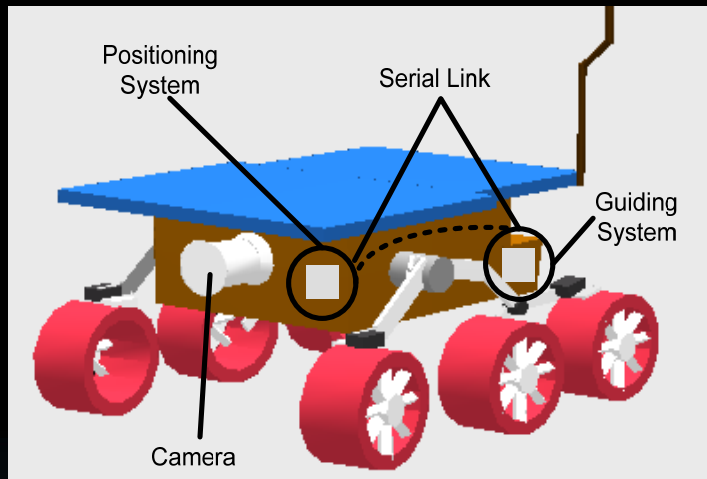
Architectural exploration examples

	# Processor		latency (s)	# images/sec	CPU %	AHB Bandwith %
Config1	N/A		0,0022991	435	N/A	24
Leon 3						
Config2	1 Leon	with cache	0,0713448	15	100	8
		without cache	0,209142	5	100	20
Config3	2 Leon	with RTOS	0,0585551	18	P1: 99	AHB1: 7
					P2: 43	AHB2: 7
		without RTOS	0,0361186	28	100	AHB1: 7
					100	AHB2: 15
uBlaze						
Config2	1 uBlaze	BRAM	0,0938534	11	100	2

Rover

Demo

$$V = \frac{1}{2}(R+L) \cdot V_{max}$$



TASTE Change Note: Objectives

- **Demonstrate that TASTE's capabilities for complex systems development would greatly benefit from codesign technologies**
- **Show that such codesign technologies can be integrated into the TASTE toolset**

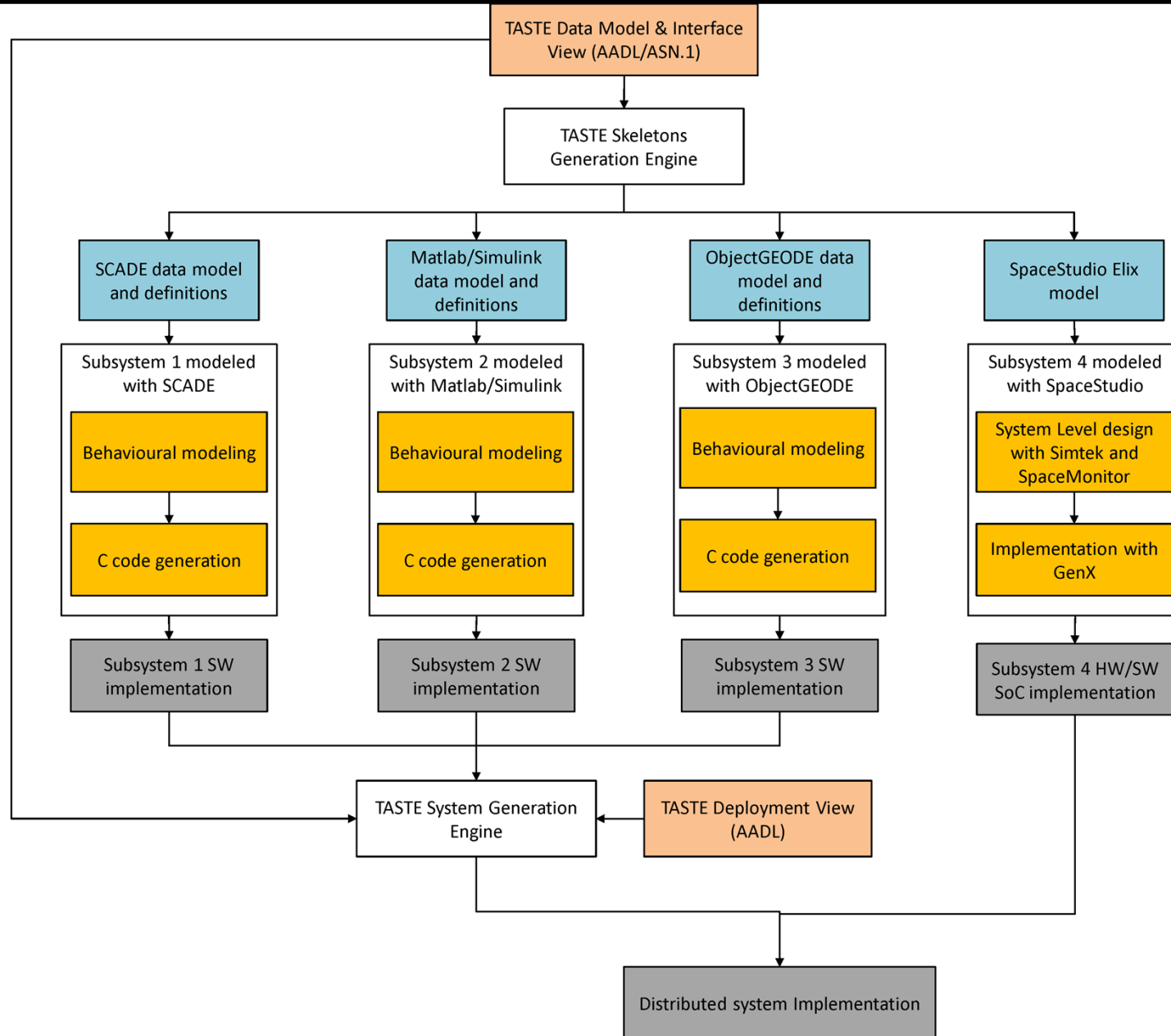
TASTE Change Note: Methodology

- **Assessment of the TASTE and SpaceStudio tool suites**
- **Identification of complementarities between the TASTE and SpaceStudio**
- **Identification of integration possibilities**
- **Specification of a roadmap for integration**
- **Work performed jointly by Space Codesign and M3 Systems**

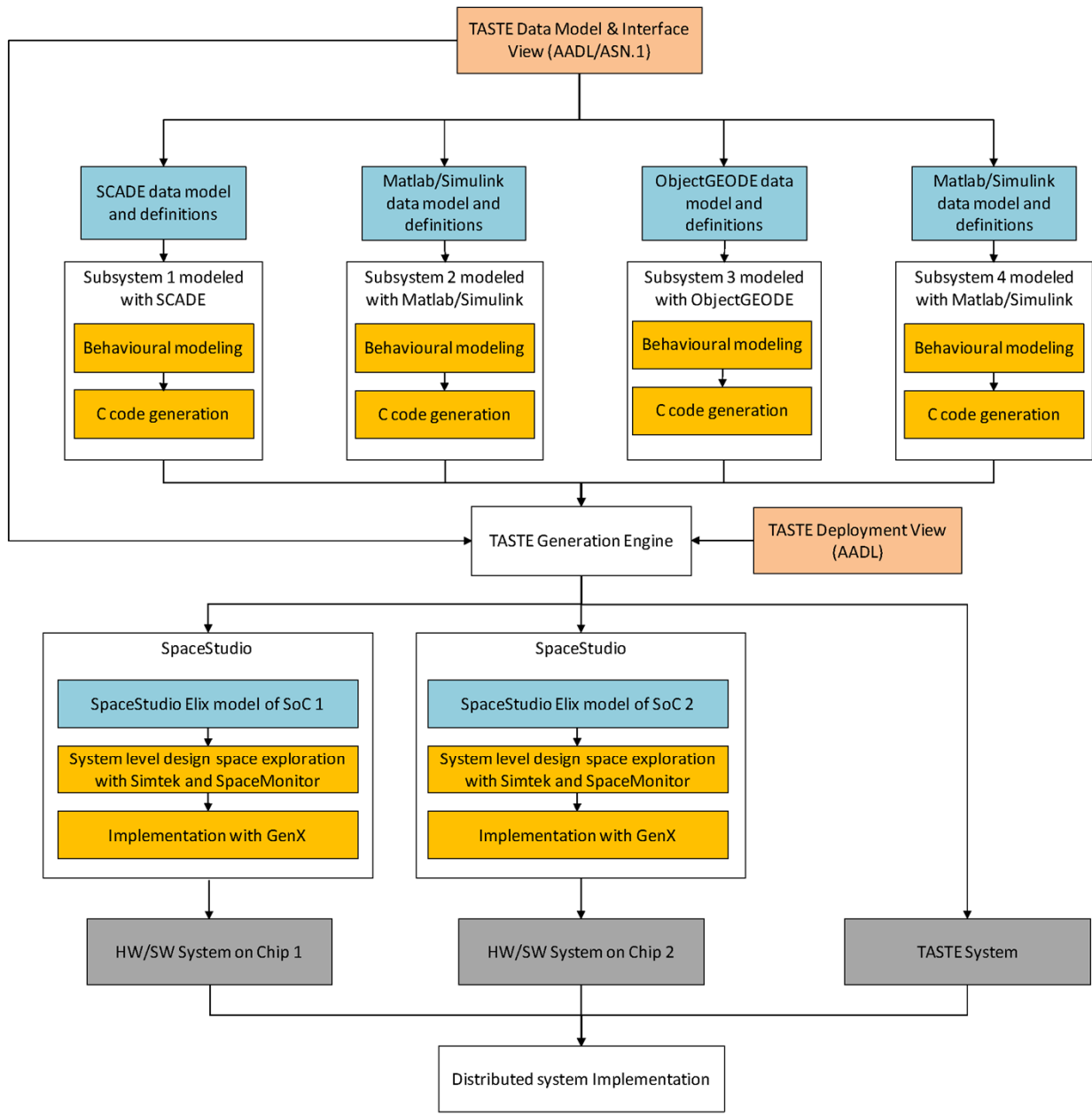
Complementarity of TASTE and SpaceStudio

Strong points of TASTE	Strong points of SpaceStudio
<ul style="list-style-type: none">• Strong support for complex distributed multi-board systems• Graphical and explicit definition of component interfaces• Ease of implementation of individual system functions• Support for several languages for functional implementation• Strong support of aerospace technologies	<ul style="list-style-type: none">• Strong support for complex systems-on-chip• Ease of defining and modifying the system-on-chip architecture• Ease of mapping functions on the architecture• Strong support for design space exploration & HW/SW co-design• Integrated performance monitoring and analytics

Side by side integration



Bottom-up Integration



Top-down Integration

