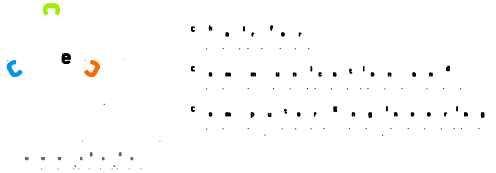


Hardware Modeling using Virtual Platforms

The ESA HW/SW Co-Verification SoC Validation Platform

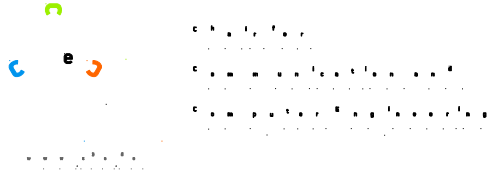
-

T. Schuster, R. Meyer

19-Sep-11

Outline

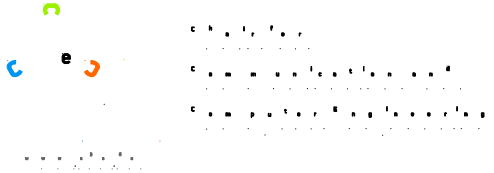
SoCRocket



Introduction to Virtual Platforms and TLM
The SoCRocket SystemC Modeling Library
Models Verification

Outline

SoCRocket

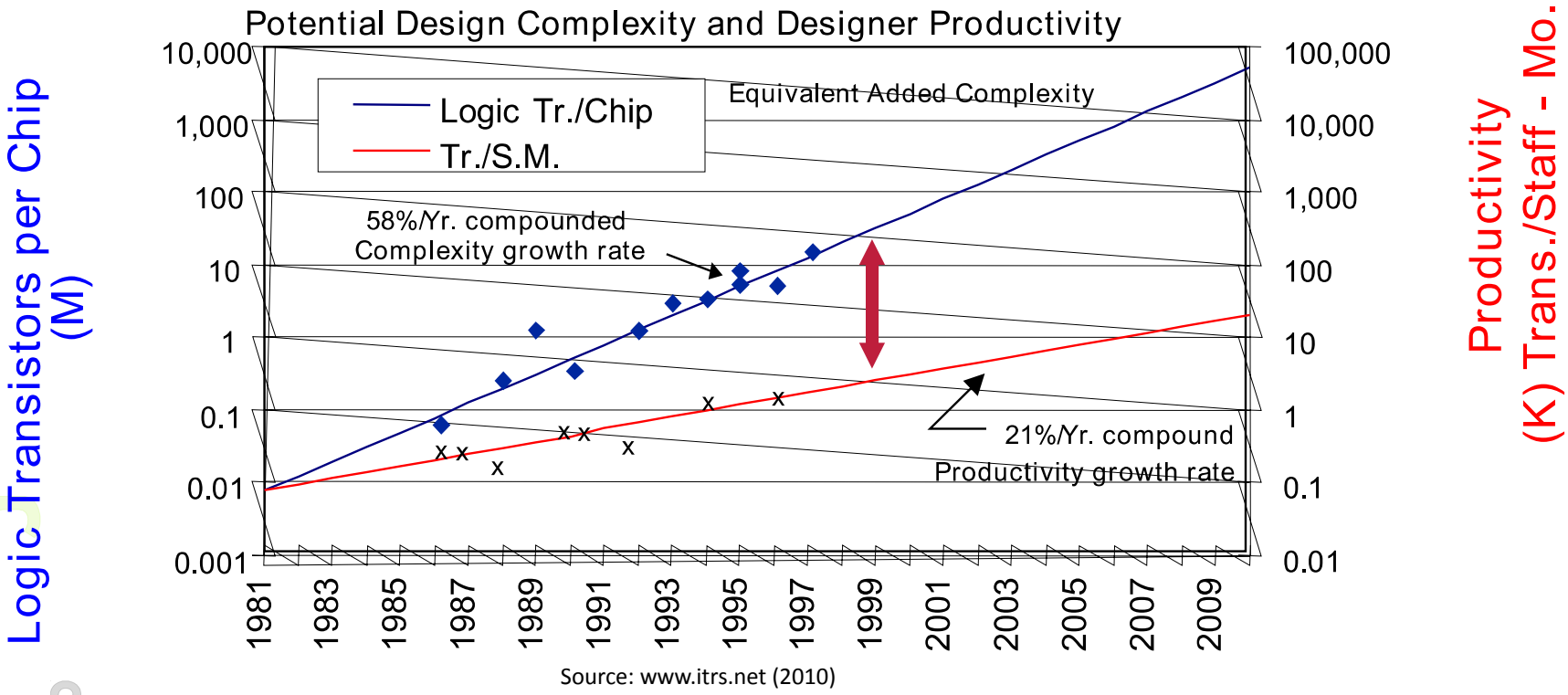


Introduction to Virtual Platforms and TLM

The SocRocket VP

Verification

Design & Productivity Gap



Source: www.itrs.net (2010)

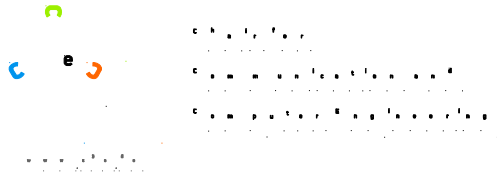
How to manage the raising complexity?

Advantages of Virtual Platforms

Virtual Platforms are abstract hardware models that are simulated by software:

- Availability
  - Software development can start early
- Productivity
  - Can be easily duplicated and packaged
- Accessibility
  - Software is easy to observe and control
- Consistency
  - Gradual HW refinement / keep your tests

SystemC / TLM 2.0



Use Cases

- Software-Development
- Software-Performance
- Architecture-Analysis
- Hardware-Verification

Coding Styles

- **Loosely-Timed (LT)**
  blocking, function calls, single-phased
- **Approximately-Timed (AT)**
  non-blocking, scheduled, multi-phased

Mechanisms

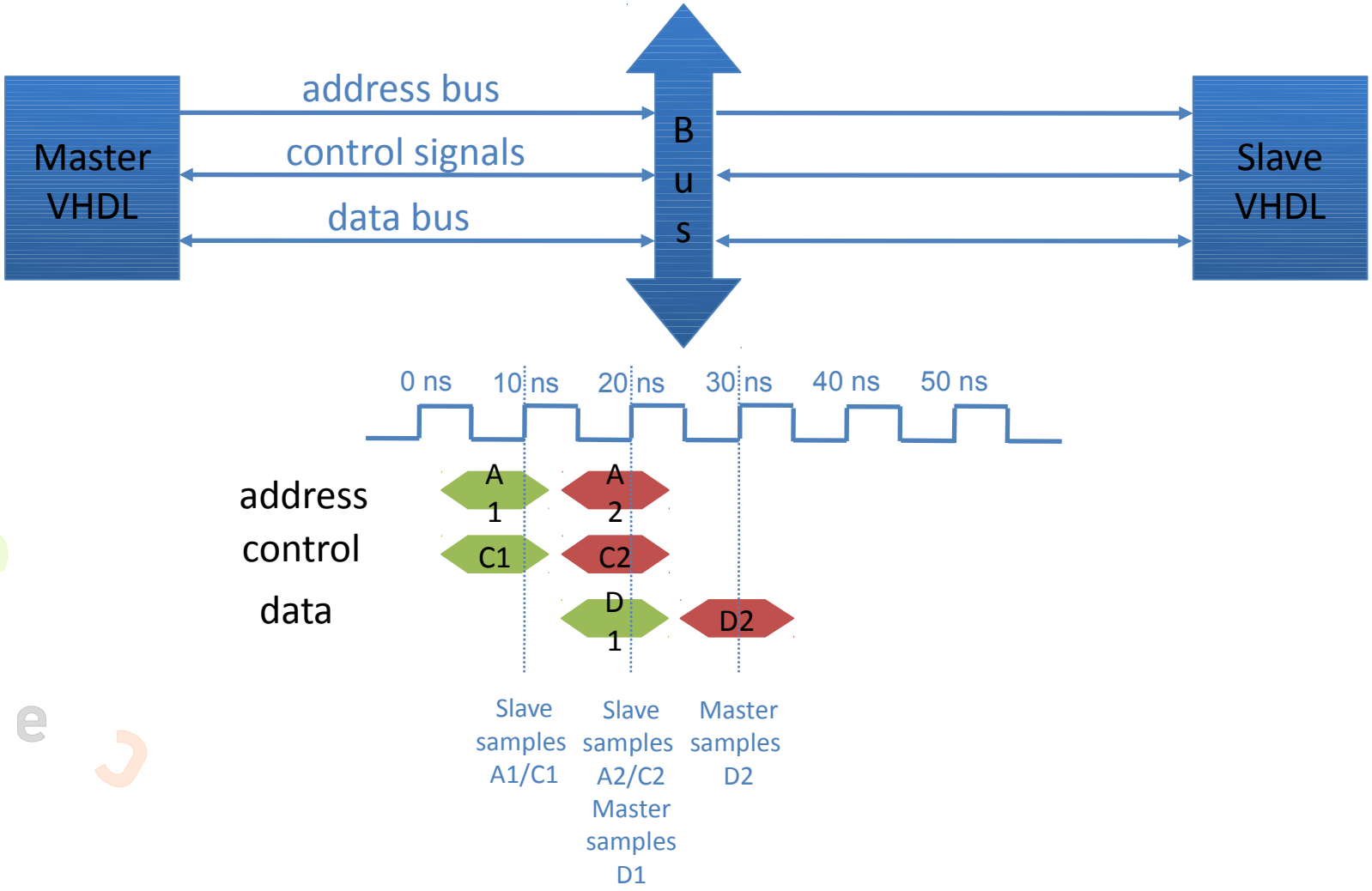
- Blocking Interfaces
- DMI
- Quantum
- Sockets
- Generic Payload
- Phasen
- Non-blocking Interfaces

Source: www.osci.org (2011)

TLM: Abstraction of communication using function calls.

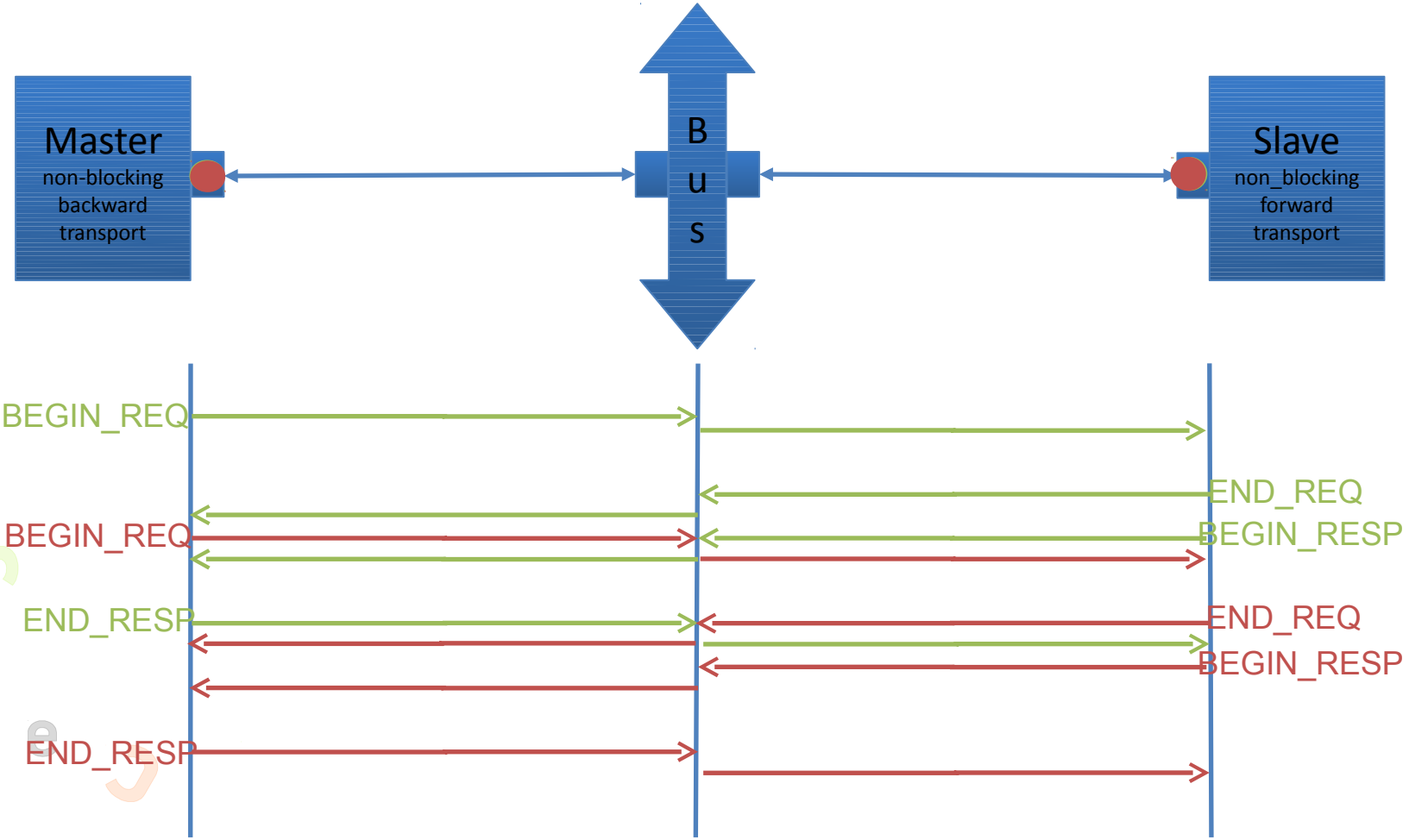
Hardware Verification

Cycle-Timed Modeling



Architecture Analysis

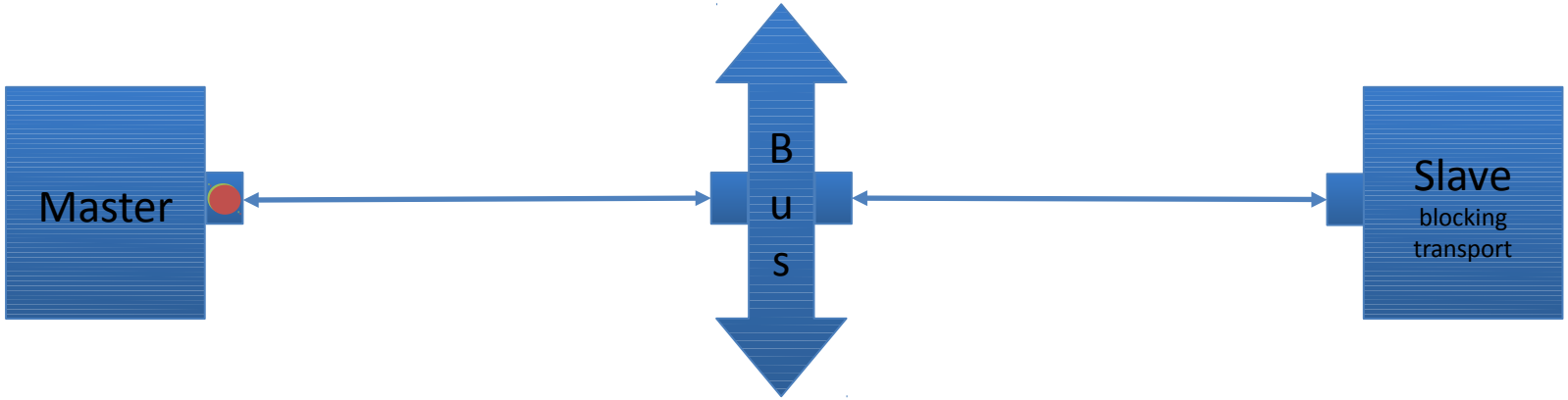
TLM 2.0 Approximately Timed Coding Style (AT)

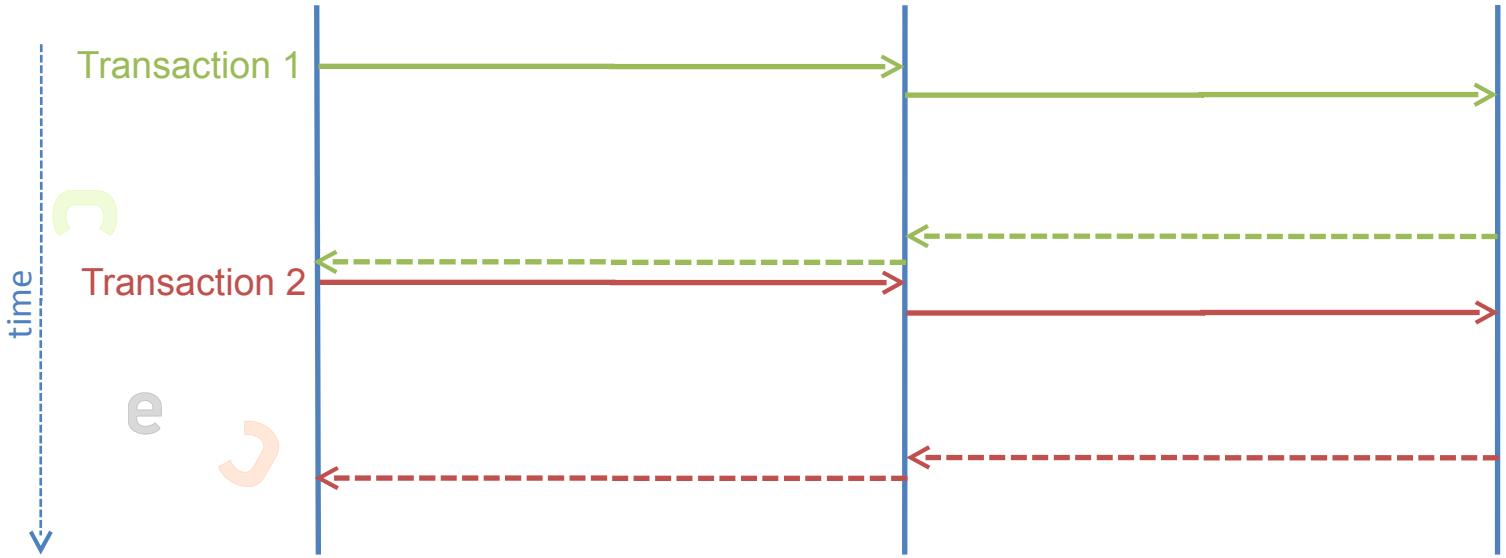


Some concurrent processes synchronizing at significant points in time.

Software Development

TLM 2.0 Loosely Time Coding Style (LT)





Very little concurrency – blocking communication only.

Drawbacks of VP Approach

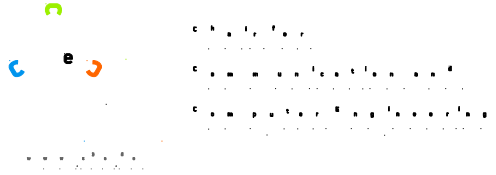
Availability of Simulation IP

Additional EDA costs

- In Aerospace domain trusted components are reused many times.
- The long IP life cycle repays the simulation models.

Outline

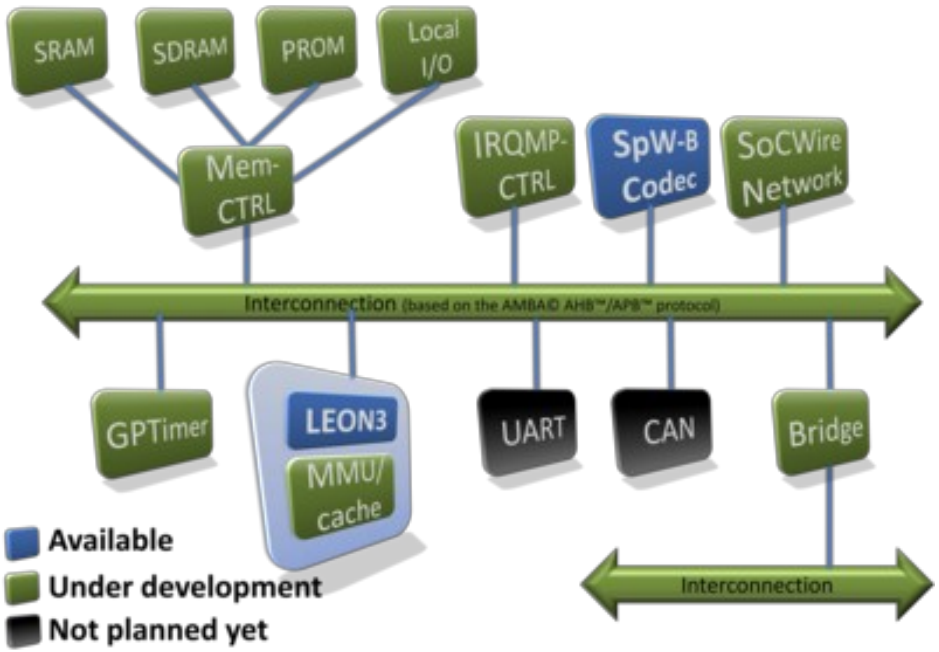
SoCRocket



Introduction to Virtual Platforms and TLM

SoCRocket VP

Verification and Documentation



http://www.esa.int/TEC/Microelectronics/SEM151AMT7G_0.html

TLM Simulation Models for Aeroflex GRLIB library
Modeling library and tools

Library structure

models

templates

tools

platforms

Library structure

Models

models

templates

tools

platforms

Simulation Models for LT and AT abstraction
LEON processor simulator
Component-level tests

Library structure

Templates

Templates for platform models
(e.g. single core, multi-core)
Structural information – top level C code
Parameters for Design Space Exploration

Library structure

Tools

Platform Configurator
(generates platforms from templates)
Co-Simulation Adapters
Power Monitor
Timing Monitor

Library structure

Platforms

Platform simulators are generated here

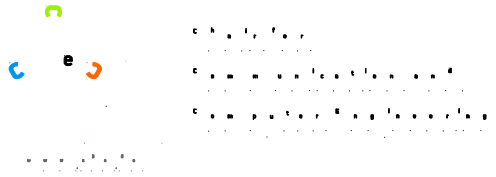
Library structure

WAF – The META build system

Python based build system
(*code.google.com/p/**waf**/*)
Manages all tools of the library

Configuring the Library

./waf configure



GreenSoCs (GreenSockets, GSParams, GreenReg)

Open Virtual Platform Infrastructure

www.greensocs.org

ARM/Carbon AMBAKit

TLM2.0 Sockets with AMBA Extensions

www.carbonsystems.org

SystemC/TLM 2.0 Installation

Mentor Modelsim Simulator (optional)

Multi-language simulator for RTL Co-Simulations

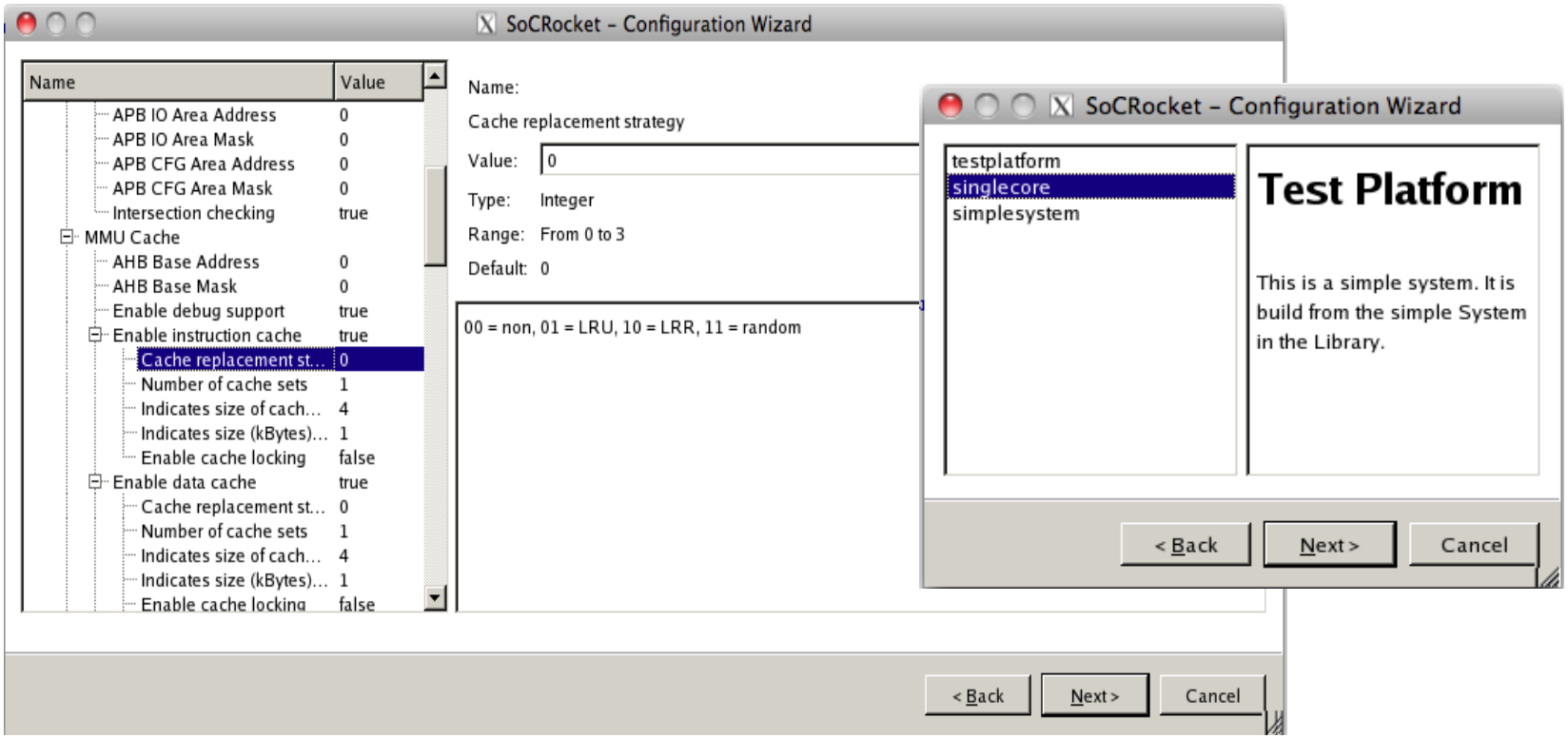
www.mentor.com

Python

GCC, GDB, other GNU

Setting up a system

./waf generate



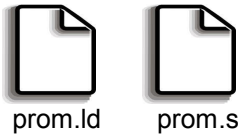
Select an architecture template
(e.g. single core, multi-core, custom)
Configure parameters like cache size, address masks, …
Generate the platform simulator

Compiling the platform

./waf –target=singlecore

Top-level of SystemC simulation (sc_main)
Instantiation of all components

- Parameter definitions (settings from Platform Configurator)
- Defines constructor parameters of all IP blocks



- Boot code for LEON processor
- Linker script for boot code

- Linker script for application

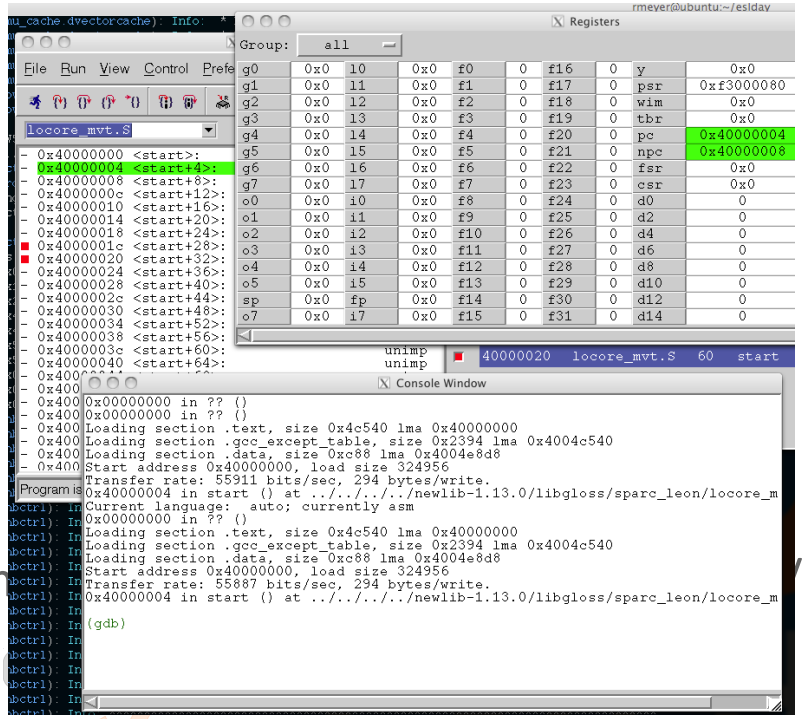
- WAF build script

Result is executable simulator: *./singlecore boot.elf program.elf*

Simulating the platform

Verbosity & Debug

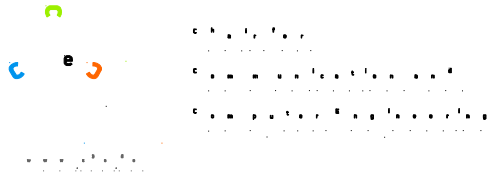
Verbosity of debug output may be configured in four stages (error, warn, info, debug)



Sim / DDD / INSIGHT

Analyze results

Event Monitoring



Event Monitor provides API for Event Recording
IPs register at begin of simulation

EM::registerIP(this,"type")

At runtime time-stamps for begin and end of important events are send to the monitor

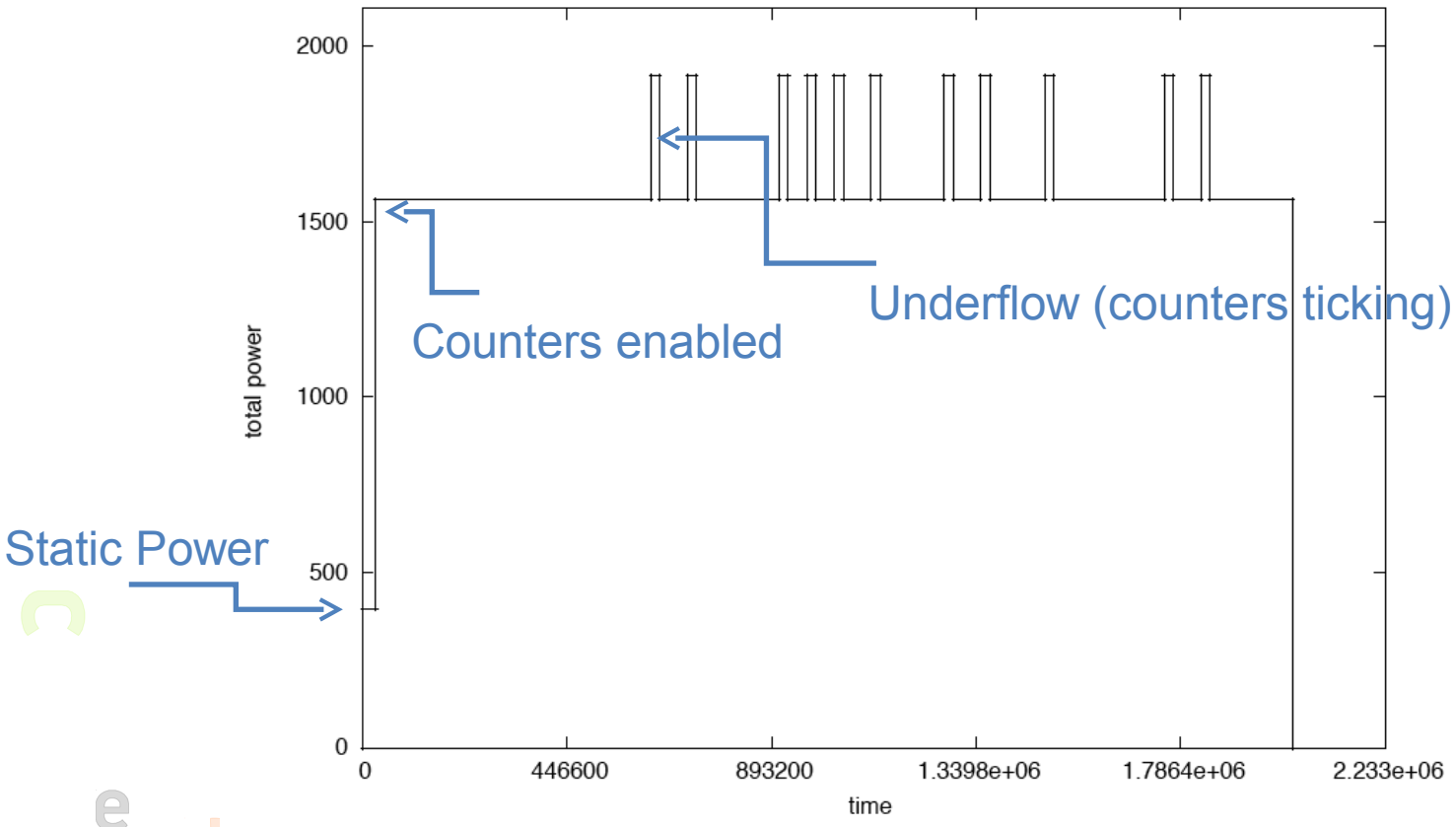
EM::send(this, "event", 1, sc_time_stamp())

Event Monitor maintains hierarchical database of events
After simulation database is analyzed

EM::analyze("power.dat")

Power Profile

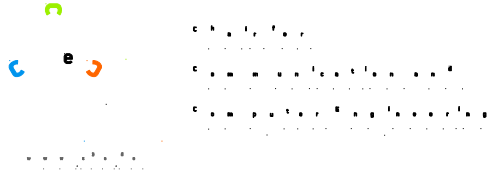
Example GPTimer



Annotation of power information to events

Outline

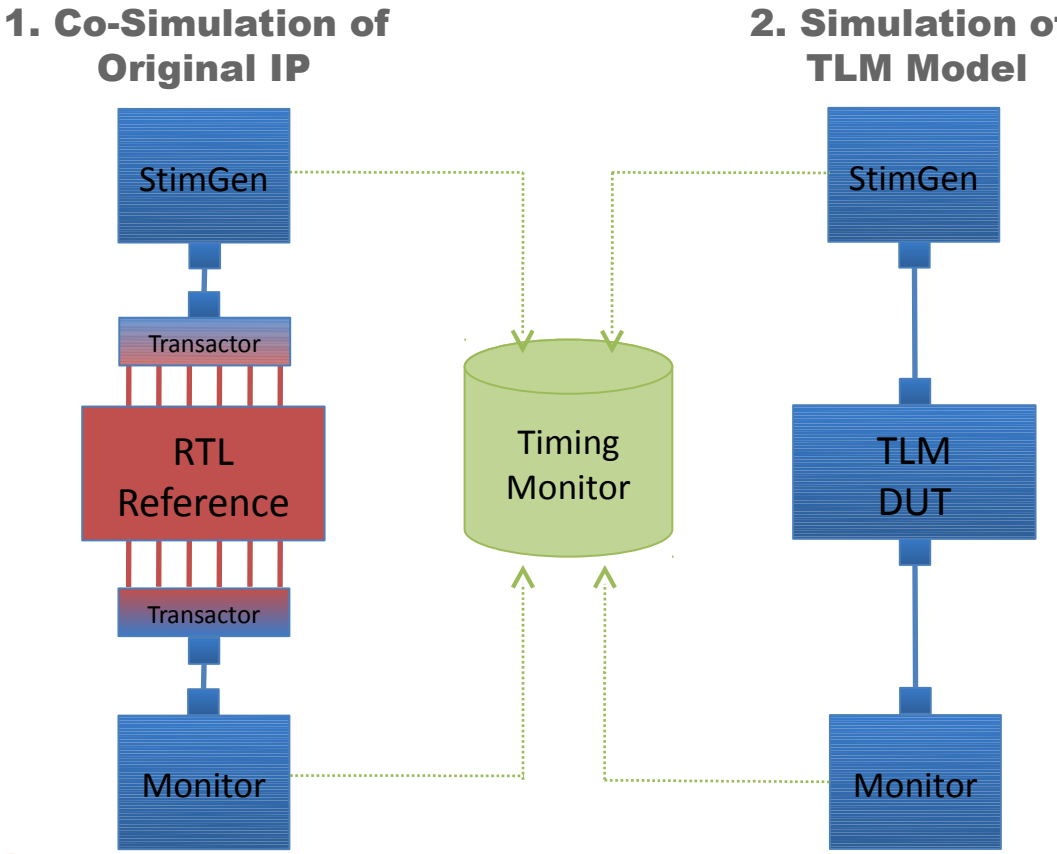
SoCRocket



Introduction to Virtual Platforms and TLM
SoCRocket VP
Verification

Verification

Behavior & Timing

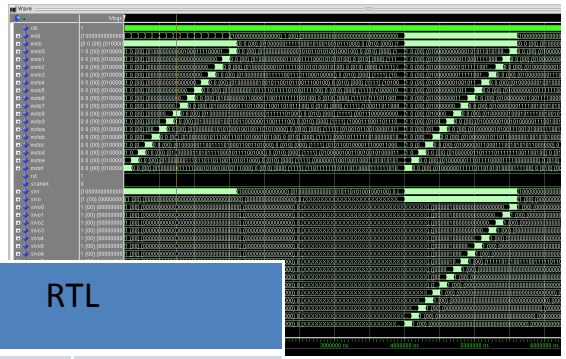


TLM Testbed is re-used for both simulations

Timing Monitor keeps track of simulation time

Verification

Timing Monitor



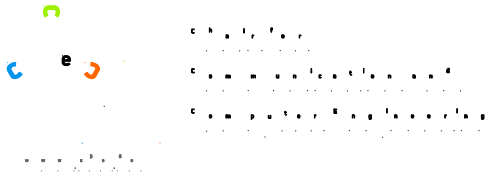
Example: Simulation of AHBCTRL with 16 masters and 16 slaves

	LT		AT		RTL	
Phase	Start	End	Start	End	Start	End
1	100	10100	100	10100	100	10100
2	100	10100	100	20100	100	20100
…	…	…	…	…	…	…
Total		**21000**		**359990**		**360140**

LT Timing is far off – LT Router does not model arbitration ✓

Code Coverage

GCOV/LCOV



LCOV - code coverage report

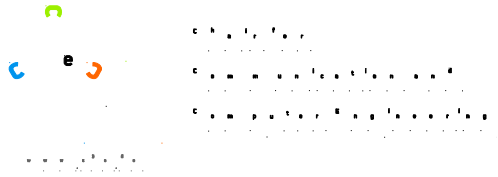
				Hit	Total	Coverage
Current view:	top level		**Lines:**	3098	5242	59.1 %
Test:	lcov.info		**Functions:**	773	1618	47.8 %
Date:	2011-07-26		**Branches:**	1335	3562	37.5 %

Directory	Line Coverage			Functions		Branches	
common		100.0 %	18 / 18	74.9 %	224 / 299	50.0 %	1 / 2
contrib/transactors		15.1 %	103 / 684	40.7 %	11 / 27	5.6 %	30 / 532
models/ahbctrl		66.1 %	211 / 319	19.5 %	16 / 82	44.4 %	63 / 142
models/gptimer		88.5 %	255 / 288	36.1 %	39 / 108	46.7 %	100 / 214
models/irqmp		98.0 %	144 / 147	25.6 %	20 / 78	70.2 %	73 / 104
models/mctrl		46.2 %	249 / 539	22.9 %	22 / 96	32.0 %	135 / 422
models/mmu_cache/lib		68.2 %	899 / 1318	39.5 %	77 / 195	47.6 %	395 / 829
models/socwire		54.0 %	516 / 955	41.5 %	73 / 176	33.2 %	168 / 506
models/utils		70.3 %	600 / 853	45.2 %	75 / 166	55.6 %	253 / 455
signalkit/signalkit_h		85.1 %	103 / 121	55.2 %	216 / 391	32.9 %	117 / 356

Generated by: LCOV version 1.9

Code coverage still too low for most of the IPs.
Verification is work in progress

Summary



Virtual Platforms are abstract hardware models that are simulated by software.

Virtual Platforms and TLM can help to manage the raising complexity in system design

The SoCRocket VP provides simulation models and infrastructure for Design Space Exploration of LEON based SoCs.

Project planned to be completed end of 2011